Using TSB43Cx43A: S/PDIF Over 1394

Connectivity Solutions

ABSTRACT

This document details the requirements and how to set up the TSB43Cx43A (iCEM) to support S/PDIF (IEC60958). This application report tells how to configure iCEM to both transmit S/PDIF over 1394 and receive S/PDIF formatted packets from 1394.

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1 S/PDIF (IEC60958) Transmit Over 1394

The iCEM supports S/PDIF transmit over 1394 by decoding the bi-phase mark encoded S/PDIF data and packetizing the decoded data into an IEC61883-6 specification compliant format.

The iCEM is capable of decoding an S/PDIF stream encoded with any of the following sampling frequencies (fs): 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, and 192 kHz.

iCEM has the following two dedicated interfaces through which a S/PDIF stream can be routed:

- Iso data path 0 (HSDI0_60958_IN and HSDI0_AMCLK_IN)
- Iso data path 1 (HSDI1_60958_IN and HSDI1_AMCLK_IN)

An Iso data path can only support one data type at a time. For example, if Iso data path 0 is being using for S/PDIF transmit, then this same data path cannot be used for MPEG2 transmit.

1.1 Configuring S/PDIF Data Type

The iCEM must be configured to transmit S/PDIF data over 1394. Since iCEM supports several different data types, such as MPEG and DV, the software must configure iCEM appropriately to support the IEC60958 data type. See Table 1.

Table 1. Configuring Data Types

Iso*Cfg.DataType	HSDI*Cfg.Mode	Description
0x7	0x5	IEC60958 conformant data
0x8	0x6	IEC60958 conformant data converted to MLPCM data. This mode is only used for RX.
0x9	0x7	MBLA. DVD-audio
0xA	0x8	SACD
0xD	0x9	Command base rate control (flow control). Used only for receive.

1.2 Blocking Transmission Mode

Two types of tranmission methods are defined in the 1394 Trade Association Audio and Music Data Transmission Protocol 2.1.

- Non-blocking transmission method
- Blocking transmission method

The iCEM only performs the blocking transmission method. It can receive 1394 packets that are transmitted using either method. In the blocking transmission method, all packets are transmitted using the same size. See Figure 1.

For information on the different transmission methods see the 1394 Trade Association Audio and Music Data Transmission Protocol 2.1.

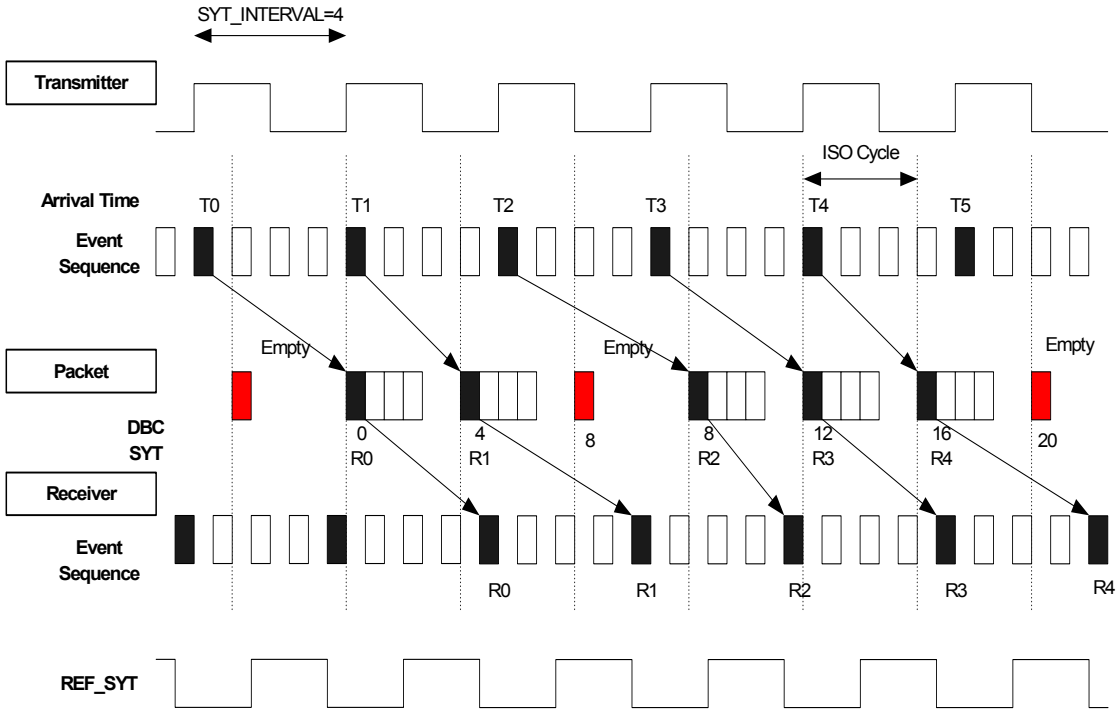

Figure 1. Blocking Transmission Method

1.3 MCLK Required for S/PDIF Decode

Embedded in an S/PDIF stream is a 128-fs MCLK. In a typical S/PDIF receiver, the MCLK would be extracted from the S/PDIF stream and used to decode the bi-phase mark enabled data. iCEM does NOT have the MCLK extraction capability. In order for iCEM to decode the S/PDIF stream, an MCLK that is synchronous to the S/PDIF stream must be provided. The MCLK frequency can be one of any of the following: 128 fs, 256 fs, 384 fs, and 768 fs. The default operation for iCEM is that a 128-fs MCLK input into the HSDI*_AMCLK_IN pin. If any of the other three frequencies are used, then the Aud*TxCfg.MClkin must be programmed as appropriate. All frequencies above 128 fs are divided down to create the 128-fs clock. See Table 2 for the programmable options of Aud*TxCfg.Mclkin.

Table 2. Aud*TxCfg.Mclkin Settings

Aud*TxCfg.Mclkin	MCLK Frequency
1’b00	128 fs (default)
1’b01	256 fs
1’b10	384 fs
1’b11	768 fs

1.4 Sample Frequency (fs) and MCLK

As mentioned above, iCEM supports several combinations of sampling frequencies and MCLK frequencies. Table 3 depicts which sampling frequency is supported for each MCLK frequency.

Table 3. Fs vs MCLK

Fs	128fs MCLK	256fs MCLK	384fs MCLK	768fs MCLK
32 kHz	4.096 MHz	8.192 MHz	12.288 MHz	24.576 MHz
44.1 kHz	5.6448 MHz	11.2896 MHz	16.934 MHz	33.8688 MHz
48 kHz	6.144 MHz	12.288 MHz	18.432 MHz	36.864 MHz
88.2 kHz	11.2896 MHz	16.934 MHz	33.8688 MHz	Not supported
96 kHz	12.288 MHz	18.432 MHz	36.864 MHz	Not supported
176.4 kHz	22.5792 MHz	Not supported	Not supported	Not supported
192 kHz	24.576 MHz	Not supported	Not supported	Not supported

1.5 Empty Packet Support

At certain times, a complete audio packet is not available for transmission over 1394, or the interface is muted. During these times, it is important that the transmit node transmits a packet during its isochronous time period. iCEM transmits one of two types of packets, an empty packet or a no-data packet.

1.5.1 Empty Packet Mode

The empty packet only contains an H0, two CIP headers, and no data payload. The value of the SYT field is typically all 1s. At certain times, the SYT field contains a valid timestamp as depicted in Table 4.

Table 4. Empty Packet With Valid SYT

IsoDPEn	HSDIEn	DataPinEn	Mute	NoDataEvent	DataPinEn
1	0	X	X	0	SYT=0xFFFF
1	1	X	1	0	SYT during valid data period. SYT=0xFFFF during no data period.
1	1	0	0	0	No-data packet with SYT during valid data period. Empty packet with SYT=0xFFFF during a no data period.
1	1	1	0	0	Empty packet transmitted with SYT=0xFFFF during a no data period. At all other times, a data packet with a SYT is transmitted.

1.5.2 No-Data Packet Mode

The no-data packet is similar to the empty packet, with the addition of a data payload of DBS * SYT_INTERVAL. The specific values of the data payload are determined by the following two registers:

- Aud*NoData (defaults to 0xCF000000)
- Anc*NoData (defaults to 0xCFCF0000).

Unlike the empty packet, the no-data packet transmits the FDF field to all 1s whenever SYT equals 0xFFFF. As with empty packets, the value of the SYT field is typically all 1s. At certain times, the SYT field contains a valid timestamp as depicted in the Table 5.

Table 5. No-Data Packets With Valid SYT

IsoDPEn	HSDIEn	DataPinEn	Mute	NoDataEvent	DataPinEn
1	0	X	X	1	SYT=0xFFFF
1	1	X	1	1	SYT during valid data period. SYT=0xFFFF during no data period.
1	1	0	0	1	No-data packet with SYT during valid data period. No-data packet with SYT=0xFFFF during a no data period.
1	1	1	0	1	No-data packet transmitted with SYT=0xFFFF during a no data period. At all other times, a data packet with an SYT is transmitted.

1.6 S/PDIF Packetization

1.6.1 IEC60958 Conversion

According to the IEC60958 specification, the decoded S/PDIF stream has the subframe format as depicted in the Table 6.

Table 6. IEC60958 Subframe Format

0							7																		27				31
PA			AUX				(LSB)													Audio Sample					(MSB)			V	U	C	P

Where:

PA … Sync preamble

V … Validity flag

U … User data

C … Channel status

P … Parity bit

iCEM reassembles the above IEC60958 subframe into the following format, as shown in Table 7 for transmit over 1394.

Table 7. IEC60958 Subframe Over 1394

31				27				23																	4				0
PA				P	C	U	V	(MSB)												Audio Sample							(LSB)	AUX			

1.6.2 1394 Audio Isochronous Headers (H0, CIP0, and CIP1)

iCEM automatically inserts the isochronous headers for each audio packet. The isochronous headers look like Figure 2. It is the software's responsibility to program the appropriate values in these specific fields: Channel, DBS, FMT, FDF, and SY. Hardware handles configuring all the other fields.

Figure 2. 1394 Audio Isochronous Headers

	31							23							15							7							0
H0	DataLength														Tag	Channel							tCode				SY		
	Header CRC																												
CIP0	0	0	SID							DBS							FN	QPC		SPH	Rsv		DBC						
CIP1	0	1	FMT							FDF							SYT												

Field Name	Field Description
DataLength	Indicates the number of bytes in the current packet. This field is updated by hardware using the following formula: Datalength = DBS x SYT_INTERVAL x 4
Tag	Indicates the format of data carried by the isochronous packet. For all 61883 packets (all audio formats), this field is always 1'b01. A 1'b01 indicates that a CIP header is included in the packet.
Channel	The isochronous channel the current packet is associated. Value determined by software. Iso x TxHdr.ChanNum
tCode	The transaction code for the current packet. It is always Ah for 61883 packets.
SY	Carries the transaction layer specific synchronization bits. Value determined by software. If encryption is enabled, this field is updated by hardware.
DBC	Data block count. An incremental value that rolls over to 0 after 255. This field is automatically updated by hardware.
DBS	Data block size. For S/PDIF the data block size should be programmed to 02h due to the fact that S/PDIF only has two channels (a left and a right channel). Iso x TxCIP0.DBS
SYT	A 16-bit timestamp that is added by hardware. The timestamp is the lower 16 bits of the cycle timer register plus a programmed offset. The timestamp is time when the specified event is to be presented at the receiver.
SID	Source ID. This field is automatically generated by hardware.
FN	Fraction number. This field is automatically determined by hardware for audio.
FMT	Format type. Software determines the value of this field for audio. For S/PDIF, the FMT field should be programmed to 10h. A 10h indicates the format is for audio and music. Iso x TxCIP1.FMT
FDF	Format dependent field. See the table describing the FDF field. This field is determined by software. Iso x TxCIP1.FDF
QPC	Quadlet padding count. This field is automatically determined by hardware.

Table 8. FDF Description

FDF						Description
0	**0**	**0**	**0**	**N**	**SFC**	
0	0	0	0	0	000	Clock based rate control. Fs = 32 kHz
0	0	0	0	0	001	Clock based rate control. Fs = 44.1 kHz
0	0	0	0	0	010	Clock based rate control. Fs = 48 kHz
0	0	0	0	0	011	Clock based rate control. Fs = 88.2 kHz
0	0	0	0	0	100	Clock based rate control. Fs = 96 kHz
0	0	0	0	0	101	Clock based rate control. Fs = 176.4 kHz
0	0	0	0	0	110	Clock based rate control. Fs = 192 kHz
0	0	0	0	1	000	Command based rate control. Fs = 32 kHz
0	0	0	0	1	001	Command based rate control. Fs = 44.1 kHz
0	0	0	0	1	010	Command based rate control. Fs = 48 kHz
0	0	0	0	1	011	Command based rate control. Fs = 88.2 kHz
0	0	0	0	1	100	Command based rate control. Fs = 96 kHz
0	0	0	0	1	101	Command based rate control. Fs = 176.4 kHz
0	0	0	0	1	110	Command based rate control. Fs = 192 kHz

1.6.3 SYT_INTERVAL

The SYT_INTERVAL denotes the number of data blocks between two successive valid SYTs (timestamps). The SYT_INTERVAL varies based on the sampling frequency. Using Table 9, the software programs the Aud*TxCfg.SYTInterval to the appropriate value. iCEM uses this STY_INTERVAL with the data block size (DBS) to determine the data length of the audio packet.

Table 9. SYT_INTERVAL for Specific fs

Sampling Frequency (fs)	SYT_INTERVAL	Aud*TxCfg.SYTInterval	DataLength w/ DBS = 2
32 kHz	8	0x0	64 bytes
44.1 kHz	8	0x1	64 bytes
48 kHz	8	0x1	64 bytes
88.2 kHz	16	0x2	128 bytes
96 kHz	16	0x2	128 bytes
176.4 kHz	32	0x3	256 bytes
192 kHz	32	0x3	256 bytes

1.6.4 TimeStamp (SYT)

For each DBS*SYT_INTERVAL, a timestamp is generated. This timestamp is the lower 16-bits of the cycle timer register plus a programmable offset. The timestamp is used by the receive node to reproduce the transmitting nodes sampling clock (fs).

This offset is defined according to the *1394 Trade Association Audio and Music Data Transmission Protocol 2.1* as a transfer delay. The transfer delay accommodates a default transfer delay of 479.17 μs (the maximum latency time of CIP transmission through an arbitrated short bus reset.) plus the delay of transmitting the data payload. It is recommended that software program the Iso*TmStmp.Offset register with the appropriate value according to the Table10.

Table 10. Transfer Delay for Blocking Transmission

Fs	Transfer Delay	Iso*TmStmp.Offset
32 kHz	729.17 μs	0x5A00
44.1 kHz	660.58 μs	0x536A
48 kHz	645.84 μs	0x5200
88.2 kHz	660.58 μs	0x536A
96 kHz	645.84 μs	0x5200
176.4 kHz	660.58 μs	0x536A
192 kHz	645.84 μs	0x5200

1.6.5 Complete 1394 S/PDIF Packet

Using the information from above (SYT_INTERVAL, H0 and CIP Headers, DBS), the 1394 packet is created. The amount of audio data provided within a particular packet is dependent on the DBS value and the SYT_INTERVAL. For IEC60958, there are only two channels defined in the specification. For this reason, the DBS is fixed at two. From Table 9, the SYT_INTERVAL varies based on sampling frequency. For example, for 48-kHz sampling frequency the SYT_INTERVAL is eight, but for 96 kHz the SYT_INTERVAL is 16. Figure 3 assumes a SYT_INTERVAL of eight.

Figure 3. 1394 IEC60958 Packet

<table>
<tr><td></td><td>31</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>23</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>15</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>7</td><td></td><td></td><td></td><td></td><td></td><td></td><td>0</td></tr>
<tr><td>H0</td><td colspan="16">DataLength</td><td colspan="2">Tag</td><td colspan="6">Channel</td><td colspan="4">tCode</td><td colspan="4">SY</td></tr>
<tr><td></td><td colspan="32">Header CRC</td></tr>
<tr><td>CIP0</td><td>0</td><td>0</td><td colspan="6">SID</td><td colspan="8">DBS</td><td colspan="2">FN</td><td colspan="3">QPC</td><td>SPH</td><td colspan="2">Rsv</td><td colspan="8">DBC</td></tr>
<tr><td>CIP1</td><td>0</td><td>1</td><td colspan="6">FMT</td><td colspan="8">FDF</td><td colspan="16">SYT</td></tr>
<tr><td>B</td><td>0</td><td>0</td><td>1</td><td>1</td><td>P</td><td>C</td><td>U</td><td>V</td><td colspan="24">Ch 1 data</td></tr>
<tr><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>P</td><td>C</td><td>U</td><td>V</td><td colspan="24">Ch 2 data</td></tr>
<tr><td>M</td><td>0</td><td>0</td><td>0</td><td>1</td><td>P</td><td>C</td><td>U</td><td>V</td><td colspan="24">Ch 1 data</td></tr>
<tr><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>P</td><td>C</td><td>U</td><td>V</td><td colspan="24">Ch 2 data</td></tr>
<tr><td>M</td><td>0</td><td>0</td><td>0</td><td>1</td><td>P</td><td>C</td><td>U</td><td>V</td><td colspan="24">Ch 1 data</td></tr>
<tr><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>P</td><td>C</td><td>U</td><td>V</td><td colspan="24">Ch 2 data</td></tr>
<tr><td>M</td><td>0</td><td>0</td><td>0</td><td>1</td><td>P</td><td>C</td><td>U</td><td>V</td><td colspan="24">Ch 1 data</td></tr>
<tr><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>P</td><td>C</td><td>U</td><td>V</td><td colspan="24">Ch 2 data</td></tr>
<tr><td>M</td><td>0</td><td>0</td><td>0</td><td>1</td><td>P</td><td>C</td><td>U</td><td>V</td><td colspan="24">Ch 1 data</td></tr>
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<tr><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>P</td><td>C</td><td>U</td><td>V</td><td colspan="24">Ch 2 data</td></tr>
<tr><td></td><td colspan="32">Data CRC</td></tr>
</table>

1.7 Example: TX 44.1-kHz S/PDIF Over 1394 (Clock Recovery)

In this section, an example of how to configure iCEM to transmit S/PDIF data over 1394 is discussed. This particular example assumes clock based rate control is used. Since both Isochronous data paths, 0 and 1, support S/PDIF transmit over 1394, this example can be used for either data path.

1. Configure the Iso data type to be IEC60958 (serial interface). This means Iso*Cfg.DataType should be programmed to 0x7.
2. Configure the HSDI mode to be IEC60958. This means HSDI*Cfg.Mode should be programmed to 0x5.
3. Next, configure the direction of the isochronous data path to transmit. Iso*Cfg.Direction = 1.
4. iCEM requires a MCLK that is synchronous to the S/PDIF stream. The frequency of HSDI*_AMCLK_IN must be programmed into the Aud*TxCfg.Mclkin register. For this example, lets assume that HSDI*_AMCLK_IN is 256 fs. A value of 0x1 should be programmed into Aud*TxCfg.Mclkin.

5. iCEM does support adding all the appropriate headers for the S/PDIF packet. This feature must be activated by setting the following bit: Iso*TxCfg.HdrInsert = 1.
6. Next, configure the software controllable fields within the headers. A 44.1-kHz sampling frequency over S/PDIF should have the following fields programmed. It is important to note, the receive node is listening on a specific isochronous channel. For this example, the assumption is the receive node is listening to channel 32.
    - Iso*TxCIP0.DBS = 0x02
    - Iso*TxCIP1.FMT = 0x10
    - Iso*TxCIP1.FDF = 0x01FFFF
    - Iso*TxHdr.ChanNum = 0x20
7. The transfer delay for 44.1 kHz of 660.58 μs should be programmed next. Software should program the transfer delay into the following register: Iso*TmStmp.Offset = 0x536A.
8. Enable the timestamp insertion. This is done by the setting Iso*TmStmp.Insert = 1.
9. The next step is to program the SYT_INTERVAL for 44.1 kHz. Software should program the SYT_INTERVAL as follows: Aud*TxCfg.SYTInterval = 0x1.
10. Next, software tells iCEM how many audio channels are being input into the HSDI interface. Because IEC60958 only supports two channels, software should program Aud*TxCfg.Channels = 2.
11. iCEM supports two forms of no data packets, empty packet mode and no-data packet mode. For this example, it is assumed that software would prefer to use the empty packet mode. Aud*TxCfg.NoDataEvent = 0.
12. Next, software should enable the transmission of full sample word packets. This is done by setting Aud*TxCfg.DataPinEn to a 1. Also, Iso*TxCfg.Hold is cleared so that data in the buffer can be transmitted over 1394.
13. Finally, the data paths must be enabled so that audio packets can be transmitted over 1394. To perform this task, software performs the following two tasks in the order specified.
    a. Aud*TxCfg.IsoDP0En = 1
    b. Aud*TxCfg.HSDI0En = 1

After following steps 1 through 13, iCEM is now ready to transmit IEC60958 (S/PDIF) packets over 1394. The S/PDIF stream that is input into HSDI*_60958_IN is decoded by iCEM using the HSDI*_AMCLK_IN and is transmitted over 1394 when a complete packet (DBS*SYT_INTERVAL) is in the buffer.

The 13 steps above can be summarized in the following script:

```
LLC.LinkCfg.CycMasAuto      = 1
LLC.LinkCfg.CycTmrEn        = 1
```

LLC.PhyCfg.LPS = 1

Iso0.Iso0Cfg.DataType = 0x7

Iso0.Iso0Cfg.Direction = 1

Iso0.Iso0TxCfg.HdrInsert = 1

Iso0.Iso0TxCfg.Hold = 0

Iso0.Iso0TxHdr.ChanNum = 0x20

Iso0.Iso0TxCIP0.DBS = 0x02

Iso0.Iso0TxCIP1.FMT = 0x10

Iso0.Iso0TxCIP1.FDF = 0x01FFFF

Iso0.Iso0TmStmp.Offset = 0x536A

Iso0.Iso0TmStmp.Insert = 1

Iso0.HSDI0Cfg.Mode = 0x5

Aud0.Aud0TxCfg.MClkIn = 0x1

Aud0.Aud0TxCfg.Channels = 0x2

Aud0.Aud0TxCfg.SYTInterval = 0x1

Aud0.Aud0TxCfg.ChAssign = 0x1

Aud0.Aud0TxCfg.NoDataEvent = 0

Aud0.Aud0TxCfg.DataPinEn = 1

Aud0.Aud0TxCfg.Mute = 0

Aud0.Aud0TxCfg.IsoDP0En = 1

Aud0.Aud0TxCfg.HSDI0En = 1

2 S/PDIF (IEC60958) Receive Over 1394

The iCEM does support receiving IEC61883-6 formatted packets, specifically S/PDIF, MBLA, and SACD. Since iCEM does support multiple types of audio formats, it is the software's responsibility to configure iCEM appropriately for each format. This section discusses the items that the software should be aware of to receive S/PDIF formatted packets.

NOTE: iCEM cannot receive audio packets into isochronous buffer 0.

2.1 Determining the IEC61883-6 Packet Type

As mentioned above, iCEM supports three different types of IEC61883-6 formatted packets. For each type of packet, a label field specifies what type of packet is being transmitted. iCEM supports labels values 00-5Fh and C0-EF. For an S/PDIF formatted packet, the label is in the range of 0x00 through 0x3F.

The label of the received packet can be determined by monitoring the Aud*Mntr0, Aud*Mntr1, and Aud*Mntr2, and Aud*Mntr3 registers. Any change in a label is flagged by a change in Aud*ExCPUInt.LabelChg. It is recommended that software either monitor this field by polling the register, or monitor through an interrupt service routine. When a label change occurs, it is recommended that software mute the audio interface by setting the Aud*RxCfg.SWMute to '1'. Once the data type is determined and programmed into the Iso1Cfg.DataType and HSDI1Cfg.Mode, the mute can be removed.

Table 11. Label Definition

Value (Hex)	Description
00-3F	IEC60958 conformant (S/PDIF)
40-4F	Multi-bit linear audio (MBLA)
50-57	One-bit audio (plain SACD)
58-5F	One-bit audio (encoded SACD)
60-7F	Reserved
80-83	MIDI conformant
84-87	Extended music data
88-8B	SMPTE time code conformant
8C-8F	Sample count
90-BF	Reserved
C0-EF	Ancillary data
F0-FF	Reserved

2.2 Determining the Sampling Frequency (fs)

The sampling frequency for all packets is contained within the FDF field of the CIP1 header. In Table 8 the coding of the sampling frequency is described. Software can determine the value of the FDF field through the Iso1RxCIP1.FDF register. Any change in the FDF field is flagged by the Iso1ExCPUInt.FDFChg register. When a change occurs in the FDF field, this indicates that the sampling frequency has changed and, as a result, software should mute the interface until it can configure iCEM for the new sample rate.

In clock based rate control mode, a change in the FDF field may require software to change the Aud*RxCfg.VCOClkDiv register. The VCOClkDiv register is used by iCEM to generate the BCLK or the 128-fs clock to encode the IEC60958 packets. For example, if the FDF field of the incoming 1394 packet is 0x04, then this would indicate a 96-kHz sampling rate for S/PDIF. Software would need to program the Aud*RxCfg.VCOClkDiv to 0x3.

Table 12. VCOClkDiv[2:0] Definition

Aud*RxCfg. VCOClkDiv (bin)	MLPCM (64fs) or SACD (Div Ratio)	MLPCM (48fs) (Div Ratio)	IEC60958 (128fs) (Div Ratio)	VCOCLK (MHz)	SFC (bin)
000	1/18	1/24	1/9	36.864	000
001	1/12	1/16	1/6	33.868	001
001	1/12	1/16	1/6	36.864	010
010	1/9	1/12	-	33.868	000*2
011	1/6	1/8	1/3	33.868	011, 001*2
011	1/6	1/8	1/3	36.864	100, 010*2
100	-	1/6	-	36.864	000*4
101	1/3	1/4	1/1.5	33.868	101
101	1/3	1/4	1/1.5	36.864	110

2.3 Audio Master Clock (MCLK)

iCEM is capable of generating a MCLK for all three (S/PDIF, MBLA, and SACD) data formats. When clock based rate control is being used, iCEM outputs a master clock (HSDI1_AMCLK_OUT) at a frequency determined by software. This frequency is determined by the value programmed into the PLLCfg.Nx. The value stored in this register is used to divide the VCO_CLK to generate the HSDI1_AMCLK_OUT. Table 13 depicts all the master clock frequencies iCEM can generate. If a master clock not listed in the table is required, then command based rate control (flow control) mode must be used.

In command-based rate control, the system provides the master clock. The system inputs the master clock on the HSDI1_AMCLK_IN pin.

Table 13. PLLCfg.Nx Programmable Options

PLLCFg.Nx	Divide Ratio	VCO_CLK	HSDI1_AMCLK_OUT
0x0	Reserved	Reserved	Reserved
0x1	1/1	33.868 MHz	33.868 MHz
0x1	1/1	36.864 MHz	36.864 MHz
0x2	1/2	33.868 MHz	16.934 MHz
0x2	1/2	36.864 MHz	18.432 MHz
0x3	1/3	33.868 MHz	11.289 MHz
0x3	1/3	36.864 MHz	12.288 MHz
0x4	1/4	33.868 MHz	8.467 MHz
0x4	1/4	36.864 MHz	9.216 MHz
0x5	1/5	33.868 MHz	6.774 MHz
0x5	1/5	36.864 MHz	7.373 MHz
0x6	1/6	33.868 MHz	5.645 MHz
0x6	1/6	36.864 MHz	6.144 MHz
0x7	1/7.5	33.868 MHz	4.516 MHz
0x7	1/7.5	36.864 MHz	4.915 MHz

2.4 HSDI Output Modes

iCEM can output a received audio packet through one of three following interfaces:

- MPLCM interface
- IEC60958 interface
- HSDI1 interface

The IEC60958 formatted packet can be output through either the MLPCM interface or the IEC60958 interface. A MBLA (DVD-Audio) formatted packet can only be output over the MLPCM interface and a SACD formatted packet can only be output over the HSDI1 interface.

The option for which interface to output an S/PDIF formatted packet is system specific. If it is desired to output an IEC60958 packet to a DAC, then software should use the MLPCM interface. It should be noted that if the validity bit is set to a 1, iCEM mutes the MLPCM interface. In some systems it may be a requirement to output the IEC60958 formatted packet in the bi-phase mark encoded S/PDIF stream.

2.4.1 Serial IEC60958 Interface

One format from which the received 1394 IEC60958 audio packets can be output is the IEC60958 (bi-phase mark, encoded S/PDIF). iCEM outputs the stream using the HSDI1_60958_OUT pin. The audio data is formatted according to the IEC60958 specification. The mode can be selected by performing the following: Iso1Cfg.DataType = 0x7 and HSDI1Cfg.Mode = 0x5.

NOTE: The received 1394 packet must be IEC60958 conformant in order to use this mode.

2.4.2 Serial IEC60958 With MLPCM Interface

The other format from which the received 1394 IEC60958 audio packet can be output is the MLPCM interface. When this mode is selected, the IEC60958 conformant packet is output over the MLPCM in one of four formats: I2S, right justified, left justified, or flow control. Table 14 shows the required settings for each option.

Table 14. IEC60958 Modes

Iso1Cfg.DataType (bin)	HSDI1Cfg.Mode (bin)	Aud1Cfg.MLPCMMode (bin)	Description
0111	0101	N/A	Bi-phase mark encoded S/PDIF stream (IEC60958)
1000	0110	00	Right justified
1000	0110	01	Left justified
1000	0110	10	I2S
1101	1001	11	Flow control

The iCEM also supports both 64 fs and 48 fs BCLK. Software can select either option by programming the appropriate value in the Aud1Cfg.MLPCMSlot register.

2.5 PLL

When using clock based rate control, the iCEM receive node must recover the transmit node's sampling clock (fs). Due to the fact that the iCEM does not contain an internal PLL for this purpose, the system designer must provide an external PLL. It is important to note that iCEM expects the VCOCLK coming from the PLL to be either 33.868 MHz or 36.864 MHz. The system designer should select a PLL that has good lock characteristics at both frequencies.

2.6 Signals for Phase Detector

The iCEM provides two signals that feed into an external phase detector: DIVVCO and REFSYT. See Figure 4.

DIVVCO is a divided version of the VCOCLK. When 1/Nvco counter equals 0, then DIVVCO goes low and when the counter equals Nvco/2, DIVVCO goes high.

The other signal is called REFSYT. The origin of this signal comes from valid SYT (timestamps) for each received packet. When the SYT equals the receivers' node cycle timer, a pulse is generated called SYTMATCH that clears the 1/N counter. When the 1/N counter equals zero, the REFSYT goes low. When the counter equals N/2, the REFSYT goes high. This counter is clocked off the 24.576-MHz isochronous clock.

The value of Nvco and N can be either automatically determined by iCEM or if desired software can program the values. If the system designer wishes to let software determine these values, then iCEM must be put into manual PLL mode (PLLCfg.Mode = 1). Once in manual PLL mode, software can adjust the values of N and Nvco through the following two registers: PLLManN.ManN and PLLManvco.ManNvco. The default operation is automatic PLL mode. When in automatic PLL mode, both REFSYT and DIVVCO are between 4 kHz and 7.35 kHz. The specific value is determined by the sampling frequency (fs).

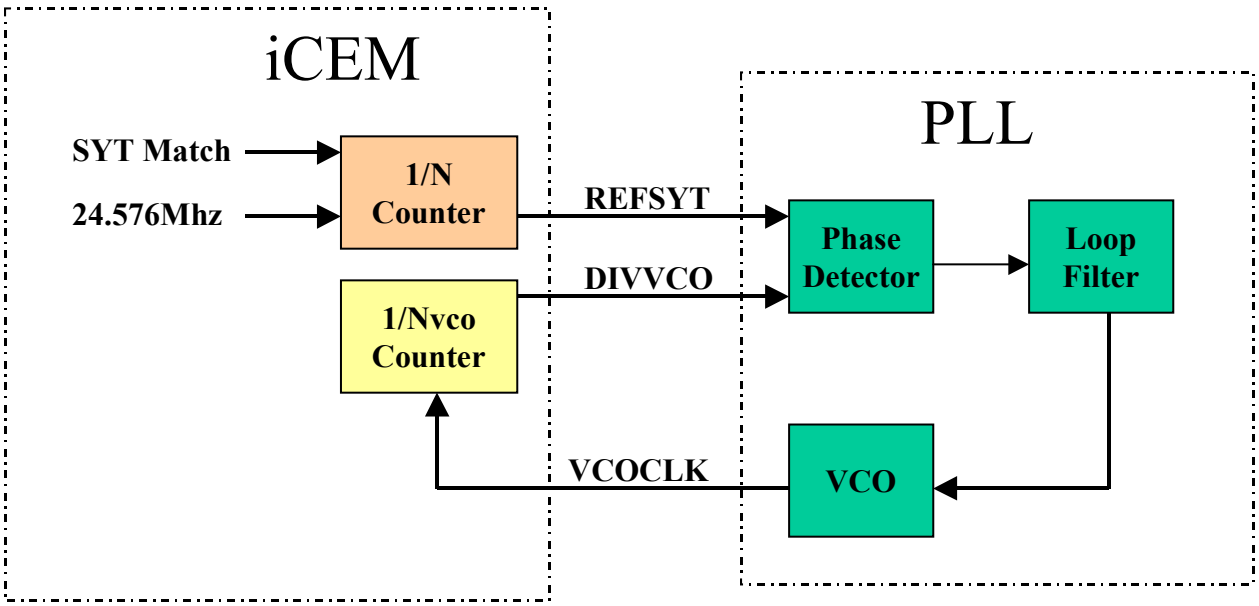

Figure 4. External PLL Connection to iCEM

2.6.1 Lock Detection

iCEM has the following three software programmable counters that are used to determine when the external PLL is locked or not.

- LockWin counter
- OK counter
- NG (no good) counter

The LockWin counter, which is clocked from VCOCLK, determines the size of the lock window. The size of the window is determined by multiplying the VCOCLK by PLLParams.LockWin.

When a SYTMatch occurs within the lock window, the OK counter decrements and the NG counter resets. When a SYTMatch occurs outside the lock window or if it does not occur, the NG counter decrements and the OK counter resets. Once the OK counter equals zero, the PLL is considered locked and the PLLCfg.LockStat bit is set. If the NG counter equals zero, the PLL is not considered locked so the PLLCfg.LockStat bit is cleared. Software can modify the size of the OK and NG counter through the following two registers: PLLParams.OKCnt and PLLParams.NGCnt.

2.7 Mute Control

The audio interface can be muted by both hardware and software. Software controls whether the audio interface is muted or not by the state of the Aud1RxCfg.SWMute bit. See Figure 5. When this bit is set to a 1, the audio interface is muted. Hardware can also control whether or not the audio interface is muted. See Figure 5.

The following three conditions are used by the hardware uses to determine whether or not to mute the audio interface.

- PLL Lock
- Before data is received into RX FIFO, and
- Ancillary no data packet.

The SWMute bit has higher priority over hardware mute. If desired, the system designer can disable the hardware mute feature by clearing the Aud1RxCfg.HWMuteEn bit.

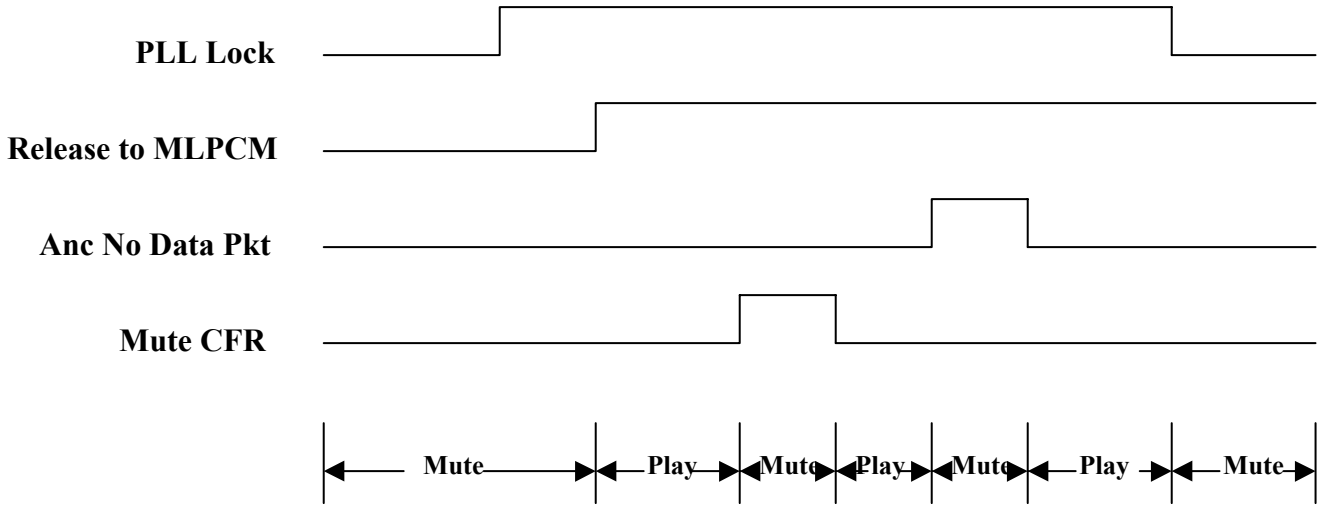

Figure 5. Conditions for Mute

Table 15. Mute Values

Data Type	Mute Value
IEC60958 (S/PDIF)	Bi-phase mark encoded 0
MLPCM or MBLA (DVD audio)	All 0 is sent
SACD	Repeated Aud1RxCfg.MuteCtrl (defaults to 0x96)

2.7.1 Mute Status

The following two means provide mute status to the system:

- Mute status bit
- Mute pin

The mute status bit is located in the Aud1RxCfg registers and when it is set to a 1 the audio interface is muted.

The mute pin, HSDI1_Audio_Mute, is a hardware means to indicate the interface is muted and is asserted on the rising edge of LRCLK or at the data block boundary in SACD mode. Both the status bit and the pin are asserted high, whenever one of the mute conditions above is met.

2.8 Example: RX 44.1 kHz S/PDIF over 1394 (Clock Recovery)

In this example, how to configure iCEM to receive a S/PDIF signal is discussed. For this example, the assumption is that the clock based recovery mode is used.

Steps:

1. The first step is software mutes the MLPCM interface until iCEM is completely configured. Aud1RxCfg.SWMute = 1. This bit defaults to 1. It is also a good idea to make sure hardware mute enable support is enabled. Aud1RxCfg.HWMuteEn = 1. This bit also defaults to 1.

2. Software informs iCEM to listen to a particular Iso channnel. This is typically done using A/V commands (Details on A/VC commands is beyond the scope of this document.). Based on the channel specified by software, the appropriate filter and mask are set. For this example, assume the channel is 32. So, software programs the filter to Iso1FltrIsoHdr.ChanNum = 0x20 and the mask to Iso1MskIsoHdr.ChanNum = 0x3F.

3. Configure the direction of the Iso buffer: Iso1Cfg.Direction = 0 for receive.

   Software ensures that the packets on the isochronous channel 32 have a FMT (format type) of 0x10. A format type of 0x10 indicates the packets are formatted according to the*1394 Trade Association Audio and Music Data Transmission Protocol 2.1*. Iso1RxCIP1.FMT should equal 0x10. If the FMT field does not equal 0x10, the software stops configuring iCEM because the packet is not an audio packet.

4. The next step is to configure the data type and HSDI mode. For this example, we are assuming the Serial IEC60958 with MLPCM is the desired data type and mode: Iso1Cfg.DataType = 0x8 and HSDI1Cfg.Mode = 0x6.

5. The received data block size (Aud1RxCfg.RxDBS) is configured next. The DBS can be determined by the DBS field in CIP0 header (IsoRx1CIP0.DBS). For an IEC60958 packet, the DBS is always 2. Software programs Aud1RxCfg.RxDBS to 0x1.

6. Software determines the sampling frequency and configure iCEM appropriately. This is done by monitoring the value SFC of the FDF field in the CIP1 header (Iso1RxCIP1.FDF). According the FDF Description Table 8, a 44.1- kHz sampling rate is a SFC value of 1’b001. For a SFC value of 1’b001, the Aud*RxCfg.VCOClkDiv should be programmed to 0x1.

7. The MLPCM interface should now be configured. For this example, the assumption is 24-bit audio, 64-fs bit clock (bclk), 256-fs master clock (mclk), and I2S as the MLPCM mode.

   - Aud1Cfg.MLPCMMode = 0x2 (I2S)
   - Aud1Cfg.Qb = 0x0 (24-bit)
   - Aud1Cfg.MLPCMSlot = 0x0 (64fs)
   - PLLCfg.Nx = 0x3 (256fs)

8. Program timestamp offset with 0x1000.

   - Iso1TmStmp.Offset = 0x001000

9. Configure the PLL interface logic. The assumption in this example is auto PLL is the desired mode instead of manual PLL mode.

   - PLLCfg.Mode = 0 (Auto PLL Mode)
   - PLLCfg.IsoDPSel = 1 (ISO Path 1 SYT used)
   - PLLCfg.SYTCompEn = 1 (Enable SYT compare)
   - PLLCfg.Enable = 1

10. Enable the audio interface (MLPCM, S/PDIF, etc…): Aud1RxCfg.OutDis = 0 and HSDI1Cfg.Enable = 1. Because the SWMute bit is still set, iCEM drives the appropriate mute pattern to the system.

11. For clock recovery, the timestamp of the packet provided by the transmit node needs to equal the current cycle timer of the receiver node before it is released from the ISO FIFO. The following two registers need to be enabled for this feature to work: Iso1TmStmp.Release = 1 and Iso1RxCfg.SYTRtrvEn = 1.

12. Enable the Iso buffer and ensure that the received packet is an IEC60958 conformant packet. The Iso buffer is enabled by programming Iso1Cfg.Enable = 1. Once the Iso buffer is enabled, software checks the value of Aud1Mntr0, Aud1Mntr1, Aud1Mntr2, and Aud1Mntr3. For an IEC60958 packet, the label field is between 0x00 and 0x3F. If the label is outside this range, please refer to the document on how to configure iCEM for a different data type like DVD audio or SACD. Keep in mind that DVD audio and SACD packets are typically encrypted. iCEM can NOT decode an encrypted packet without the proper authentication keys. Please contact TI for DTLA documentation. Recipients MUST have a signed TI NDA and be a current DTLA licensee to receive this document.

13. If the label of the received packet correctly matches an IEC60958 conformant packet, then software can remove the mute. Aud1RxCfg.SWMute = 0.

14. From this point on, software monitors for any changes in the label, sampling frequency (FDF field), format type (FMT), and data block size (DBS). If any changes occur, software mutes the audio interface until iCEM can be reconfigured.

The previous 14 steps can be summarized in the following script:

```
Aud1.Aud1RxCfg.SWMute          = 1
LLC.LinkCfg.CycMasAuto         = 1
LLC.LinkCfg.CycTmrEn           = 1
LLC.PhyCfg.LPS                 = 1
Iso1.Iso1Cfg.DataType          = 0x8
Iso1.Iso1Cfg.Direction         = 0
Iso1.Iso1RxCfg.SYTRtrvEn       = 1
Iso1.Iso1TmStmp.Release        = 1
Iso1.Iso1TmStmp.Offset         = 0x001000
Iso1.Iso1FltrIsoHdr.ChanNum    = 0x20
Iso1.Iso1MskIsoHdr.ChanNum     = 0x3F
Iso1.HSDI1Cfg.Mode             = 0x6
Aud1.Aud1Cfg.MLPCMMode         = 0x2
Aud1.Aud1Cfg.MLPCMSlot         = 0
```

Aud1.Aud1Cfg.Qb	= 0x0
Aud1.Aud1RxCfg.VCOClkDiv	= 0x1
Aud1.Aud1RxCfg.RxDBS	= 0x1
Aud1.Aud1RxCfg.HWMuteEn	= 1
Aud1.Aud1RxCfg.OutDis	= 0
PLL.PLLCfg.Nx	= 0x3
PLL.PLLCfg.SYTCompEn	= 1
PLL.PLLCfg.Mode	= 0
PLL.PLLCfg.IsoDPSel	= 1
PLL.PLLCfg.Enable	= 1
Iso1.HSDI1Cfg.Enable	= 1
Iso1.Iso1Cfg.Enable	= 1
Aud1.Aud1RxCfg.SWMute	= 0

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