TAS5132DDV2EVM

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ABSTRACT

The TAS5132V2EVM PurePath Digital™ customer evaluation module (EVM) demonstrates the integrated circuits TAS5086PAG and TAS5132DDV from Texas Instruments (TI). This application report covers the EVM specifications, audio performance and power efficiency measurements graphs, and design documentation that includes schematics, parts list, layout, and mechanical design.

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1 Introduction

The TAS5132V2EVM PurePath Digital™ customer evaluation module (EVM) demonstrates the integrated circuits TAS5086PAG and TAS5132DDV from Texas Instruments (TI).

TAS5086DBT is a high-performance, 32-bit (24-bit input) multichannel PurePath Digital™ pulse width modulator (PWM) based on Equibit™ technology with fully symmetrical AD modulation scheme. The device also has digital audio processing (DAP) that provides 48-bit signal processing, advanced performance, and a high level of system integration.

The TAS5132DDV is a high-performance, integrated stereo Digital Amplifier Power Stage designed to drive 8-Ω speakers at up to 20 W per channel. Incorporating TI's Equibit™ technology, the device is designed to be used with TI's Equibit™ modulators. This system requires only a simple passive demodulation filter to deliver high-quality, high-efficiency audio amplification. This EVM is configured with two BTL channels.

This EVM is a complete 2-channel digital audio amplifier system which includes digital input (S/PDIF), interface to PC and DAP features like digital volume control, input and output multiplexers, and bass management. The EVM is designed to demonstrate the functionality of the TAS5132DDV in a minimum component size/count scenario. Therefore, the TAS5132DDV is capable of better performance than this EVM demonstrates; however, increased performance comes at increased price.

This 2.0 system is designed for applications such as television and plasma display panels (PDP).

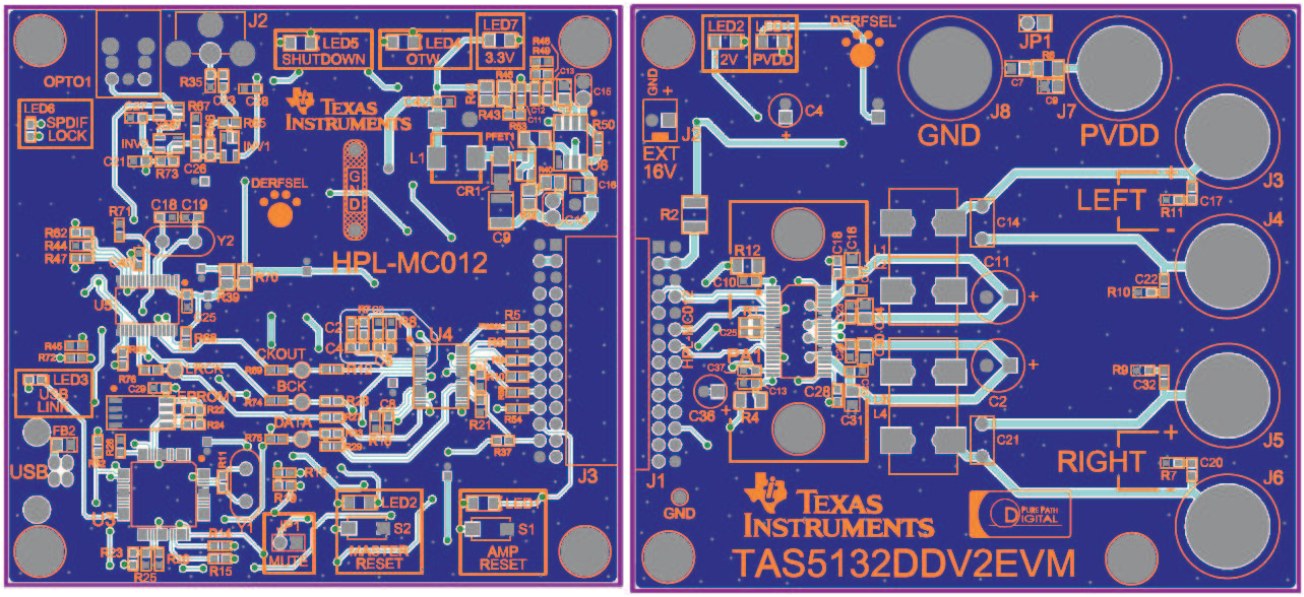


Figure 1. TAS5132DDV2EVM Evaluation Module

For EVM setup and use, see *TAS5132V2EVM User's Guide* (SLLU097).

The following sections of this document cover EVM specifications, audio performance and power efficiency measurements graphs, and design documentation that includes schematics, parts list, layout, and mechanical design.

2 TAS5132V2EVM Specification

Table 1. General Test Conditions

General Test Conditions		Notes
Output stage supply voltage: System supply voltage:	18 V	Laboratory power supply (Agilent 6574A) Derived from Output Stage Supply; GVDD = 12 V
Load impedance :	6-8 Ω	
Sampling frequency	48 kHz	
PWM processor	TAS5086DBT	
Output stage	TAS5132DDV	PG1.1
TI input-USB board	HPLMC012	Rev 1
EVM configuration file	Version 1.00	TAS5132EVM.cfg

Table 2. TAS5086 Register Settings(1)

Register	Register	Value	Notes
Modulation index limit register	0x10	0x04	Set modulation index set to 96.1%
Master volume register	0x07	0x30	Master volume set to 0 dB
Clock control register	0x00	0x6D	48-kHz sample rate; 256 FS MCLK frequency
OSC_TRIM register	0x1B	0x03	Select field trim
PWM start register	0x18	0x3F	Start channels as part of system start
Split cap charge period register	0x1A	0x00	Split-capacitor charge time = 0 ms
System control register 2	0x05	0x20	All channels started; VALID1 = VALID2

(1) These register settings are used for all test, unless otherwise specified.

Table 3. Electrical Data

Electrical Data		Notes/Conditions
Output power, BTL, 6 Ω:	18 W	1 kHz, unclipped (0 dBFS), T_A = 25°C
Output power, BTL, 6 Ω:	25 W	1 kHz, 10% THD+N, T_A = 25°C
Output power, BTL, 8 Ω:	15 W	1 kHz, unclipped (0 dBFS), T_A = 25°C
Output power, BTL, 8 Ω:	21 W	1 kHz, 10% THD+N, T_A = 25°C
Rated load impedance, BTL:	6-8 Ω	
Rated load impedance, PBTL:	3-8 Ω	
Maximum peak current, BTL:	>5 A	1-kHz burst, 3 Ω, R_{OC} = 22k
Output stage efficiency:	>90 %	2x20 W, 8 Ω
System supply current:	<110 mA	1 kHz, –60-dBFS signal, with TI input board
H-Bridge supply current:	<33 mA	1 kHz, no signal, 10-µH output inductors

Table 4. Audio Performance

Audio Performance			Notes/Conditions
THD+N, BTL, 6 Ω:	1 W	< 0.05%	1 kHz
THD+N, BTL, 6 Ω:	10 W	< 0.06%	1 kHz
THD+N, BTL, 6 Ω:	20 W	< 0.1%	1 kHz
THD+N, BTL, 8 Ω:	1 W	< 0.05%	1 kHz
THD+N, BTL, 8 Ω:	10 W	< 0.05%	1 kHz
THD+N, BTL, 8 Ω:	15 W	< 0.09%	1 kHz
Dynamic range:		> 108 dB	Reference: rated power, A-weighted, AES17 filter
Noise voltage:		< 35 μV_{rms}	A-weighted, AES17 filter

Table 4. Audio Performance (continued)

Audio Performance		Notes/Conditions
Click/pop, BTL:	< 20 mV	Mute/unmute, no input signal, 8 Ω
Channel separation	> 60 dB	1 kHz, P_{OUT} = 20 W
Frequency response:	± 2 dB	15 W/ 8 Ω, unclipped (0 dBFS)

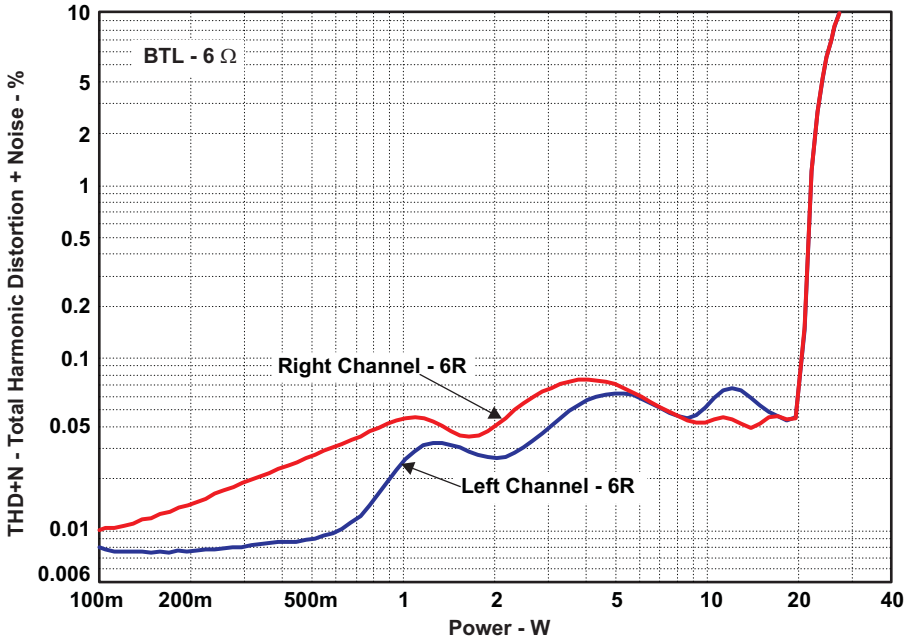
Table 5. Thermal Specification

Thermal Specification	T_{PCB} (1)	Notes/Conditions
Idle, all channels switching	<30°C	1 kHz, 15 minutes, –60-dBFS signal, T_A = 25°C
2 x 1.875 W, 8 Ω, (1/8 power)	<35°C	1 kHz, 1 hour, T_A = 25°C
2 x 15 W, 8 Ω , (full power)	<50°C	1 kHz, 5 minutes, T_A = 25°C

(1) Measured on component side of PCB, under the heat sink.

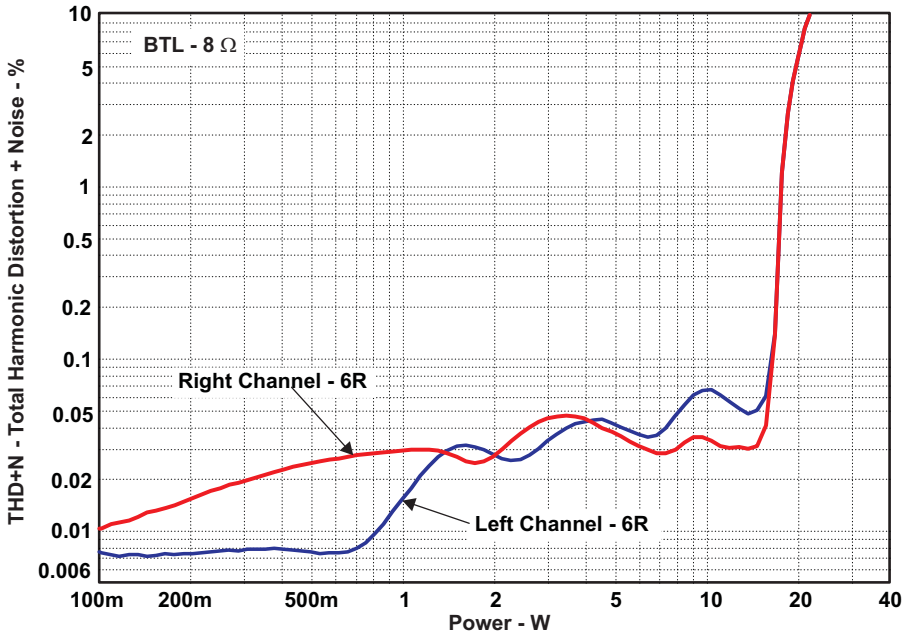
Table 6. Physical Specifications

Physical Specifications		Notes/Conditions
PCB dimensions (in mm)	200 × 100 × 25	HPLMC012-TAS5132EVMV2 total dimension
TAS5132V2EVM Amplifier Module	100 x 100 × 25	Width × length × height (mm) (power stage section = 27 mm × 50 mm)
HPL-MC012 Modulator/Controller Module Total weight	<1 kg	Components + PCB + heat sink + mechanics



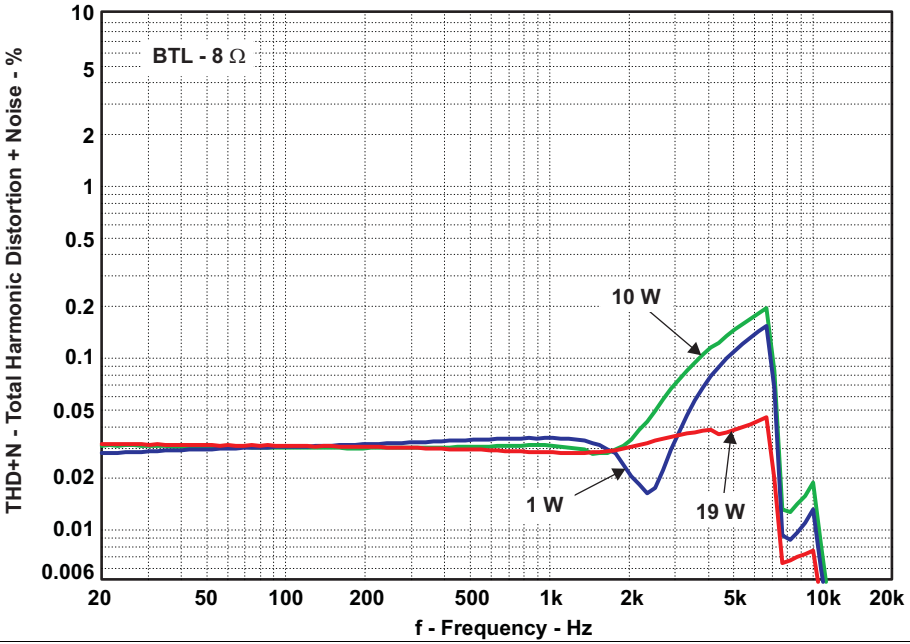
Comments:			
	Power supply: 18 Vdc	Load: 6 Ω	Filter: AES17
	Input signal: 1 kHz	+2.5-dB gain in TAS5086	Sample frequency: 48 kHz
	One trace for each channel, one channel loaded, the other muted		

Figure 2. THD+N vs Power (BTL – 6Ω)



Comments:	Power supply: 18 Vdc	Load: 8 Ω	Filter: AES17
	Input signal: 1 kHz	+2.5-dB gain in TAS5086	Sample frequency: 48 kHz
	One trace for each channel, one channel loaded, the other muted		

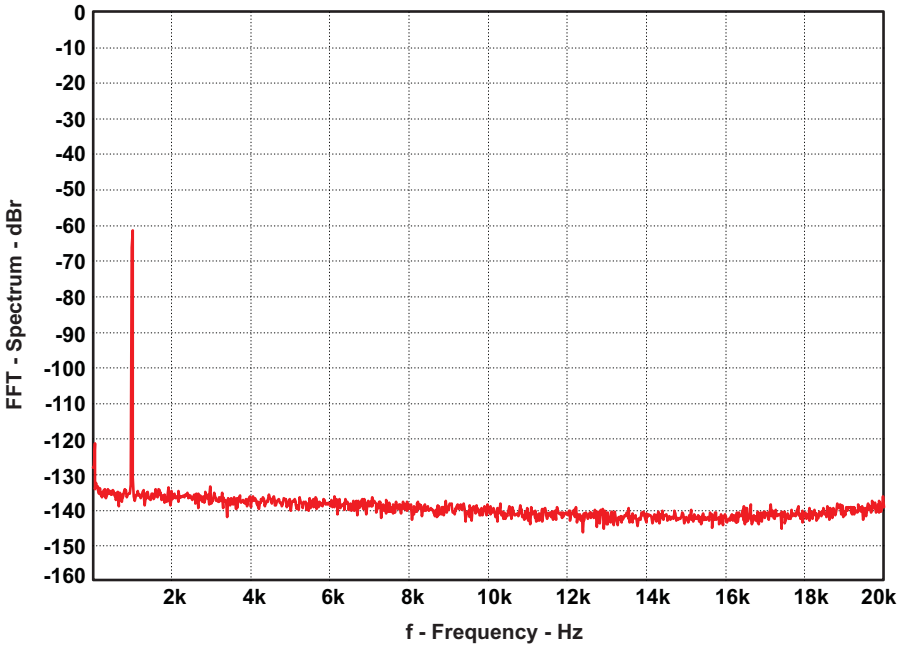
Figure 3. THD+N vs Power (BTL – 8Ω)



Comments:	Blue: 1 W	Green: 10 W	Red: 19 W	Sample frequency: 48 kHz
	Power supply: 18 Vdc	Load: 8 Ω	Filter AES17	

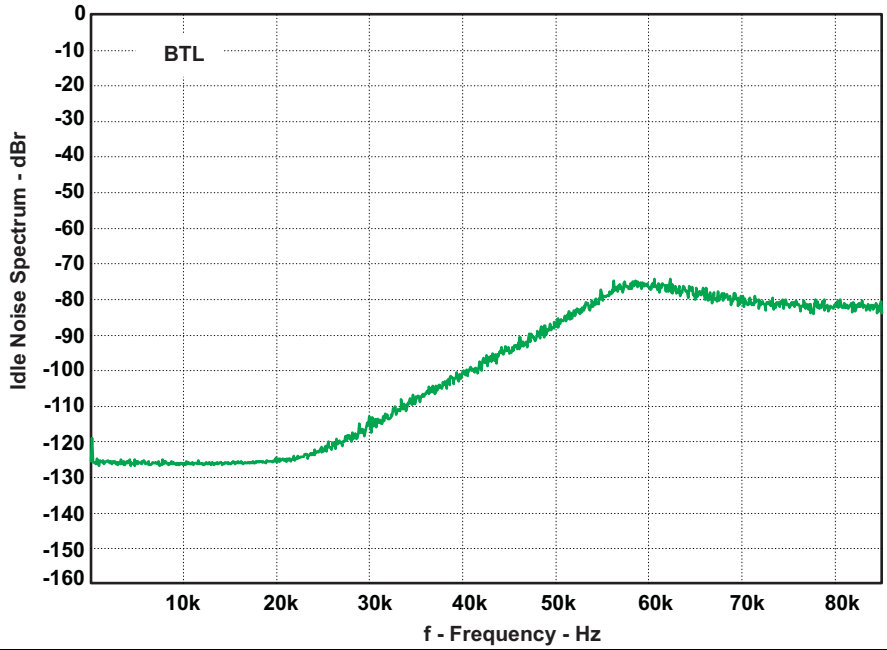
Note: THD+N at high frequencies depend on the output-filter coil material.

Figure 4. THD+N vs Frequency (BTL – 8Ω)



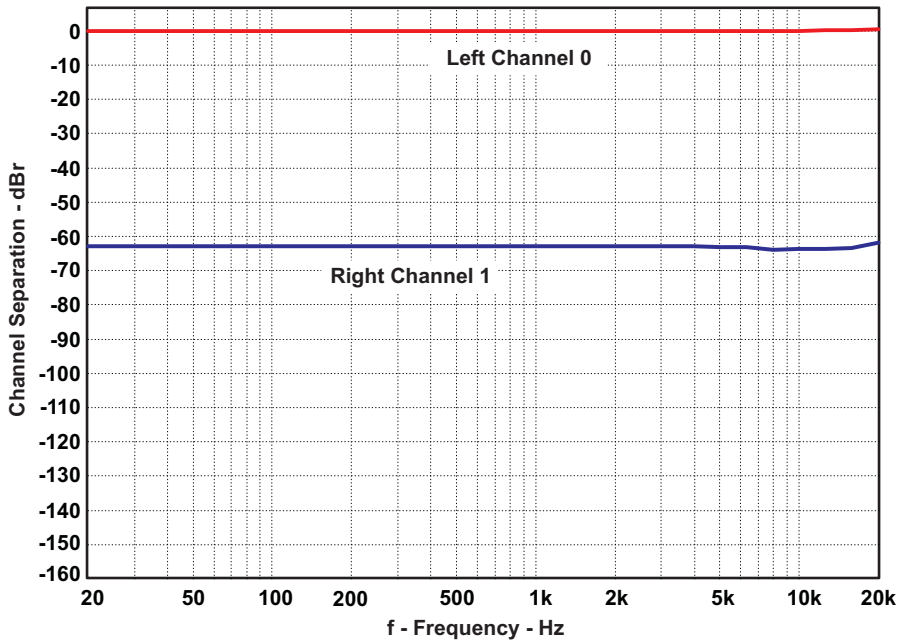
Comments:	Power supply: 18 Vdc	Load: 8 Ω	Filter: AES17	Reference: 0 dBFS
	Input signal: 1 kHz	Sample frequency: 48 kHz	FFT size: 16k	

Figure 5. FFT Spectrum With –60 dBFS Tone (BTL)



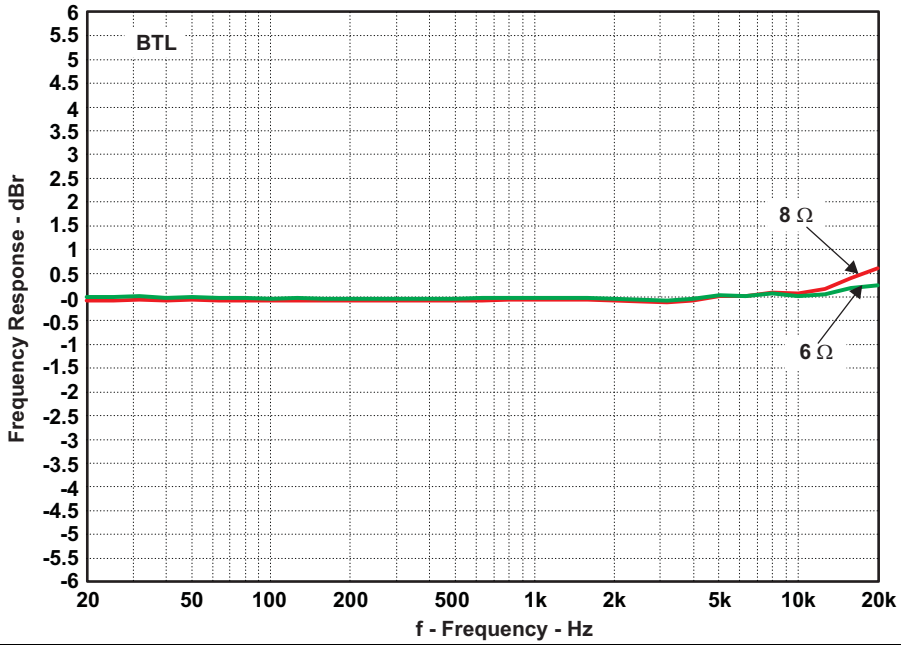
Comments:	Power supply: 18 Vdc	Load: 8 Ω	FFT size: 16k	Reference: 0 dBFS
	Input signal: Mute	Sample frequency: 48 kHz	Auto mute disabled – none	

Figure 6. Idle Noise FFT Spectrum (BTL)



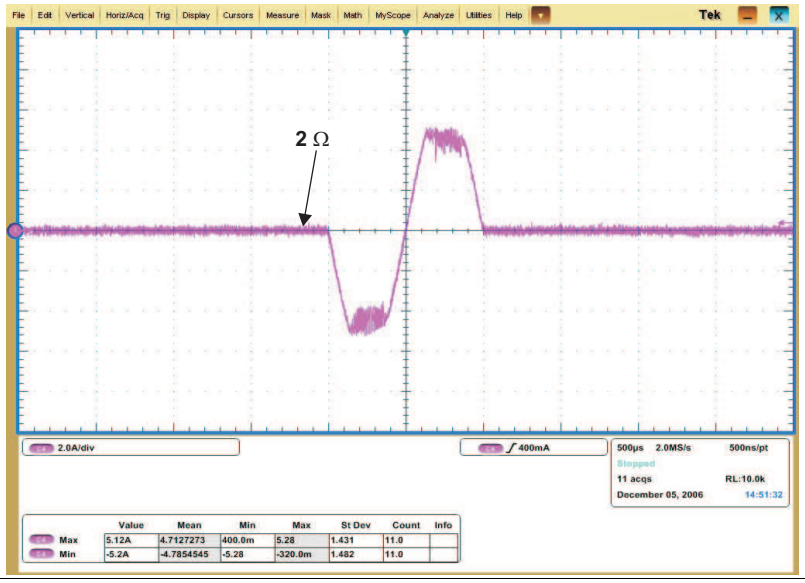
Comments:	Blue: Right Channel 1	Left Channel: 0 dB		
	Input channel 1: 0 dBFS	Load: 6 Ω		Reference: 0 dBFS
		Filter AES17	Power supply: 18 Vdc	Sample frequency: 48 kHz

Figure 7. Channel Separation



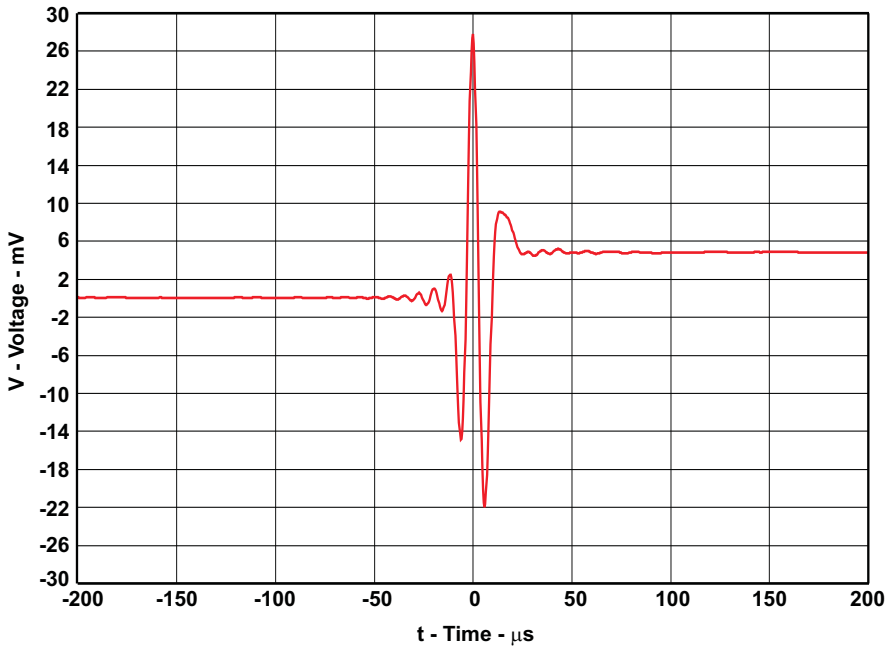
Comments:	Green: 6 Ω	Red: 8 Ω	
	Sample frequency: 48 kHz	Filter: AES17	Power supply: 18 Vdc

Figure 8. Frequency Response (BTL)



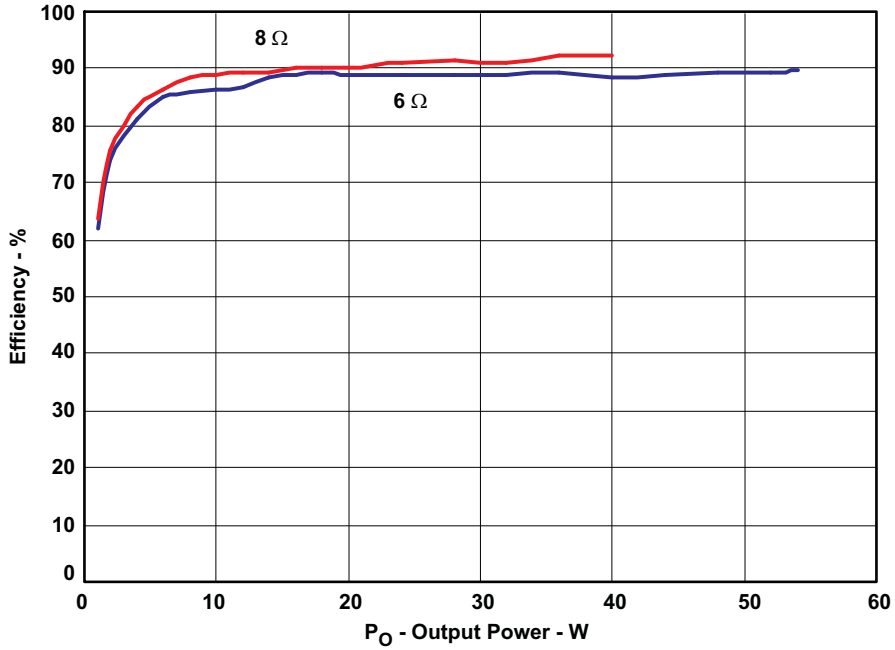
Comments:	Green: 6 Ω		
	Input signal: 1 kHz	Sample frequency: 48 kHz	Power supply: 18 Vdc

Figure 9. High-Current Protection (BTL)



Comments:	Load: 8 Ω		
	Input signal: 1 kHz	Sample frequency: 48 kHz	Power supply: 18 Vdc

Figure 10. Pop/Click (BTL)



Comments:	Stereo Power Output (BTL)		Power supply: 18 Vdc
	BTL Load: 6 Ω and 8 Ω	Sample frequency: 48 kHz	Input signal: 1 kHz

Figure 11. Output Stage Efficiency

3 Component Notes

3.1 PVDD Capacitors

The PVDD capacitors, 220 µF at 25 V were chosen to reject power supply noise and keep crosstalk below -60 dB from 20 Hz to 20 KHz. Good-quality, low-ESR capacitors should be selected to reduce the possibility of excessive noise at the amplifier's output and to keep crosstalk within the Dolby Specification of –60 dB within the audio band. These capacitors can be increased, if necessary.

3.2 Output Filter Inductors

The inductors were selected to form part of the output LC demodulation filter. They have dc resistance <50 mΩ and an inductance of 10 µH. This inductance can be increased to 16 µH to provide a lower frequency cutoff for the demodulation filter. As long as the inductance remains stable for peak current within the power band, the inductor should not present problems, as long as it provides adequate residual inductance during an output error condition to protect the amplifier (short-circuit protection).

3.3 Output Filter Capacitors

Good-quality film capacitors should be used for the 0.47-µF capacitors used in the output demodulation filter. They should have a voltage rating of not less than 2 times the PVDD supply voltage.

4 References

1. *System Design Considerations for True Digital Audio Power Amplifiers* application report (SLAA117)
2. *Digital Audio Measurements* application report (SLAA114)
3. *TAS5086: 6 Channel Digital Audio PWM Processor* data sheet (SLES131)
4. *TAS5132: Stereo Digital Amplifier Power Stage* data sheet (SLES190)
5. *PSRR for PurePath Digital Audio Amplifiers* application report (SLEA049)
6. *Power Rating in Audio Amplifier* application report (SLEA047)
7. *PurePath Digital AM Interference Avoidance* application report (SLEA040)
8. *Click & Pop Measurements Technique* application report (SLEA044)
9. *Power Supply Recommendations for DVD-Receivers* application report (SLEA027)
10. TAS5132DDV2 User's Guide (SLLU097)

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