

SN65LVDS324 Implementation Guide

Ross Eisenbeis
High Performance Analog

ABSTRACT

The SN65LVDS324 bridges the interface between high-definition video image sensors and processors. This guide describes helpful recommendations and available hardware.

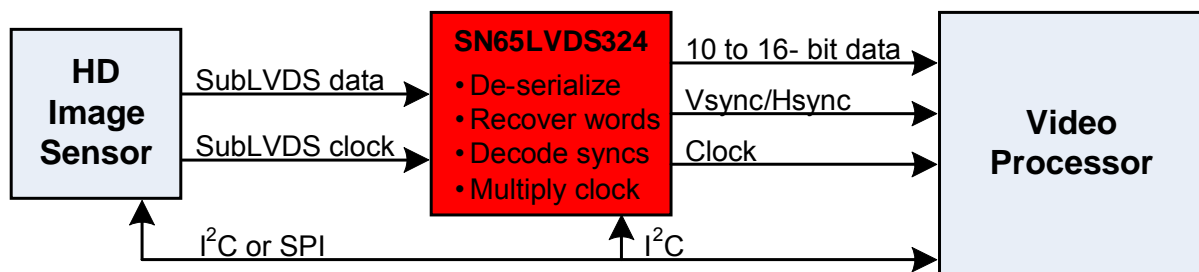


Figure 1. General block diagram

Table of Contents

- Section 1 – Compatible Image Sensors
- Section 2 – The Processor Input Voltage
- Section 3 – DaVinci™ Input Pins
- Section 4 – Layout Recommendations
- Section 5 – EVM Hardware
- Section 6 – SN65LVDS324 Configuration Registers
- Section 7 – Common Video Issues
- Section 8 – EVM Schematics

Section 1 – Compatible Image Sensors

The image sensors in this table can output SubLVDS data that's compatible with the SN65LVDS324. This is not a comprehensive list.

Aptina HiSPi Streaming-SP	Panasonic 2ch-2port	Sony LVDS Parallel
AR0331	MN34041PL	IMX136LQJ
AR0330	MN34031PL	IMX104LQJ
AR0132	MN34220PL	IMX036LQR
MT9M024	MN34210PL	IMX035LQR

Section 2 – Matching Voltages

TI has a series of DaVinci™ processors that are targeted for IP Network Cameras, including DM385, DM365, DM368, DM8127, and DMVA. They all have an Imaging Subsystem power supply (ISS) that controls the I/O voltage of the inputs that the SN65LVDS324 drives. Since the SN65LVDS324 outputs 1.8V CMOS, the ISS should be tied to 1.8V.

For DM365, DM368, DMVA1, and DMVA2, tie these ISS power pins to 1.8V:

Pin	Name
F12	VDD_ISIF_18_33
F13	VDD_ISIF_18_33

For DM385, DMVA3, and DMVA4, tie these ISS power pins to 1.8V:

Pin	Name
D12	DVDD_C
E13	DVDD_C
F12	DVDD_C
G12	DVDD_C
G13	DVDD_C

For DM8127, tie these ISS power pins to 1.8V:

Pin	Name
W19	DVDD_C
W20	DVDD_C

However, some system architectures rely on the ISS tied to 3.3V, especially if the power source is shared by other components. In that case, the SN74AVCH*T245 level shifters may be used between the SN65LVDS324 and processor, to convert the video stream from 1.8V to 3.3V. The other consideration is the control signals of I²C and RST#; when the SN65LVDS324 is used in a 3.3V system, the TXS0102 device should be used to bridge I²C voltage domains.

Generally speaking, the TI reference designs for DM385, DMVA3, and DMVA4 use 1.8V for the described signals, whereas the reference designs for DM365, DM368, DMVA1, and DMVA2, and DM8127 use 3.3V. To ease engineering development, a converter board was made that enables using 1.8V sensor boards with 3.3V systems. The converter board should be used with 3cm FFCs, to maintain signal integrity. Please contact TI if it is needed, and its schematic is in the back of this guide.

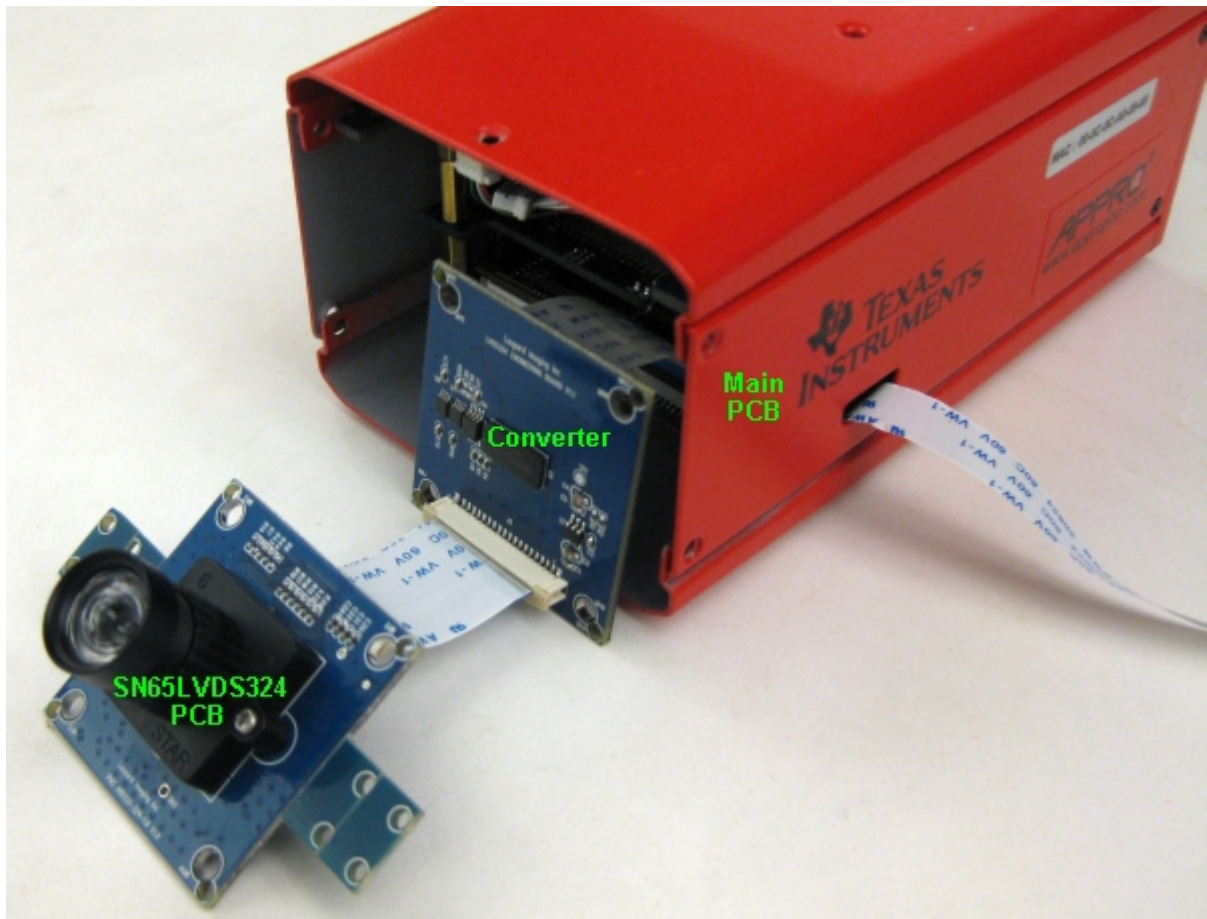


Figure 2. Engineering converter board for 3.3V systems

Section 3 – DaVinci™ Input Pins

For each processor group, these are the pins that the SN65LVDS324 drives:

	Pin	Name	Power	Description
DM365 DM368 DMVA1 DMVA2	C12	YIN7	VDD_ISIF_18_33	Standard ISIF raw[15]
	A13	YIN6	VDD_ISIF_18_33	Standard ISIF raw[14]
	B13	YIN5	VDD_ISIF_18_33	Standard ISIF raw[13]
	D12	YIN4	VDD_ISIF_18_33	Standard ISIF raw[12]
	A14	YIN3	VDD_ISIF_18_33	Standard ISIF raw[11]
	B15	YIN2	VDD_ISIF_18_33	Standard ISIF raw[10]
	D14	YIN1	VDD_ISIF_18_33	Standard ISIF raw[9]
	D15	YIN0	VDD_ISIF_18_33	Standard ISIF raw[8]
	A15	CIN7	VDD_ISIF_18_33	Standard ISIF raw[7]
	C15	CIN6	VDD_ISIF_18_33	Standard ISIF raw[6]
	B16	CIN5	VDD_ISIF_18_33	Standard ISIF raw[5]
	A16	CIN4	VDD_ISIF_18_33	Standard ISIF raw[4]
	A17	CIN3	VDD_ISIF_18_33	Standard ISIF raw[3]
	C16	CIN2	VDD_ISIF_18_33	Standard ISIF raw[2]
	A18	CIN1	VDD_ISIF_18_33	Standard ISIF raw[1]
	B17	CIN0	VDD_ISIF_18_33	Standard ISIF raw[0]
	C14	HD	VDD_ISIF_18_33	Horizontal Sync
	B14	VD	VDD_ISIF_18_33	Vertical Sync
D13	PCLK	VDD_ISIF_18_33	Pixel Clock	

	Pin	Name	Power	Description
DM385 DMVA3 DMVA4	C2	CAM_D[0]	DVDD_C	Standard ISIF raw[15]
	C1	CAM_D[1]	DVDD_C	Standard ISIF raw[14]
	B2	CAM_D[2]	DVDD_C	Standard ISIF raw[13]
	A2	CAM_D[3]	DVDD_C	Standard ISIF raw[12]
	A3	CAM_D[4]	DVDD_C	Standard ISIF raw[11]
	J13	CAM_D[5]	DVDD_C	Standard ISIF raw[10]
	C5	CAM_D[6]	DVDD_C	Standard ISIF raw[9]
	C12	CAM_D[7]	DVDD_C	Standard ISIF raw[8]
	K11	CAM_D[8]	DVDD_C	Standard ISIF raw[7]
	E12	CAM_D[9]	DVDD_C	Standard ISIF raw[6]
	K10	CAM_D[10]	DVDD_C	Standard ISIF raw[5]
	D7	CAM_D[11]	DVDD_C	Standard ISIF raw[4]
	F9	CAM_D[12]	DVDD_C	Standard ISIF raw[3]
	C7	CAM_D[13]	DVDD_C	Standard ISIF raw[2]
	A6	CAM_D[14]	DVDD_C	Standard ISIF raw[1]
	A5	CAM_D[15]	DVDD_C	Standard ISIF raw[0]
	D5	CAM_HS	DVDD_C	Horizontal Sync
	H9	CAM_VS	DVDD_C	Vertical Sync
B3	CAM_PCLK	DVDD_C	Pixel Clock	

	Pin	Name	Power	Description
DM8127	AA22	CAM_D[0]	DVDD_C	Standard ISIF raw[15]
	AC19	CAM_D[1]	DVDD_C	Standard ISIF raw[14]
	AC18	CAM_D[2]	DVDD_C	Standard ISIF raw[13]
	AD18	CAM_D[3]	DVDD_C	Standard ISIF raw[12]
	AD17	CAM_D[4]	DVDD_C	Standard ISIF raw[11]
	AC22	CAM_D[5]	DVDD_C	Standard ISIF raw[10]
	AC15	CAM_D[6]	DVDD_C	Standard ISIF raw[9]
	AB17	CAM_D[7]	DVDD_C	Standard ISIF raw[8]
	AA21	CAM_D[8]	DVDD_C	Standard ISIF raw[7]
	AB21	CAM_D[9]	DVDD_C	Standard ISIF raw[6]
	AF20	CAM_D[10]	DVDD_C	Standard ISIF raw[5]
	AF21	CAM_D[11]	DVDD_C	Standard ISIF raw[4]
	AC17	CAM_D[12]	DVDD_C	Standard ISIF raw[3]
	AE18	CAM_D[13]	DVDD_C	Standard ISIF raw[2]
	AC21	CAM_D[14]	DVDD_C	Standard ISIF raw[1]
	AC16	CAM_D[15]	DVDD_C	Standard ISIF raw[0]
		D5	CAM_HS	DVDD_C
	H9	CAM_VS	DVDD_C	Vertical Sync
	AF18	CAM_PCLK	DVDD_C	Pixel Clock

Section 4 – Layout Recommendations

For power supply filtering, it's recommended to use at least two 100nF and two 10nF ceramic capacitors. Depending on the amount of power noise in the system, it can also be beneficial to isolate the VCCA node from the 1.8V board plane through a ferrite bead—then place at least one 100nF and 10nF on the isolated node.

The SN65LVDS324 should be placed closely to the processor, to minimize CMOS trace length and EMI. The image sensor output of SubLVDS is well-suited for distance transmission (>0.5 meters is generally expected; the bitrate and medium are significant variables). Note that the TI IPNC reference designs don't use optimal placement, since the SN65LVDS324 is on the Sensor PCB rather than the Main PCB.

Single-ended CMOS signaling can cause significant EMI. This applies to the path between the SN65LVDS324 and the processor. Here are several ways to control it:

1. Minimize the trace/cable distance.
2. Use extra spacing or GND guard traces to isolate signals from the parallel video bus.
3. Set the SN65LVDS324 to use a slower data slew rate with register 0x0A[5:4]. Reducing edge rates reduces coupling.
4. Add an RC low-pass filter on CLKOUT near the SN65LVDS324. Slowing clock edges greatly reduces EMI.
5. Follow these PCB design practices: <http://focus.ti.com/lit/an/szza009/szza009.pdf>.

The SN65LVDS324 parallel output should be trace-length matched with respect to the clock, to within 1cm (400mils). Mismatched lengths cause skew, which reduces setup/hold time.

Reset (pin RST#) must transition Low-to-High at least 30µs after VCC is High and stable. Adding an external capacitor can achieve this, since it creates an RC-filter from the internal 1.8V rail through the internal 150kΩ resistor. For instance, a 100nF capacitor should ideally delay the RST# rise time by 21ms. Alternatively, RST# can be externally controlled by a processor.

TI IPNC reference designs interface the Sensor PCB with the Main PCB using a Flat Flexible Cable (FFC) and 36-pin MOLEX connector **52559-3652**. Some documents list 52559-3679 instead, which is functionally the same but less available. The blue side of the FFC faces the curved side of the connector.

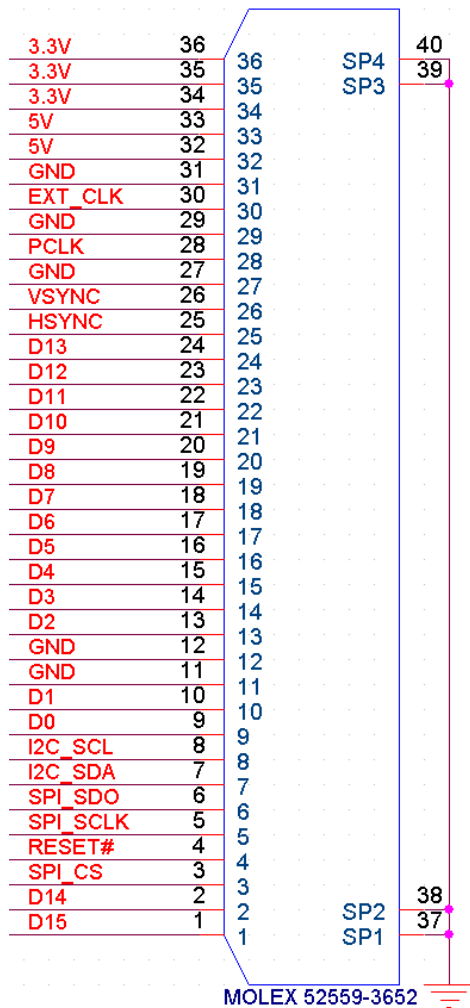


Figure 3. Sensor Board side

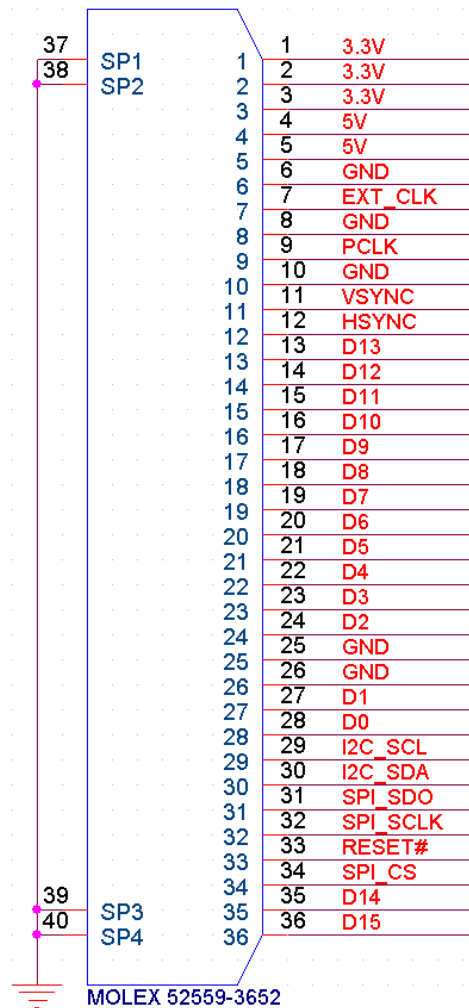


Figure 4. Main Board side

Section 5 – EVM Hardware

Boards are available that contain the SN65LVDS324 and different image sensors. Schematics of those with the Aptina AR0331, Panasonic MN34041, and Sony IMX136 can be found in the back section of this guide. These boards are part of the DaVinci DM385 reference design. The reference camera system can be purchased from Appro Photoelectron Inc. at <http://www.ApproPho.com/> and the individual boards can be purchased from Leopard Imaging at these links:

Aptina AR0331 - <http://shop.leopardimaging.com/product.sc?productId=85&categoryId=17>

Panasonic MN34041 - <http://shop.leopardimaging.com/product.sc?productId=87&categoryId=17>

Sony IMX104 - <http://shop.leopardimaging.com/product.sc?productId=83&categoryId=17>

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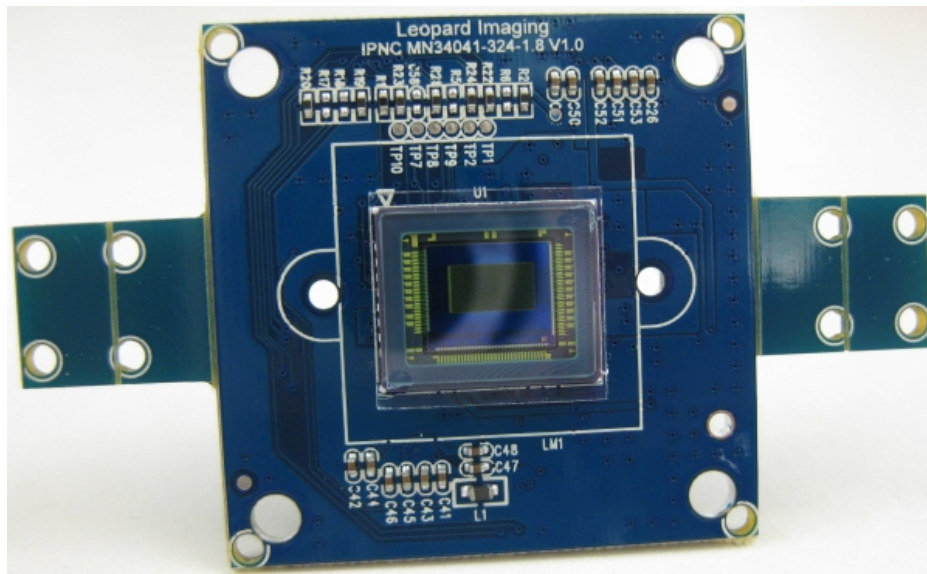


Figure 5. EVM front (without lens)

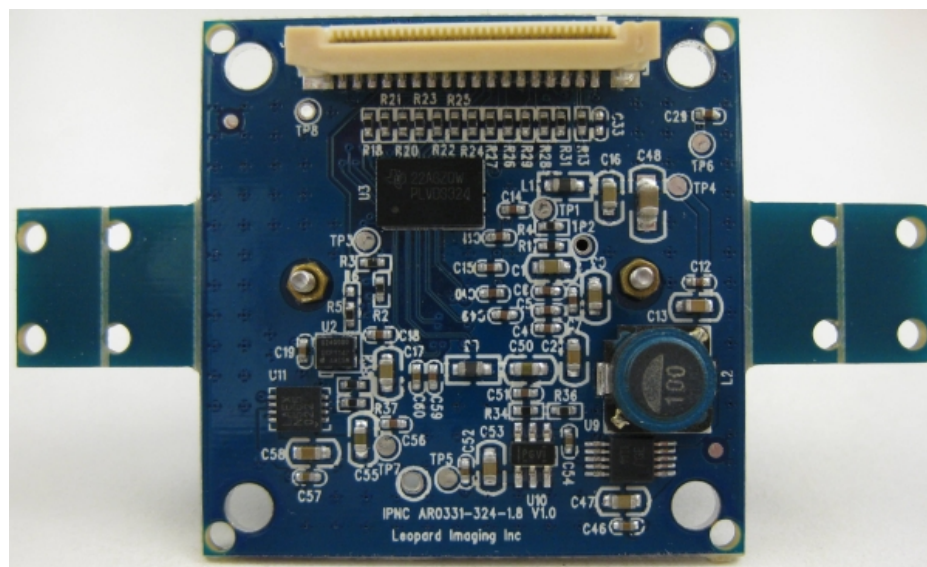


Figure 6. EVM backside

Some SN65LVDS324 applications could involve a platform that doesn't have the 36-pin MOLEX interface. For these, a breakout board was created to provide easy access to each EVM signal. Please contact TI if this is needed.



Figure 7. Breakout Board

Section 6 – SN65LVDS324 Configuration Registers

The SN65LVDS324 is configurable through I²C. Only 6 of the registers must be programmed; they are LSB_FIRST_OUTPUT, SYNC_ACTIVE_HIGH, CLK_CENTERED_TIMING, SENSOR_CFG, VCM_MODE, and PLL_CFG. CLK_CENTERED_TIMING “0” was intended for DaVinci™, while “1” was intended for OMAP™.

An I²C calculator program was created to help determine register values to program. For a general idea of typical values, when the Aptina AR0331 is used at 1080p60, 12bpp, and SLVS mode, consider writing address 0x09 = 0x24, and 0x0A = 0x22. When the Panasonic MN34041 is used at 1080p60 and 12bpp, consider writing address 0x09 = 0x12, and 0x0A = 0x62.



Figure 8. I²C calculator program

TESTMODE_VIDEO can be useful for debug, to help distinguish between a sensor problem versus processor problem. With a clock applied to pin SCLK, the SN65LVDS324 will generate parallel video data using your specified frame size. This data is a RAW Bayer Mosaic format, just like in normal operation with a sensor, where each clock period represents red, green, or blue. If during debug, there's an image problem using a real sensor, while the testmode produces a good image, that suggests the problem lies between the sensor and LVDS324, or there may be a sensor configuration problem.



Figure 9. Testmode pattern

Section 7 – Common Video Issues

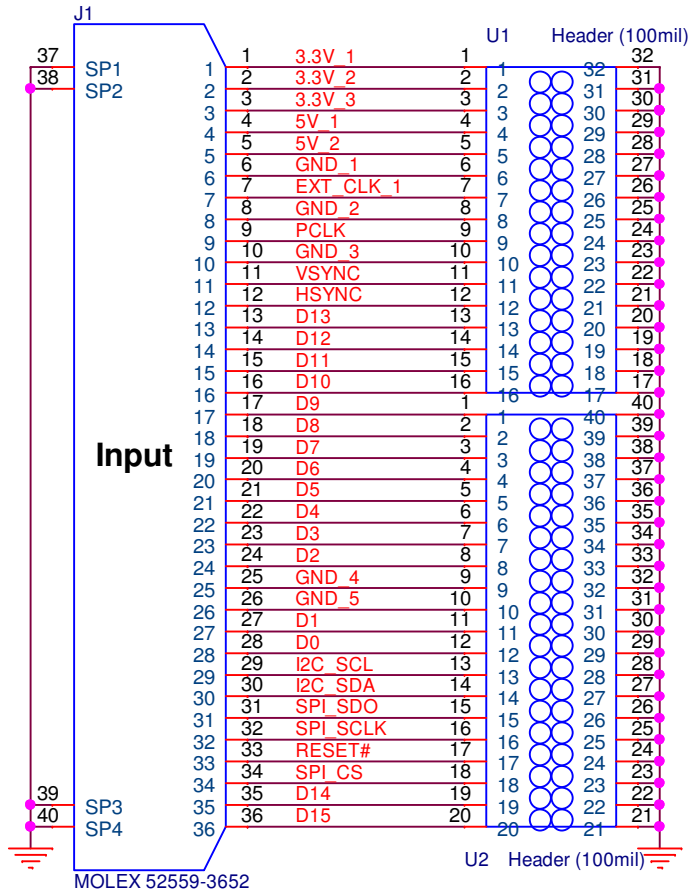
Problem	Cause	Solution
Video is saturated with purple.	The polarity convention of Vsync and Hsync is swapped.	Change SN65LVDS324 register SYNC_ACTIVE_HIGH to “0”.
Video is extremely dark.	The camera is set to use 2A Engine “Appro”.	Use ActiveX to login, go to menu “Camera”, and change the 2A Engine to “TI”.
Video is 100% multicolor random noise.	The parallel output has MSB/LSB-first swapped.	Change SN65LVDS324 register LSB_FIRST_OUTPUT.
Video works, but certain colors have noise.	The processor is programmed to latch video data on the <i>falling</i> clock edge.	Change the software so that the processor latches on the <i>rising</i> clock edge.
Video through Internet Explorer ActiveX is laggy.	ActiveX can have a hard time keeping up with 1080p60.	It can improve if you click “Video”, set the framerate to 15, click OK, set the framerate to 60, and click OK. Or use the camera’s HDMI output instead.
Video stops, and the log gives error “AE write to sensor failed” or “I2C Arbitration lost”.	The I ² C has insufficient signal integrity.	Reduce the FFC length, use a slower SN65LVDS324 data slew rate for less crosstalk (register D_SLEW_RATE), or add capacitance to I ² C signals to filter noise.
I ² C reads return nothing.	There are several possibilities.	Verify I ² C signals are connected, verify pull-up resistors are present, verify RST# is High, and verify RST# went High after VCC went High.

Section 8 – EVM Schematics

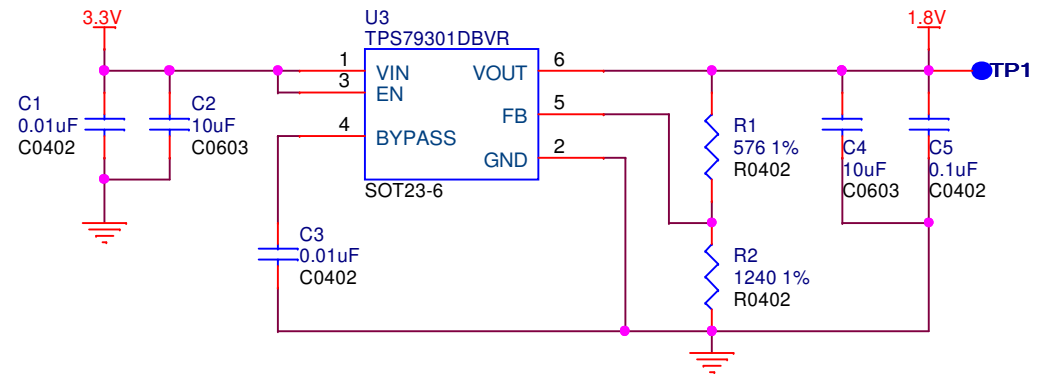
The next 2 pages: Breakout Board and Engineering Converter Board

MH1 MH2 MH3 MH4 MH5 MH6 MH7 MH8
 MHOLE-2M MHOLE-2M MHOLE-2M MHOLE-2M MHOLE-3M MHOLE-3M MHOLE-3M MHOLE-3M
 MHOLE-2M MHOLE-2M MHOLE-2M MHOLE-2M MHOLE-3M MHOLE-3M MHOLE-3M MHOLE-3M

FFC Breakout

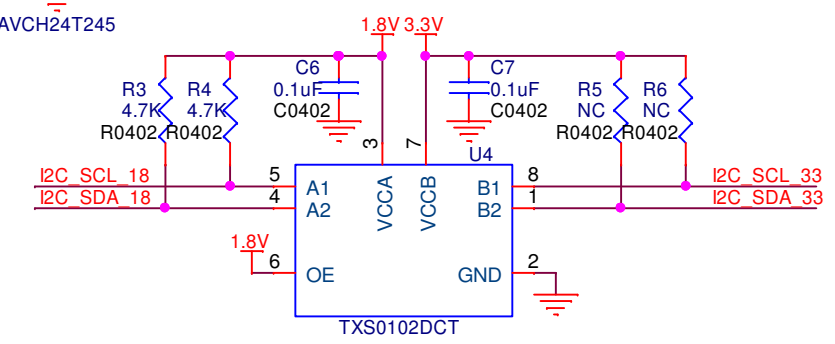
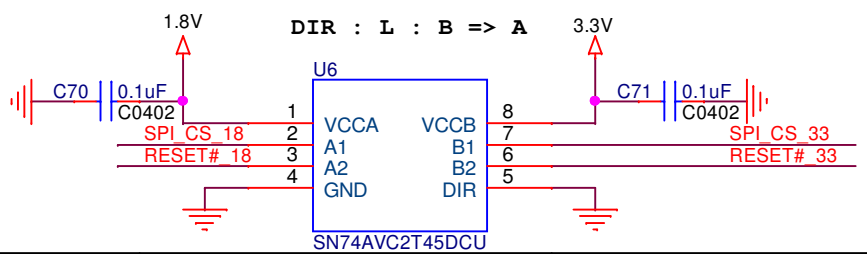
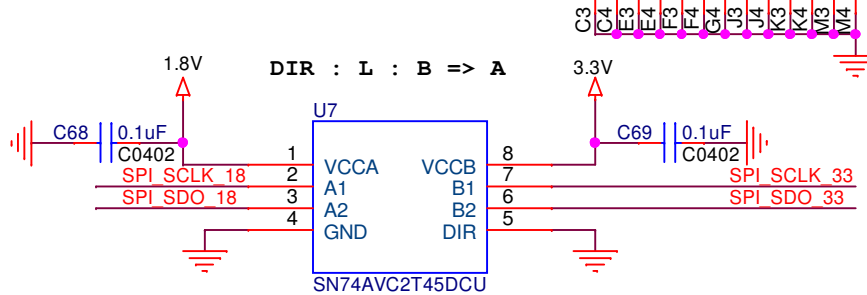
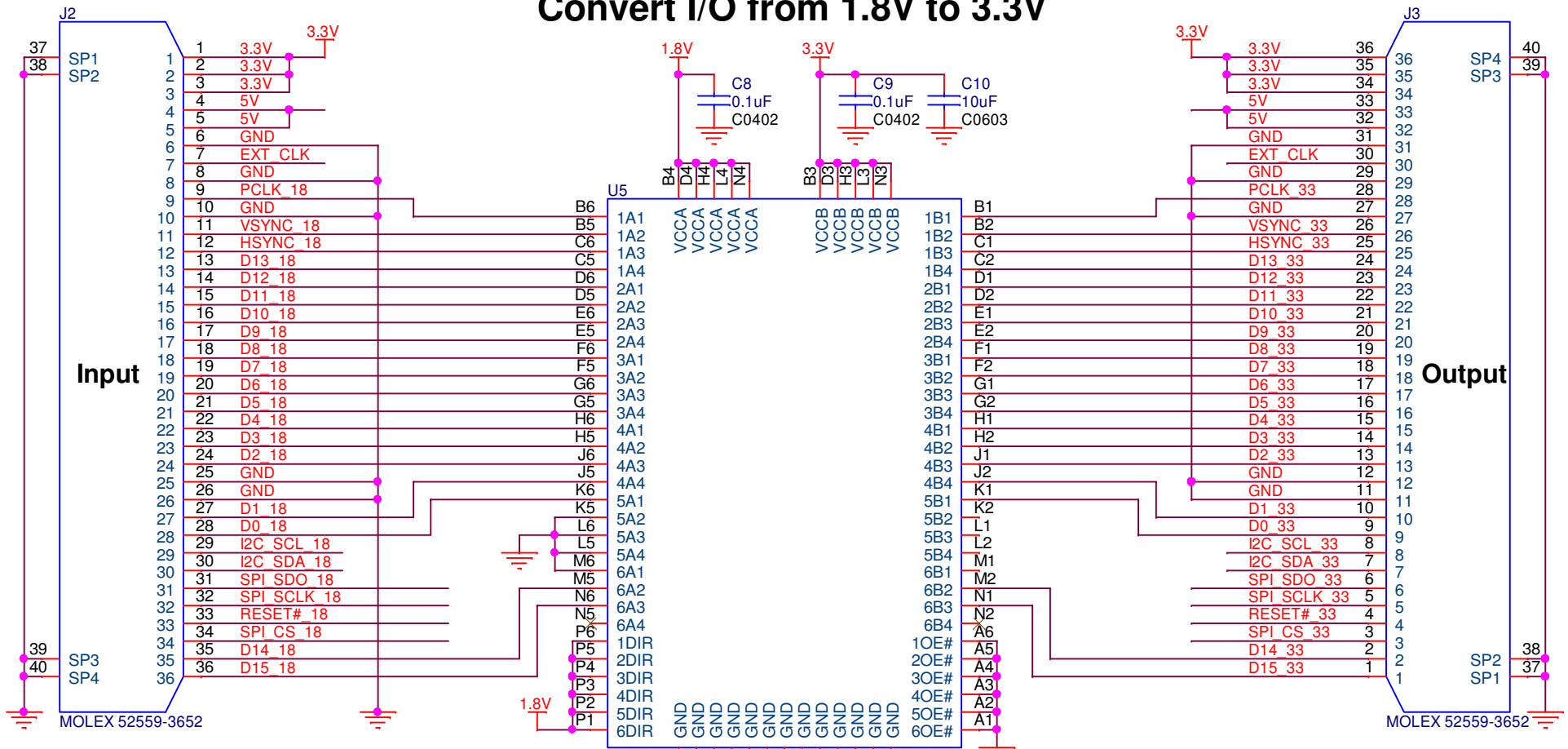


Regulate 3.3V to 1.8V



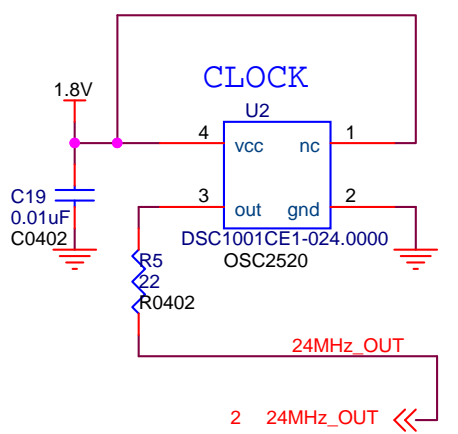
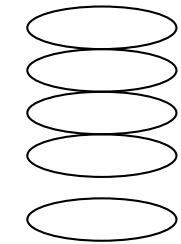
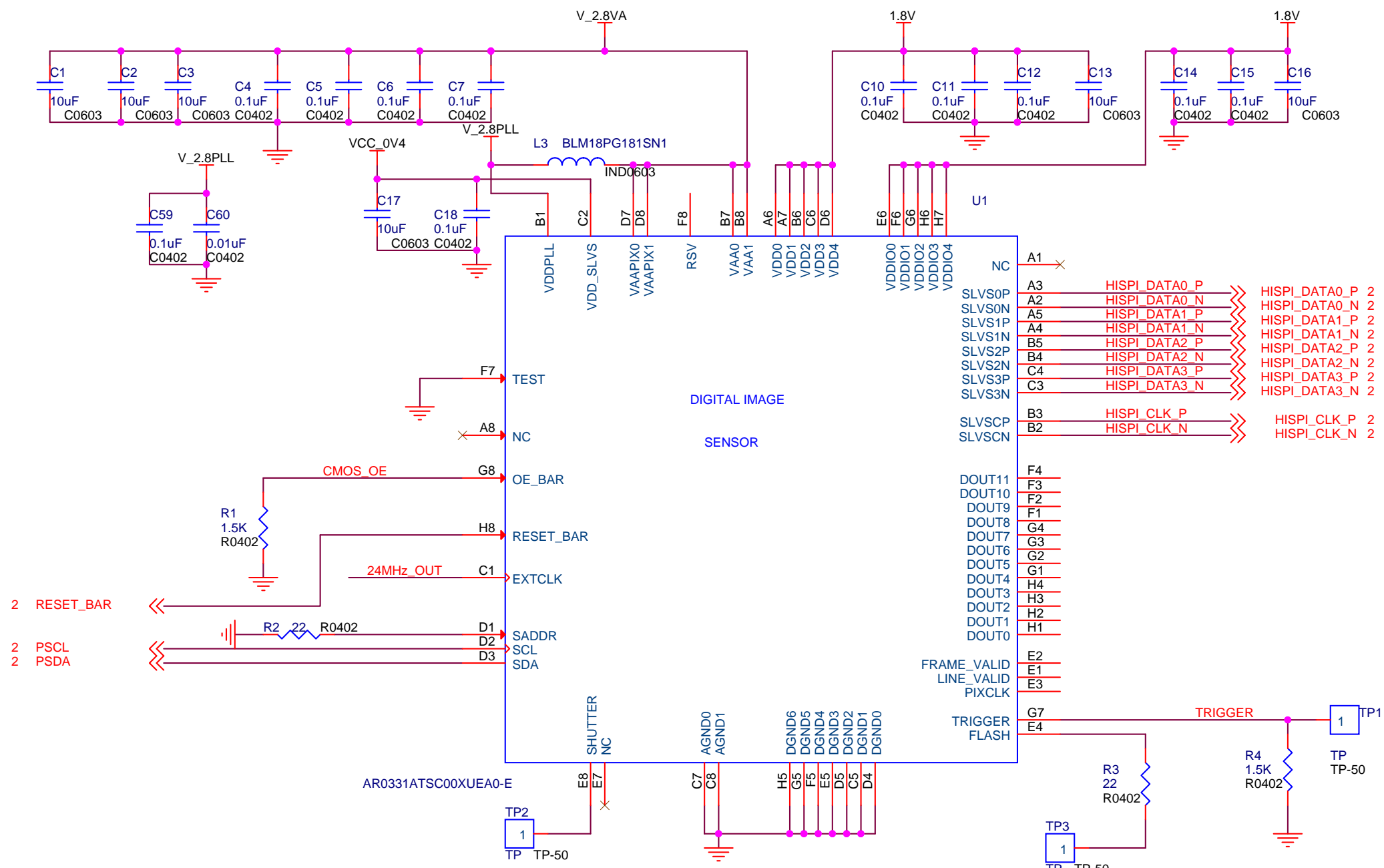
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Convert I/O from 1.8V to 3.3V

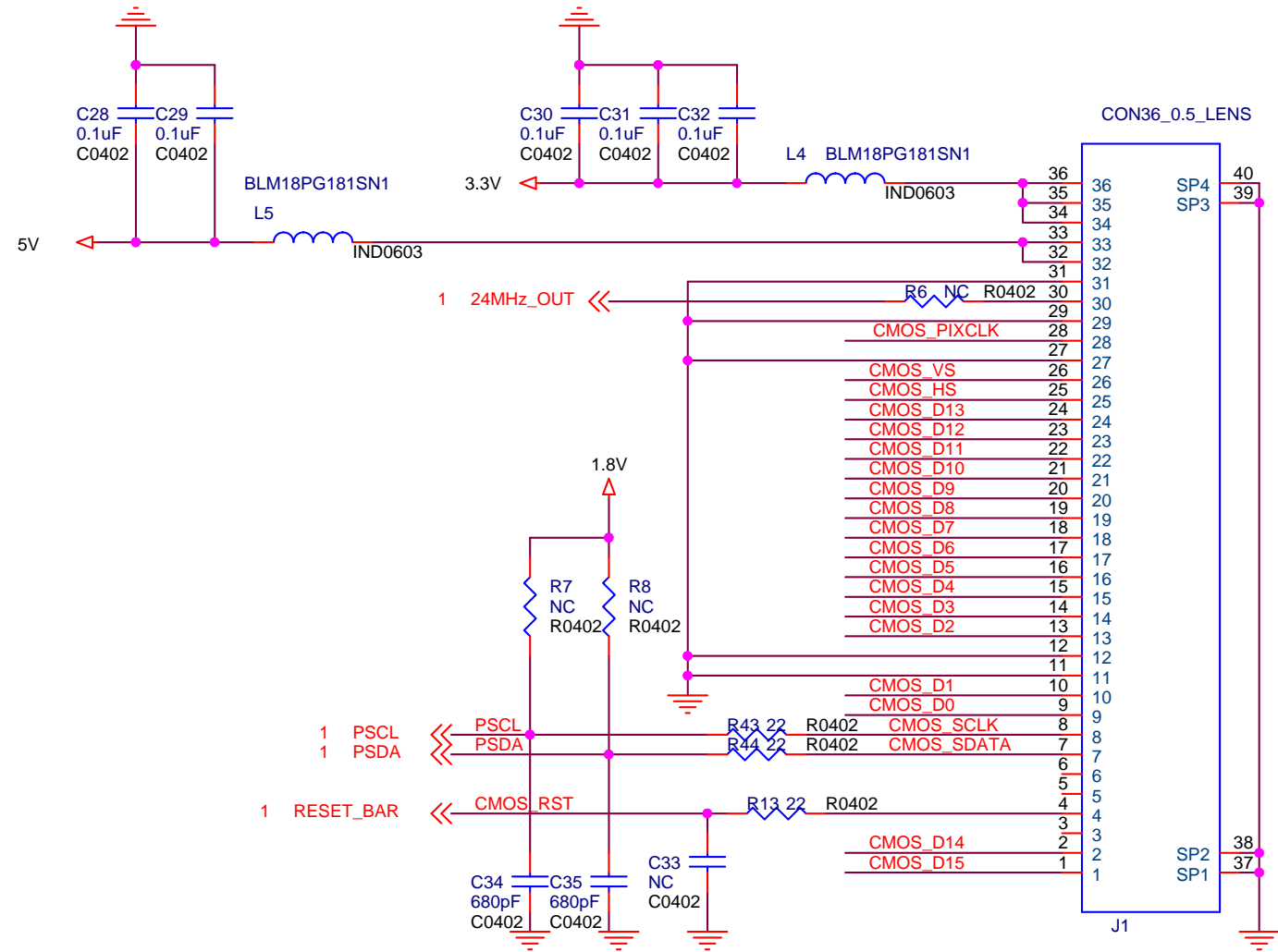
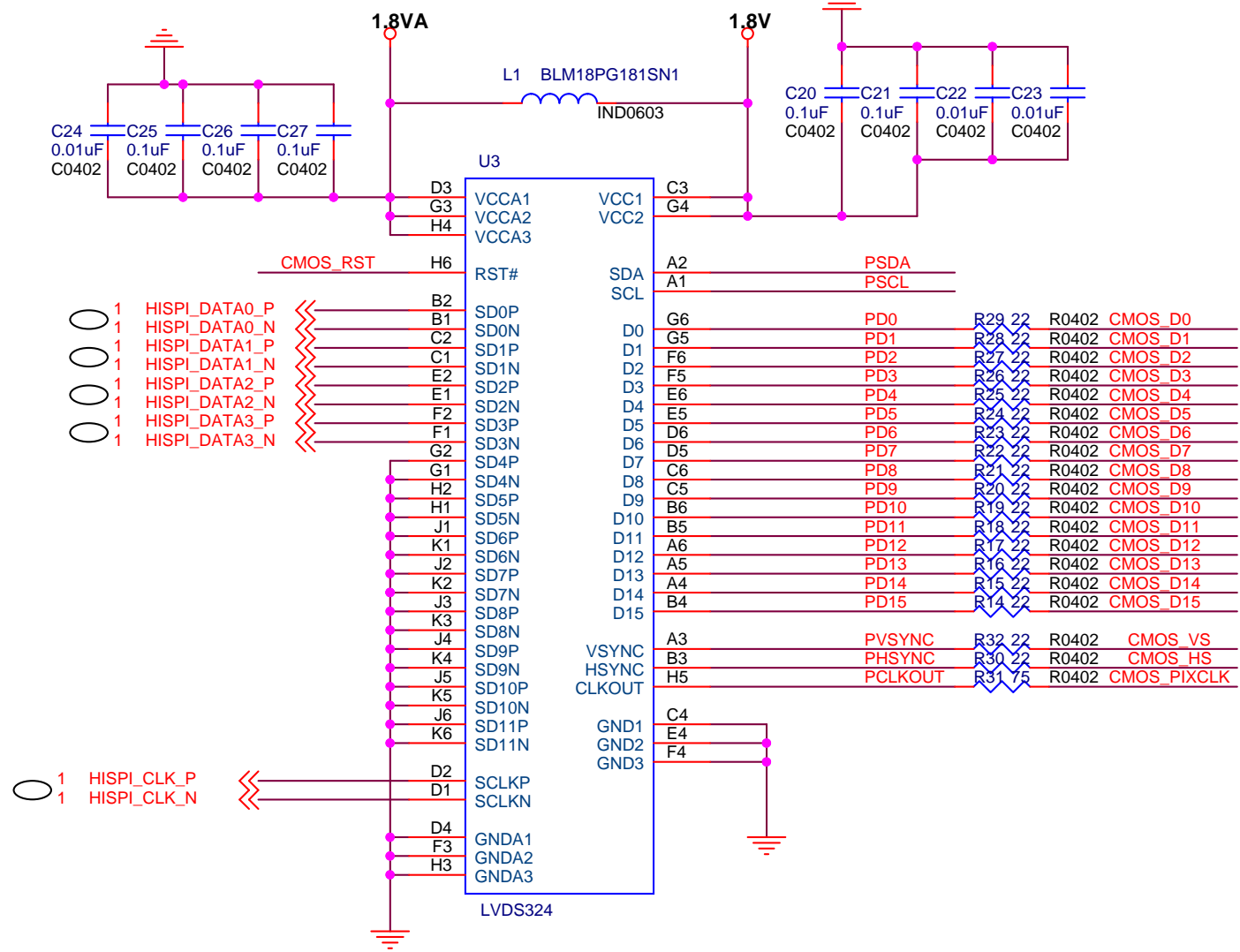


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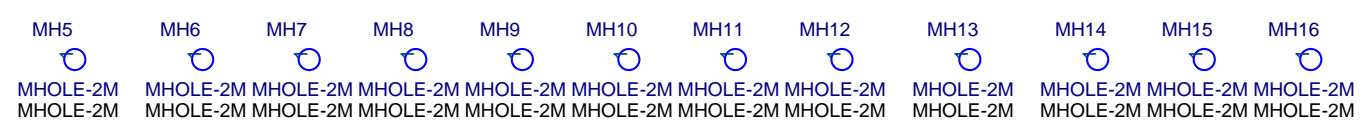
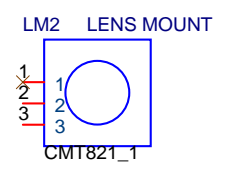
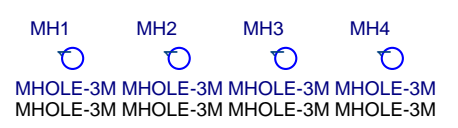
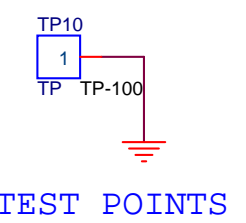
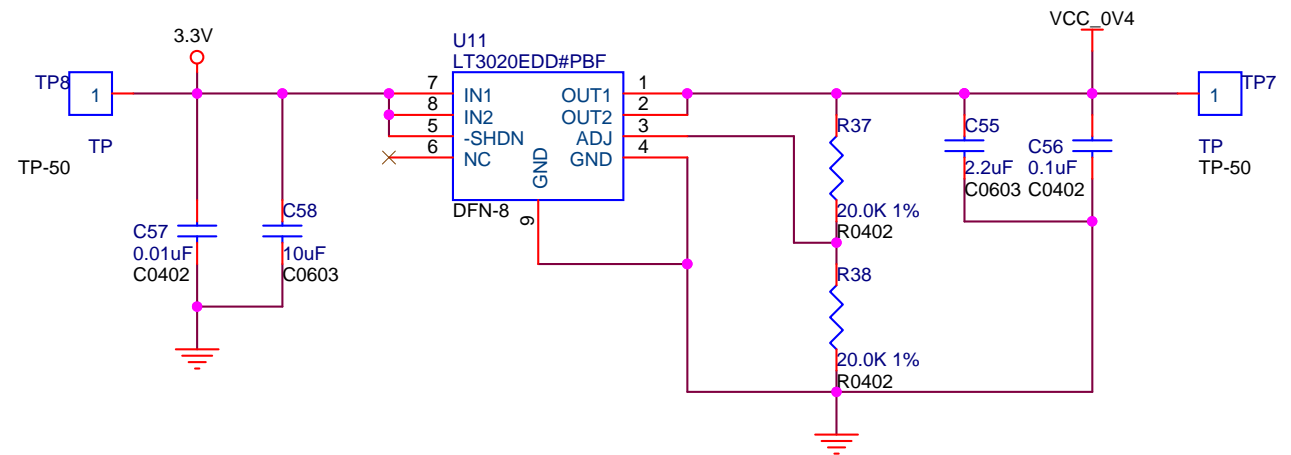
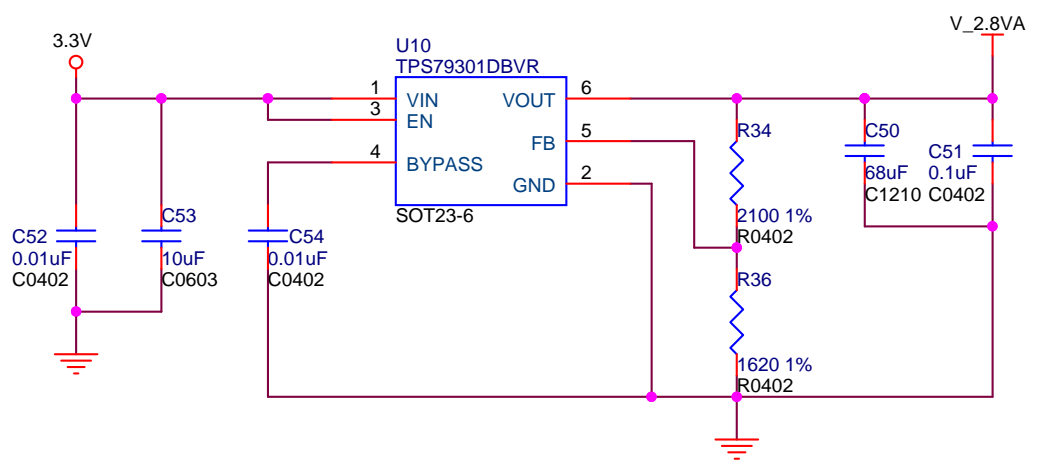
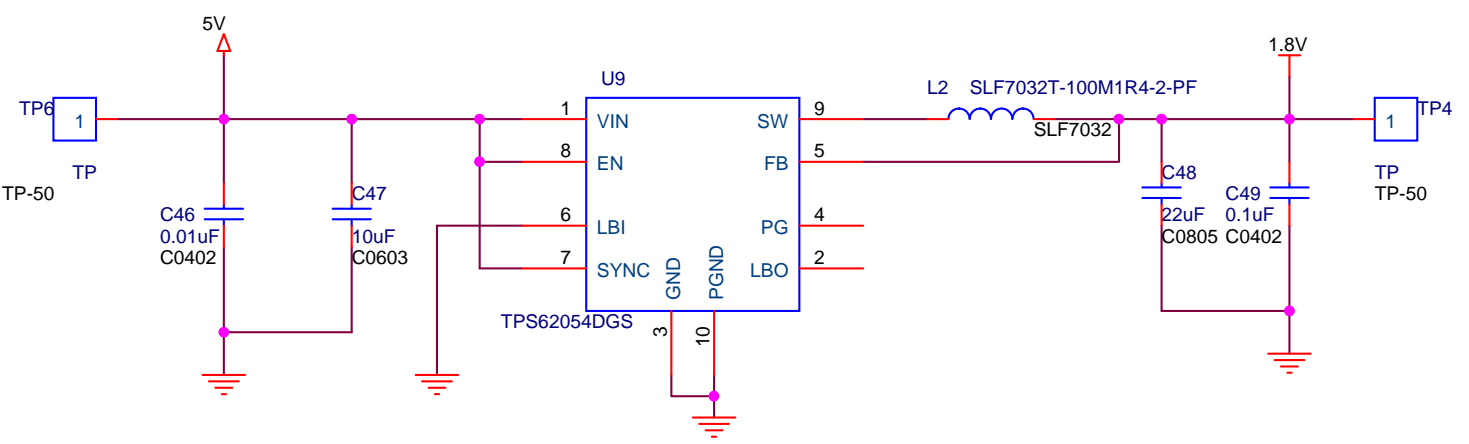
The next 3 pages: EVM with the AR0331



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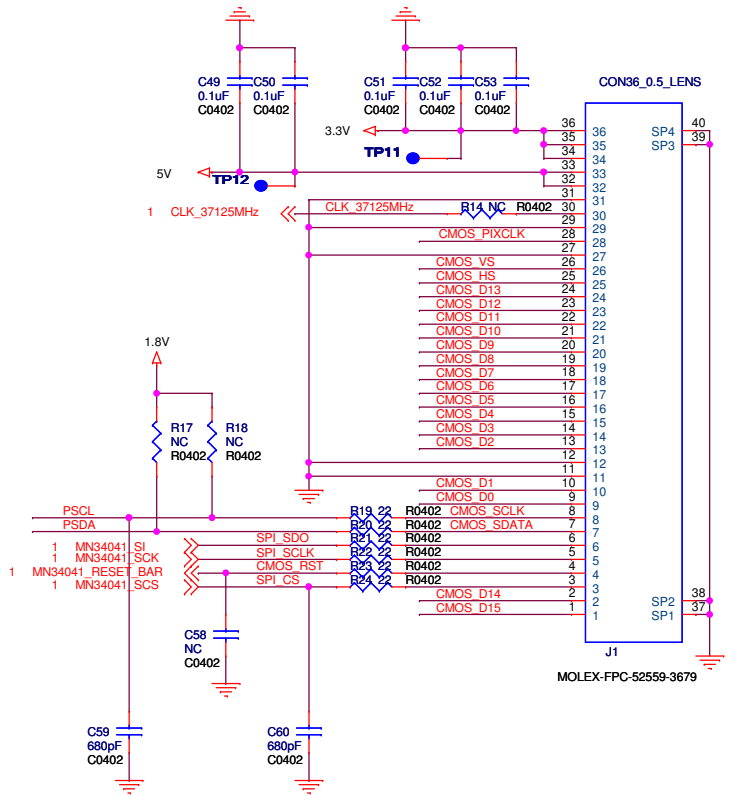
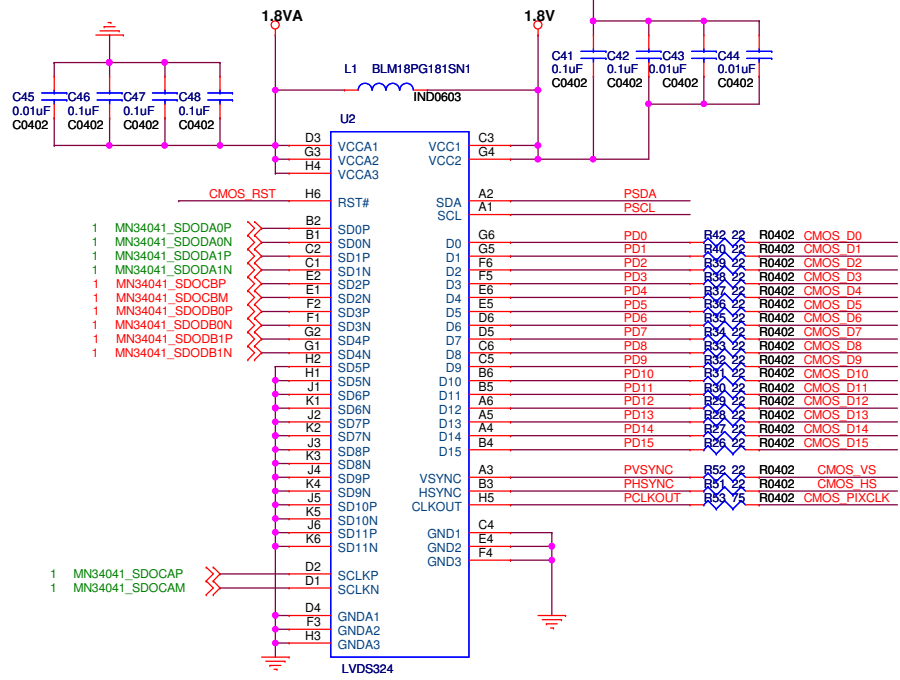


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		G2	SD4P	D7	PD8	R21 22	R0402	CMOS_D8
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		J5	SD10P					
		K6	SD10N					
		J6	SD11P					
		K6	SD11N					
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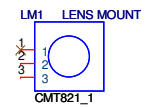
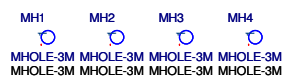
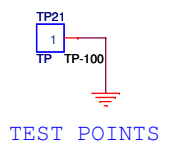
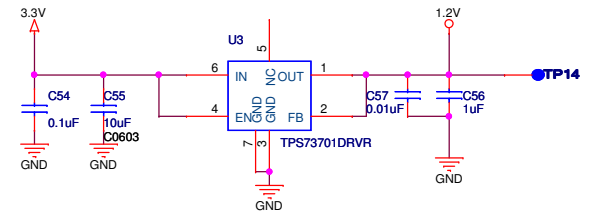
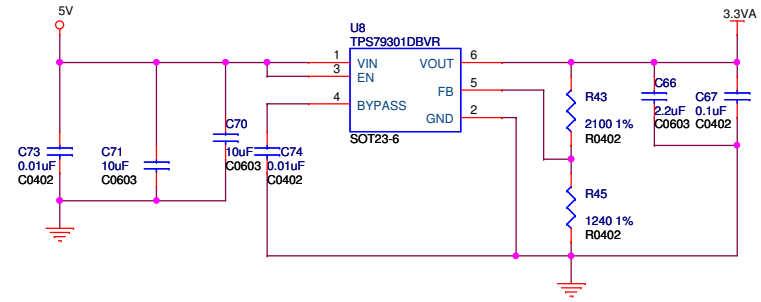
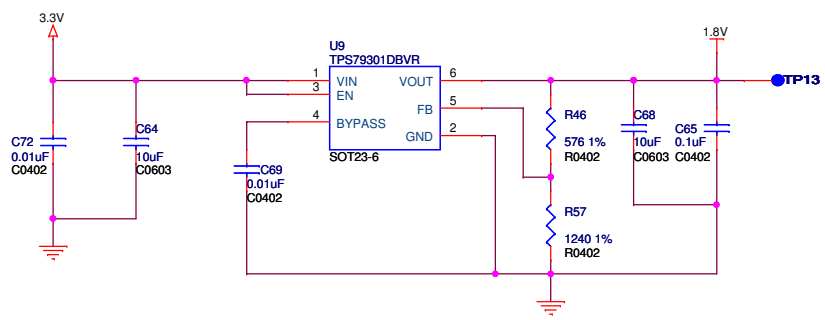


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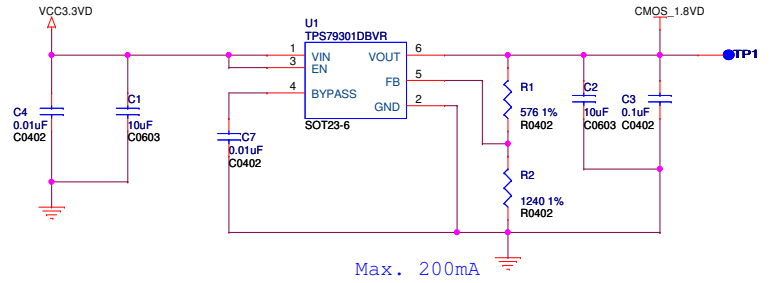
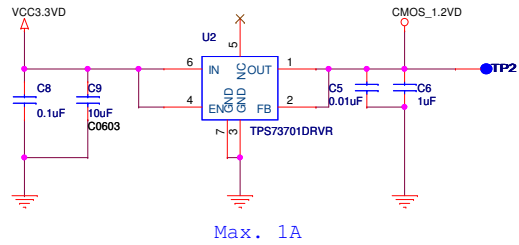
Title			MN34041-324-1.8 CAMERA BOARD
Size	Document Number	Power Regulator	
B			Rev 1.1
Date:	Wednesday, July 18, 2012	Sheet	3 of 3

The next 2 pages: EVM with the IMX136

MH1 MH2 MH3 MH4
MHOLE-2M MHOLE-2M MHOLE-2M MHOLE-2M
MHOLE-2M MHOLE-2M MHOLE-2M MHOLE-2M

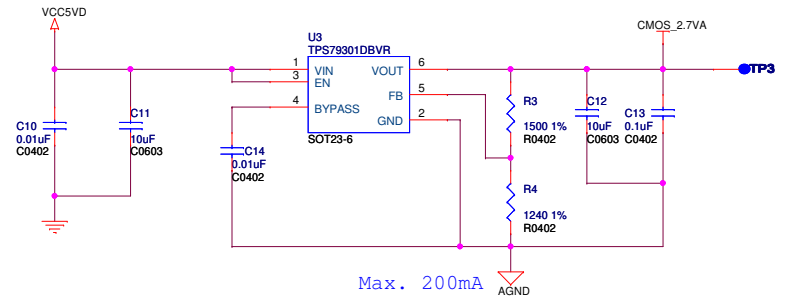
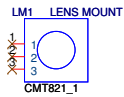
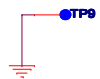
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MH10 MH11 MH12
MHOLE-2M MHOLE-2M MHOLE-2M
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FDC1 FDC2 FDC3 FDC4
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MH13 MH14 MH15 MH16
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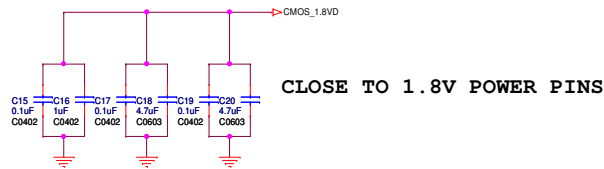


TEST POINTS

IMX104 Camera Board:

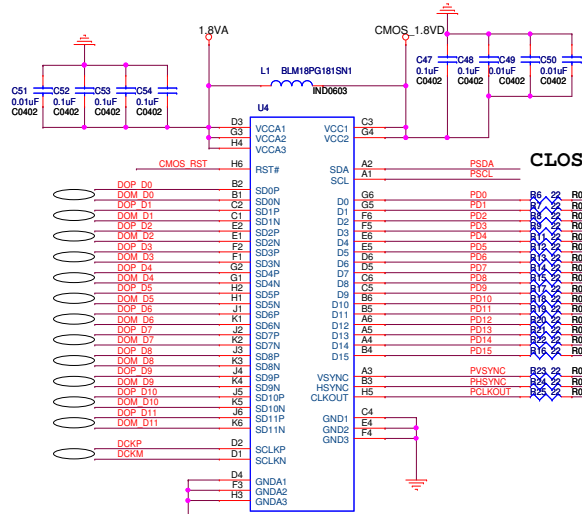
- Change R3 to 2100 1% for 3.3V Analog Voltage
- Populate R49,C66,C67,C68,C69,C70

LEOPARD IMAGING INC		
Title IPNC Camera Board - Sony IMX136-324 -1.8V		
Size A3	Document Number	Rev 1.0
Date: Wednesday, February 01, 2012	Sheet 1	of 2

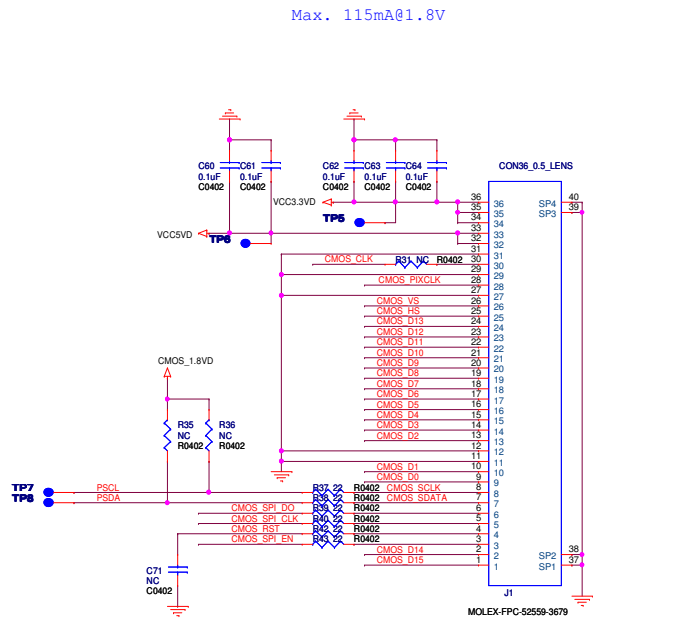


CLOSE TO 1.8V POWER PINS

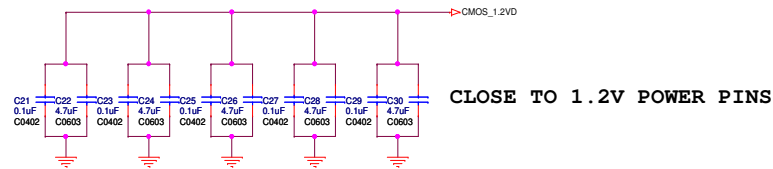
PIN-D3



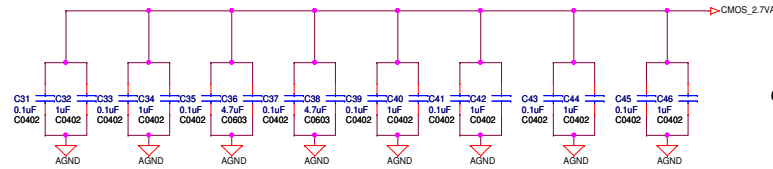
CLOSE TO LVDS324



Max. 115mA@1.8V

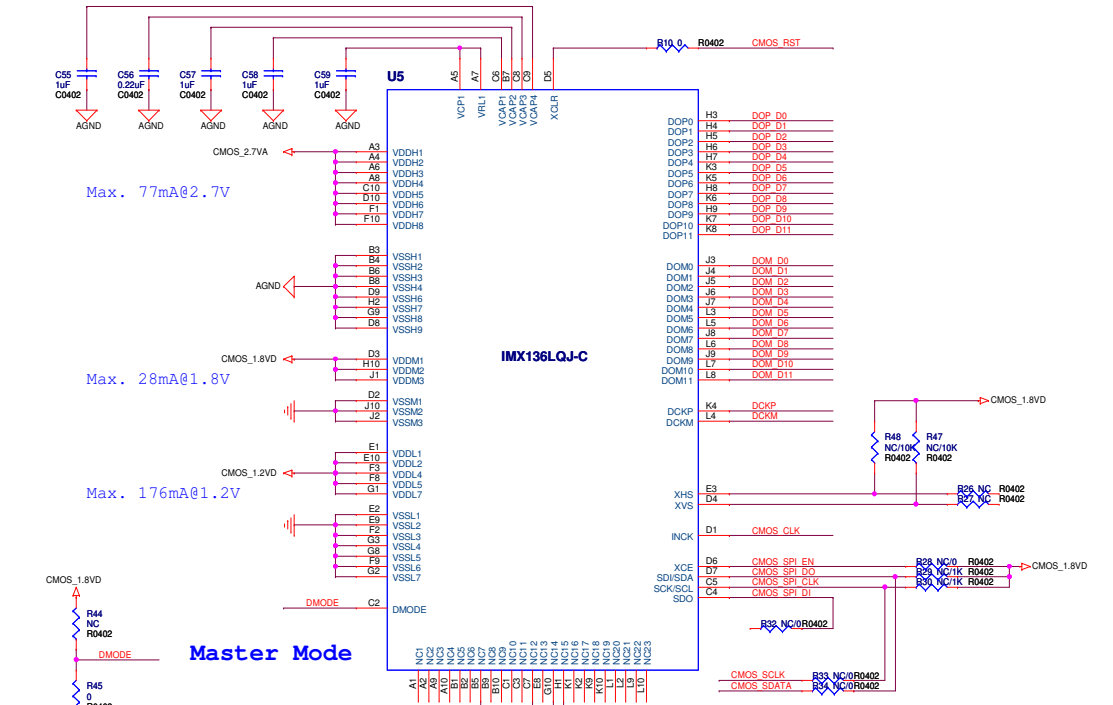


CLOSE TO 1.2V POWER PINS



CLOSE TO 2.7V POWER PINS

PIN-A6
PIN-A8



Max. 77mA@2.7V

Max. 28mA@1.8V

Max. 176mA@1.2V

Master Mode

IMX104 Camera Board

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