Application Report
SLLA349–September 2014

Implementation Guide: DP130 in a Sink

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ABSTRACT

The SN75DP130 compensates for intersymbol interference (ISI) loss across a transmission line to provide the optimum DisplayPort® (DP) electrical performance from source to sink. Even though source applications (notebook, docking station, and so forth) are the intended target application for the DP130, the DP130 can also be used in a sink application (DisplayPort monitor). This document describes how to use the DP130 in a sink application.

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1 Introduction

The SN75DP130 is a four channel DisplayPort® (DP) re-driver that regenerates the DP high-speed digital link. The device complies with the VESA DisplayPort Standard Version 1.2, and supports a four lane main link interface signaling up to HBR2 rates at 5.4 Gbps per lane. The device compensates for ISI loss across a transmission line to provide the optimum DP electrical performance from source to sink.

The DP130 is typically used in source applications either on a motherboard or in a docking station. With its large amount of equalization gain and ability to adjust its outputs levels, the DP130 can also be used in a sink application. This document details how to implement a DP130 in a sink application.

1.1 References

1. SN75DP130 Datasheet (SLLSE57D)
2. Total Phase Aardvark I2C/SPI Host Adapter
3. VESA DisplayPort Standard Version 1, Revision 2a. May 23, 2012

2 Local I^2C Interface

In a sink application, it is recommended to use the DP130's local I^2C interface to configure the DP130's receivers (IN[3:0]P/N) and transmitters (OUT[3:0]P/N). The DP130's internal registers are accessed through the SCL_CTL pin and SDA_CTL pin. The 7-bit I^2C slave address of the DP130 is determined by the ADDR_EQ pin.

Table 1. DP130 I^2C Slave Address Options

ADDR_EQ	7-bit I^2C Slave Address	Read Slave Address	Write Slave Address
Low (VIL)	7'b0101100	'h59	'h58
VCC/2 (VIM)	7'b0101101	'h5B	'h5A
High (VIH)	7'b0101110	'h5D	'h5C

3 Hot Plug Detect (HPD) Implementation

The HPD signal from sink should be connected to the DP130 in one of two ways. The two options are illustrated in Figure 1.

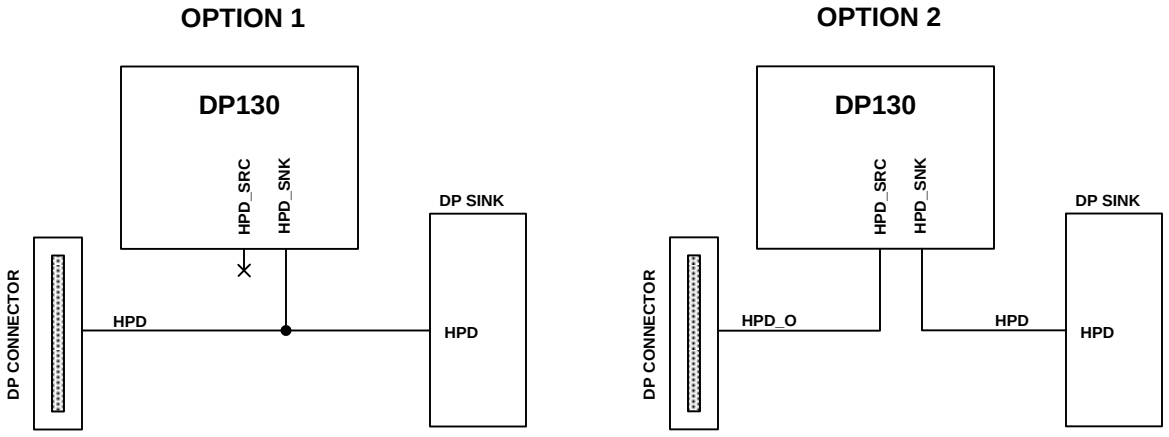

Figure 1. HPD Implementation Options

In a typical sink, the sink will monitor for a source by looking at the AUXP signal and assert HPD when a source is detected. The DP130 will monitor the HPD signal to know when to enter/exit low power state. By following either option above, the DP130 will always be able to conserve power when a source is not connected.

4 AUX Implementation

Connection to the AUX interface is only necessary when monitoring the D3 power state transitions of the sink. When connecting the DP130 to the AUX channel interface, it should be done as shown in Figure 2. The AUX_SRCP/N, SCL_DDC, SDA_DDC, and CAD_SRC pins should be left unconnected and the CAD_SNK pin should be pulled down to ground.

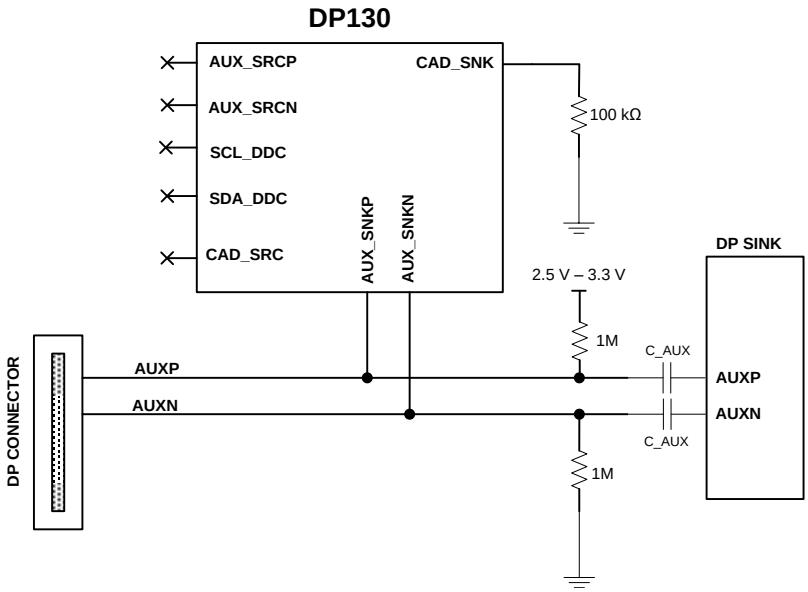

Figure 2. AUX Channel Implementation

Please note, the DP130's link training feature must be disabled. This is done by writing a zero to DP130's LINK_TRAINING_ENABLE bit (address 0x04 bit 2).

In the case in which the AUX interface is not connected to the DP130, whenever the sink is placed into the D3 state by the source software needs to place the DP130 into Low power state by writing a 02h to DP130's DPCD 0x00600 register. The reverse (exiting D3 state) must also be handled by software. Refer to Section 6.2 for details on this DPCD register.

5 Receiver (IN[3:0]P/N) Adjustments

5.1 Equalization Level

In a sink application, it is recommended to use the DP130's local I^2C interface to configure the DP130's receiver equalization level. Before adjusting the DP130's equalization levels, software should first disable the DP130 link training feature by writing a zero to bit 2 of address 04h. Software should then enable equalization control by writing a one to EQ_I2C_ENABLE bit (bit 7 at address 05h). After EQ_I2C_ENABLE is set, then software can program the equalization for each lane (IN[3:0]) to the appropriate value. Refer to Table 2 for details on equalization settings for each lane. For a sink application, it is recommended to choose a higher equalization value like 13 dB or 15 dB.

Table 2. DP130 Equalization Levels

Address	Bit	Description	Access
05h	7	EQ_I2C_ENABLE 0 – EQ settings controlled by device inputs only (default). 1 – EQ settings controlled by I^2C register settings	RW
	2:0	EQ_LEVEL_LANE0. This field selects the EQ gain level for Lane 0 (IN0P/N) when EQ_I2C_ENABLE bit is set and LINK_TRAINING_ENABLE bit is cleared. 000 – 0 dB 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 100 – 5 dB (HBR); 10 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)	RW
07h	2:0	EQ_LEVEL_LANE1. This field selects the EQ gain level for Lane 1 (IN1P/N) when EQ_I2C_ENABLE bit is set and LINK_TRAINING_ENABLE bit is cleared. Bit definition identical to that of EQ_LEVEL_LANE0.	RW
09h	2:0	EQ_LEVEL_LANE2. This field selects the EQ gain level for Lane 2 (IN2P/N) when EQ_I2C_ENABLE bit is set and LINK_TRAINING_ENABLE bit is cleared. Bit definition identical to that of EQ_LEVEL_LANE0.	RW
0Bh	2:0	EQ_LEVEL_LANE3. This field selects the EQ gain level for Lane 3 (IN3P/N) when EQ_I2C_ENABLE bit is set and LINK_TRAINING_ENABLE bit is cleared. Bit definition identical to that of EQ_LEVEL_LANE0.	RW

5.2 Squelch Level

The DP130 squelch level defaults to 80 mVpp. In a sink application it maybe necessary to adjust the squelch level. This is done by changing the SQUELCH_SENSITIVITY register located in the DP130's local I^2C register space. The SQUELCH_SENSITIVITY register is defined in the DP130 datasheet (SLLSE57D). For ease of use, the register is duplicated here. Any discrepancies between this document and the DP130 datasheet, the DP130 datasheet takes precedence.

Table 3. Squelch Sensitivity Levels

Address	Bit	Description	Access
03h	5:4	SQUELCH_SENSITIVITY – Main link squelch sensitivity is selected by this field, and determines the transitions to and from the Output Disable mode 00 – Main Link IN0P/N squelch detection threshold is set to 40mVpp 01 – Main Link IN0P/N squelch detection threshold is set to 80mVpp. (Default) 10 – Main Link IN0P/N squelch detection threshold is set to 160mVpp 11 – Main Link IN0P/N squelch detection threshold is set to 250mVpp	RW
	3	SQUELCH_ENABLE 0 – Main Link IN0P/N squelch detection is enabled (default) 1 – Main Link IN0P/N squelch detection is disabled	RW

6 Main Link Output [OUT[3:0]P/N] Adjustments

In a typical source application, the DP130's link training feature monitors the aux traffic between the source and sink and updates its output levels (TX Swing and Pre-emphasis) based on the contents of the AUX traffic. But in a sink application, the DP130's main link outputs (OUT[3:0]) must be set to a fixed level for the channel between the DP130 and the sink. This predetermined level must never change.

Setting the output level, both TX swing (VOD) and pre-emphasis, is done through the DP130's DPCD registers. It is recommended to start with VOD Level 1 and Pre-emphasis Level 0.

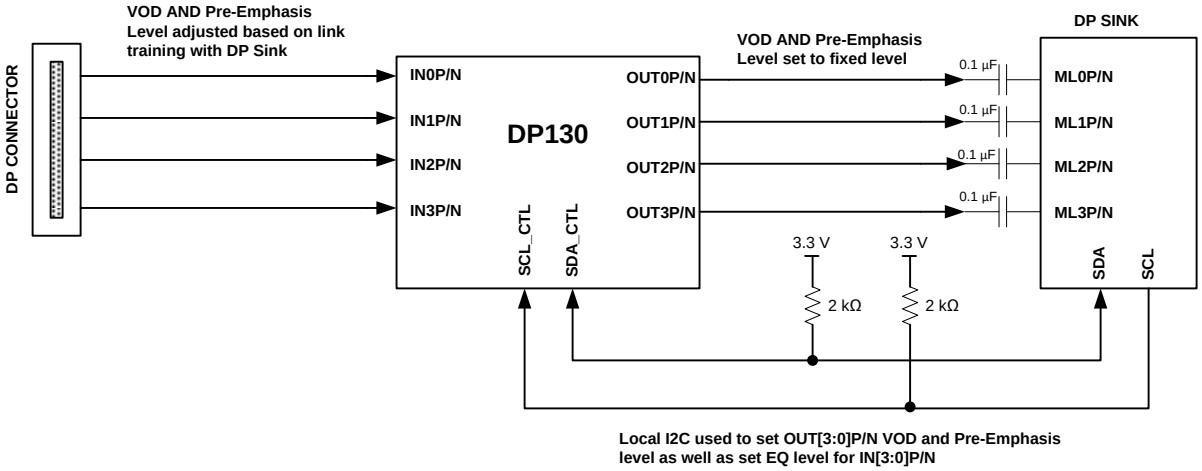

Figure 3. DisplayPort Main Link Implementation

6.1 DPCD Address Space

Access to and from the DP130's DPCD address space is indirectly addressable through the local I^2C registers as illustrated in the Figure 4.

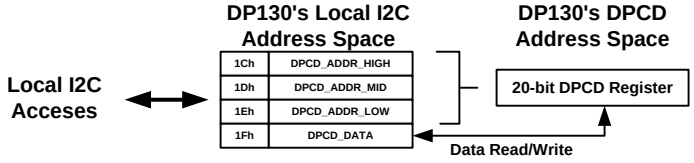

Figure 4. Accessing DP130's DPCD Registers

The configuration of these registers can be performed through the local I^2C interface, where three registers (from 1Ch to 1Eh) are used as the address to the DPCD register and another one (1Fh) as data to be read/written.

6.2 DP130's DPCD Registers

The DPCD registers contained within the DP130 datasheet are duplicated here. Any discrepancies between this document and the DP130 datasheet, the DP130 datasheet takes precedence.

Table 4. DP130 DPCD Registers

DPCD Address	Name	Value Written	Value Read	Description
00100h	LINK_BW_SET	06h	00h	1.62Gbps per lane (RBR)
		0Ah	01h	2.7Gbps per lane (HBR)
		14h	02h	5.4Gbps per lane (HBR2)
00101h	LANE_COUNT_SET	00h	00h	All Lanes disabled
		01h	01h	One lane enabled (OUT0)
		02h	03h	Two lanes enabled (OUT[1:0])
		04h	0Fh	Four lanes enabled (OUT[3:0])

Table 4. DP130 DPCD Registers (continued)

DPCD Address	Name	Value Written	Value Read	Description
00103h	TRAINING_LANE0_SET	00h	00h	VOD Level 0 and Pre-emphasis Level 0 for OUT0
		08h	04h	VOD Level 0 and Pre-emphasis Level 1 for OUT0
		10h	08h	VOD Level 0 and Pre-emphasis Level 2 for OUT0
		18h	0Ch	VOD Level 0 and Pre-emphasis Level 3 for OUT0
		01h	01h	VOD Level 1 and Pre-emphasis Level 0 for OUT0
		09h	05h	VOD Level 1 and Pre-emphasis Level 1 for OUT0
		11h	09h	VOD Level 1 and Pre-emphasis Level 2 for OUT0
		02h	02h	VOD Level 2 and Pre-emphasis Level 0 for OUT0
		0Ah	06h	VOD Level 2 and Pre-emphasis Level 1 for OUT0
		03h	03h	VOD Level 3 and Pre-emphasis Level 0 for OUT0
00104h	TRAINING_LANE1_SET	00h	00h	VOD Level 0 and Pre-emphasis Level 0 for OUT1
		08h	04h	VOD Level 0 and Pre-emphasis Level 1 for OUT1
		10h	08h	VOD Level 0 and Pre-emphasis Level 2 for OUT1
		18h	0Ch	VOD Level 0 and Pre-emphasis Level 3 for OUT1
		01h	01h	VOD Level 1 and Pre-emphasis Level 0 for OUT1
		09h	05h	VOD Level 1 and Pre-emphasis Level 1 for OUT1
		11h	09h	VOD Level 1 and Pre-emphasis Level 2 for OUT1
		02h	02h	VOD Level 2 and Pre-emphasis Level 0 for OUT1
		0Ah	06h	VOD Level 2 and Pre-emphasis Level 1 for OUT1
		03h	03h	VOD Level 3 and Pre-emphasis Level 0 for OUT1
00105h	TRAINING_LANE2_SET	00h	00h	VOD Level 0 and Pre-emphasis Level 0 for OUT2
		08h	04h	VOD Level 0 and Pre-emphasis Level 1 for OUT2
		10h	08h	VOD Level 0 and Pre-emphasis Level 2 for OUT2
		18h	0Ch	VOD Level 0 and Pre-emphasis Level 3 for OUT2
		01h	01h	VOD Level 1 and Pre-emphasis Level 0 for OUT2
		09h	05h	VOD Level 1 and Pre-emphasis Level 1 for OUT2
		11h	09h	VOD Level 1 and Pre-emphasis Level 2 for OUT2
		02h	02h	VOD Level 2 and Pre-emphasis Level 0 for OUT2
		0Ah	06h	VOD Level 2 and Pre-emphasis Level 1 for OUT2
		03h	03h	VOD Level 3 and Pre-emphasis Level 0 for OUT2
00106h	TRAINING_LANE3_SET	00h	00h	VOD Level 0 and Pre-emphasis Level 0 for OUT3
		08h	04h	VOD Level 0 and Pre-emphasis Level 1 for OUT3
		10h	08h	VOD Level 0 and Pre-emphasis Level 2 for OUT3
		18h	0Ch	VOD Level 0 and Pre-emphasis Level 3 for OUT3
		01h	01h	VOD Level 1 and Pre-emphasis Level 0 for OUT3
		09h	05h	VOD Level 1 and Pre-emphasis Level 1 for OUT3
		11h	09h	VOD Level 1 and Pre-emphasis Level 2 for OUT3
		02h	02h	VOD Level 2 and Pre-emphasis Level 0 for OUT3
		0Ah	06h	VOD Level 2 and Pre-emphasis Level 1 for OUT3
		03h	03h	VOD Level 3 and Pre-emphasis Level 0 for OUT3
00600h	SET_POWER	01h	00h	Normal Mode
		02h	01h	Power-Down mode, D3

7 Example Script

The script below is for a Total Phase Aardvark I²C controller. Details on the Total Phase Aardvark I²C controller can be obtained from the Total Phase website.

This example is for a HBR2 (5.4Gbps) data rate with 4 active DisplayPort lanes. This script assumes the AUX signals are connected to the DP130 as illustrated in Figure 2.

```
<aardvark>
<configure i2c="1" spi="1" gpio="0" tpower="1" pullups="0"/>
<i2c_bitrate khz="100"/>

======Disable Link Training=====
<i2c_write addr="0x2D" count="1" radix="16">04 00</i2c_write> />

======Program Link Bandwidth Settings to HBR2===
======DPCD 00100h  =====
<i2c_write addr="0x2D" count="1" radix="16">1C 00</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1D 01</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1E 00</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1F 14</i2c_write> />

======Program Num of Lanes to 4. ===
======DPCD 00101h  =====
<i2c_write addr="0x2D" count="1" radix="16">1C 00</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1D 01</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1E 01</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1F 04</i2c_write> />

======Program VOD L1 and Pre-Emphasis L0 for Lane 0=====
======DPCD 00103h  =====
<i2c_write addr="0x2D" count="1" radix="16">1C 00</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1D 01</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1E 03</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1F 01</i2c_write> />

======Program VOD L1 and Pre-Emphasis L0 for Lane 1=====
======DPCD 00104h  =====
<i2c_write addr="0x2D" count="1" radix="16">1C 00</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1D 01</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1E 04</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1F 01</i2c_write> />

======Program VOD L1 and Pre-Emphasis L0 for Lane 2=====
======DPCD 00105h  =====
<i2c_write addr="0x2D" count="1" radix="16">1C 00</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1D 01</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1E 05</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1F 01</i2c_write> />

======Program VOD L1 and Pre-Emphasis L0 for Lane 3=====
======DPCD 00106h  =====
<i2c_write addr="0x2D" count="1" radix="16">1C 00</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1D 01</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1E 06</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1F 01</i2c_write> />

======Set Power Mode to Normal=====
======DPCD 00600h  =====
<i2c_write addr="0x2D" count="1" radix="16">1C 00</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1D 06</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1E 00</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">1F 01</i2c_write> />

======May want to adjust Squelch Level=====
<i2c_write addr="0x2D" count="1" radix="16">03 10</i2c_write> />
```

```
======Enable EQ=====
<i2c_write addr="0x2D" count="1" radix="16">05 80</i2c_write> />

======Set EQ level to 13dB(HBR2) for lane 0=====
<i2c_write addr="0x2D" count="1" radix="16">05 85</i2c_write> />

======Set EQ level to 13dB(HBR2) for lane 1=====
<i2c_write addr="0x2D" count="1" radix="16">07 05</i2c_write> />

======Set EQ level to 13dB(HBR2) for lane 2=====
<i2c_write addr="0x2D" count="1" radix="16">09 05</i2c_write> />

======Set EQ level to 13dB(HBR2) for lane 3=====
<i2c_write addr="0x2D" count="1" radix="16">0B 05</i2c_write> />

</aardvark>
```

8 DisplayPort Sink Link Training Suggestions

This section provides suggestions for sink manufacturer on how to communicate with a DisplayPort 1.2 source with a DP130 in the middle.

8.1 Adjust AUX Read Interval

The DisplayPort 1.2a standard defines a DPCD register, called TRAINING_AUX_RD_INTERVAL, within the sink that will adjust the timing of the aux read of DPCD link status registers (DPCD address 00202h thru 00204h) and adjust request registers (DPCD address 00206h and 00207h). Typically, a sink will default this register to 00h. Changing the default to 01h or 02h will allow more time for the I^2C writes to the DP130's DCPD registers to complete.

Table 5. Sink's DPCD TRAINING_AUX_RD_INTERVAL Register

DPCD Address	Definition	Read/Write over AUX Ch
0000Eh	TRAINING_AUX_RD_INTERVAL Link status/Adjust request read interval during main link training 00h: 100 µs for main link clock recovery phase and 400 µs for main link channel equalization phase 01h: 4 ms all 02h: 8 ms all 03h: 12 ms all 04h: 16 ms all Other values are reserved	Read-Only

8.2 Link Training Clock Recovery (CR) Phase

During link training, a DisplayPort 1.2 compliant source will follow the CR phase of link training detailed in Figure 5. It is very important the DisplayPort sink take full advantage of the source behavior. The state diagram shows that CR phase will continue as long as the same VOD level is not used 5 times or a max VOD level is never used. Because of this, the sink's CR phase algorithm should never use the same voltage swing level five times or the max voltage swing. Depending on the source, the max voltage swing level can be either Level 2 or Level 3. Typically, a sink's algorithm will start at level 0 and progress to level 3. It is suggested to try level 0 two times, level 1 four times, level 2 four times, and level 3 once. Please keep in mind source support for level 3 is not required. For the case in which level 3 is not support by the source, level 2 will happen once.

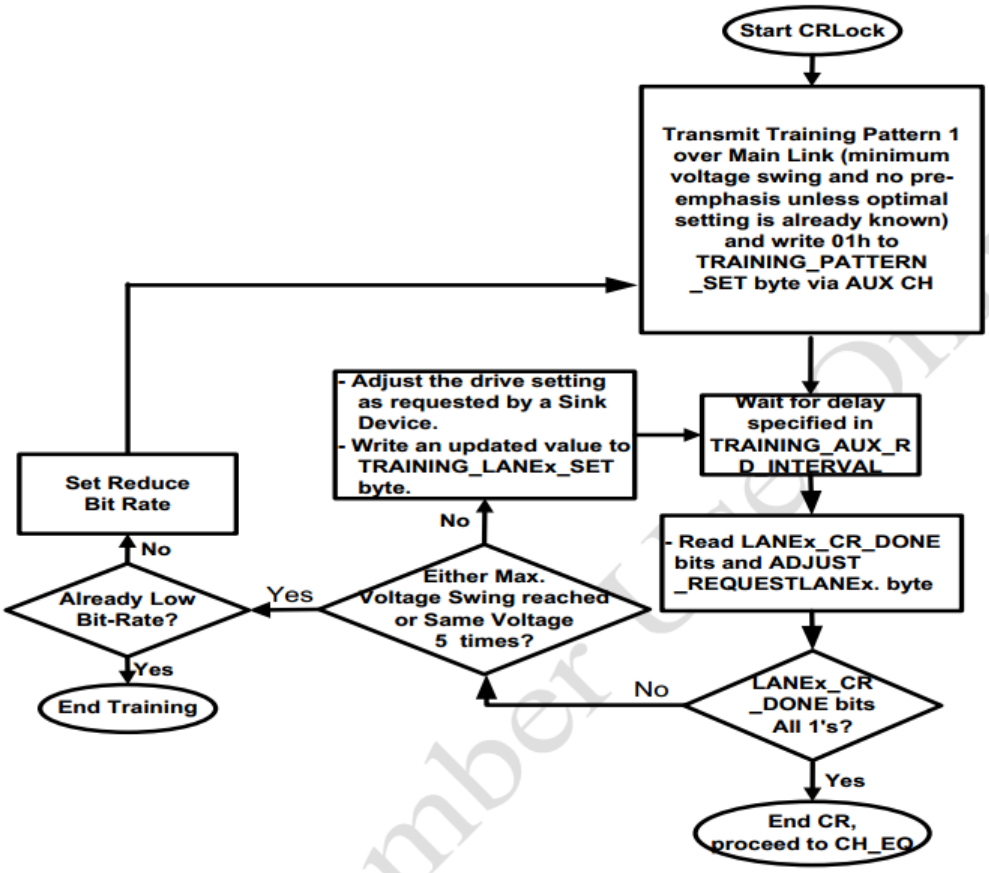

Figure 5. DisplayPort 1.2a Link Training CR Phase State Diagram

8.3 Link Training Channel Equalization (EQ) Phase

During link training, a DisplayPort 1.2 compliant source will follow the channel EQ phase of link training detailed in Figure 6. It is very important the DisplayPort sink take full advantage of the source behavior. In the EQ phase of link training, the sink will typically request an increase in pre-emphasis level starting at level 0 and ending at level 3. As mentioned in Section 6, the channel between DP130 and sink is fixed and therefore should be programmed to a fixed voltage swing and pre-emphasis level through the DP130's local I^2C interface. The EQ increase requested by the sink will not cause the DP130 to increase its output pre-emphasis level. As Figure 6 indicates, a loop count greater than 5 will cause the EQ phase to end. In order to help guarantee a successful EQ phase, the sink's channel EQ algorithm should request pre-emphasis level 0 two times, level 1 two times, and level 2 once. The sink is welcome to try other combinations but needs to keep in mind that once is loop count requirement is meet the source will end channel equalization phase of link training.

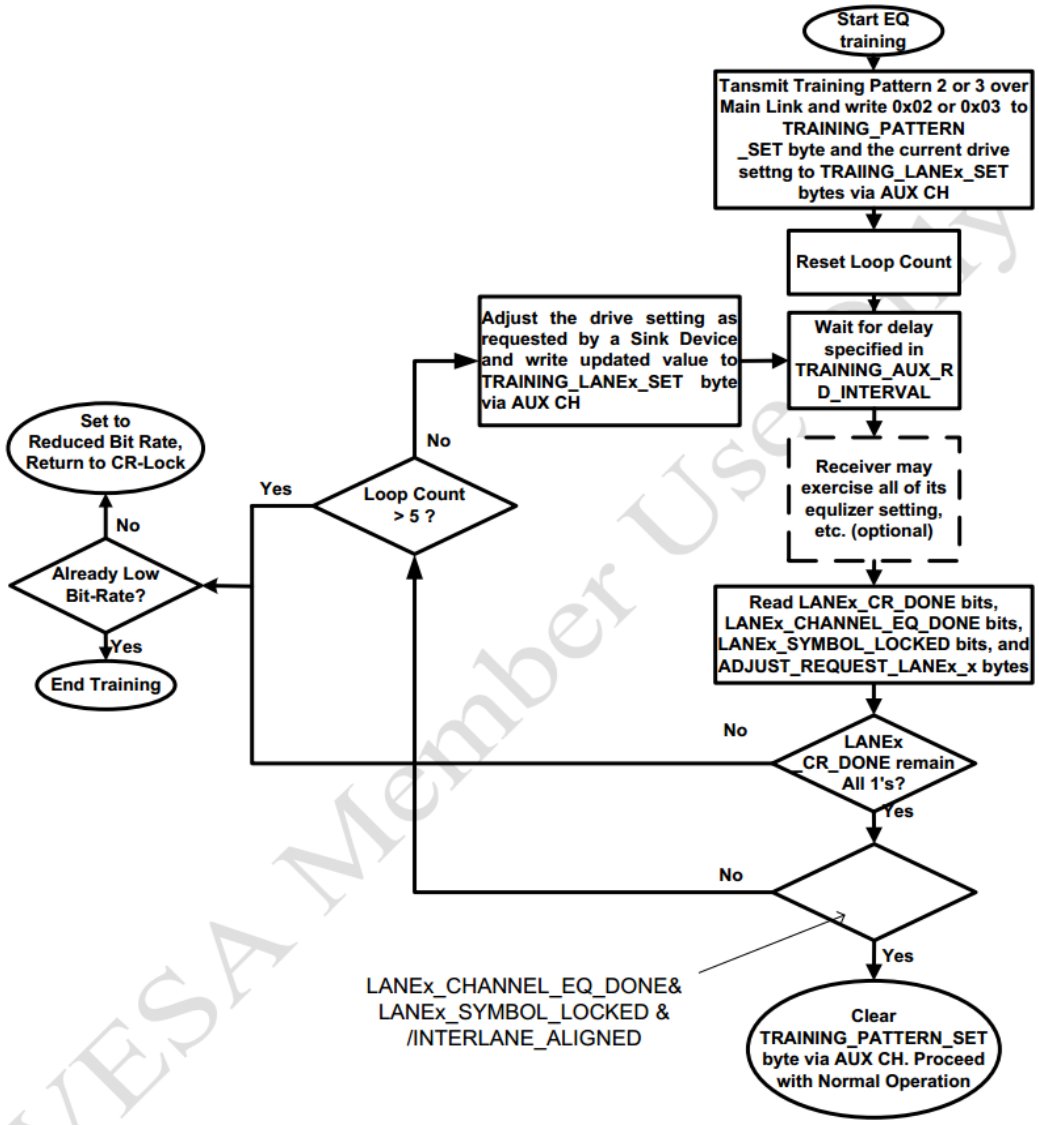

Figure 6. DisplayPort 1.2a Link Training Channel Equalization Link Phase State Diagram

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