Application Note

TMDS1204 Implementation Guide

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ABSTRACT

The TMDS1204 is a HDMI 2.1 redriver supporting data rates up to 12Gbps. It is backwards compatible to HDMI 1.4b and HDMI 2.0b. The high-speed differential inputs and outputs can be either AC-coupled or DC-coupled, which qualifies the TMDS1204 to be used as a DP++ to HDMI level shifter, HDMI redriver, or a DisplayPort™ redriver. The TMDS1204 can support 3 lane HDMI2.1 FRL at 3 and 6 Gbps and 4 lane HDMI2.1 FRL at 6, 8, 10, and 12 Gbps.

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1 Introduction

These guidelines serve as a starting point for configuring the TMDS1204 device for your application.

2 General Configuration Pin

EN: When low, TMDS1204 will be held in reset. The EN pin has a internal 250k pull-up to VIO. For passive circuitry implementation, it is recommended to add an external 0.22 µF pull-down capacitor on the EN pin.

VIO: The TMDS1204 supports 1.2-V, 1.8-V, and 3.3-V LVCMOS levels depending on the source I/O voltage requirement. The VIO pin is used to select which voltage level is used for the following 2-level control pins: LV_DDC_SDA, LV_DDC_SCL, SCL/CFG0, and SDA/CFG1.

Table 2-1. VIO Voltage Based on the LVCMOS Signaling Level

VIO Pin	LVCMOS Signaling Level
VIO < 1.5 V	1.2 V
1.5 V < VIO < 2.5 V	1.8 V
VIO > 2.5 V	3.3 V

Mode (pin-strap or I2C mode): The MODE pin provides four modes of operation: three pin-strap modes and one I2C mode.

In all three pin strap modes, the DDC snooping feature is enabled. In I2C mode, the DDC snoop feature is enabled by default but can be disabled by a register.

Table 2-2. Mode Pin Setting

Mode	Description
0	Pin-strap mode with fixed receiver equalizer
R	Pin-strap mode with flexible receiver equalizer and fan-out buffer support
F	I2C mode
1	Pin-strap mode with flexible receiver equalizer with no fan-out buffer support

Fan-out buffer: In some applications a HDMI sink requires the clock and data must be on separate paths. The TMDS1204 implements a fan-out buffer feature to support such applications. When the fan-out buffer feature is enabled, the TMDS1204 will output the HDMI clock on RCLKOUTp/n when operating in HDMI 1.4 or HDMI 2.0. The OUT_CLKp/n will be disabled. When operating in HDMI 2.1 FRL mode, the TMDS1204 will output FRL data lane 3 on OUT_CLKp/n. RCLKOUTp/n will be disabled. The feature is enabled in pin-strap mode when MODE pin = "R" or it can be enabled through FANOUT_EN register when TMDS1204 is configured for I2C mode. However, the fan-out buffer feature will be disabled if swap is enabled.

SCL/CFG0: In pin-strap mode, this is the CFG0 pin. It is recommended to tie this pin to '0' for normal HDMI mode. In I2C mode, this is the SCL pin.

SDA/CFG1: In pin-strap mode, this is the CFG1 pin. The CFG1 pin needs to be set to '0' for normal lane ordering, but set to '1' if the input/output lane order is swapped. In I2C mode, this is the SDA pin.

LINEAR_EN pin: The TMDS1204 supports both linear and limited modes and it's recommended to operate in each mode for sink and source applications, respectively. When configured as a linear redriver, the TMDS1204 differential output levels are a linear function of the GPU output levels enabling TMDS1204 to be transparent to link training and operate as a channel shortener. When configured as a limited redriver, the TMDS1204 differential output voltage levels are independent of the graphics process unit (GPU) output levels ensuring HDMI compliant levels at the receptacle.

The TMDS1204 in pin-strap mode provides the option to dynamically switch between limited and linear based on the HDMI mode of operation. It is recommended to set the LINEAR_EN pin = "F" when using this device in sink applications. It is recommended to set the LINEAR_EN pin = "0" when using this device in source applications. If using I2C mode, the LINEAR_EN register can be set to "1" to enable linear mode.

LINEAR_EN Pin Level	HDMI 1.4, 2.0, or DP	HDMI 2.1 FRL
0	Limited Enabled	Limited Enabled
R	Reserved	Reserved
F	Linear Enabled	Linear Enabled
1	Limited Enabled	Linear Enabled

Note

For HDMI2.1 in linear mode, the GPU transmitter must meet the following requirements.

GPU TX Transmitter	Min	Max	Units
Single-ended SWING	400	500	mV
Rise/Fall time for 3, 6, 8, 10, 12Gbps FRL		16	mV/ps

SIGDET_OUT: The TMDS1204 is fully functional when a signal is detected. If no signal is detected then the device enters standby state waiting for a signal. This pin supports the input signal detect function as part of the TMDS1204 power management feature. While in standby state and the HPD_IN pin is asserted high, the TMDS1204 will assert the SIGDET_OUT pin low when the signal is detected on either IN_CLK or IN_D2 per Table 2-3. Otherwise SIGDET_OUT pin is de-asserted when entering power down or standby state. If used, the SIGDET_OUT pin requires an external pull-up resistor of 10-kΩ or greater

Table 2-3. SIGDET_OUT Signal Reference

	HDMI 1.4 or 2.0	HDMI 2.1
Swap Enabled	IN_D2 signal reference	IN_CLK signal reference
Swap Disabled	IN_CLK signal reference	IN_D2 signal reference

External DDC Level Shifter: Since there is no DDC buffer function for the TMDS1204 device, an external DDC level shifter must be implemented if DDC buffering is desired. When designing with a external DDC level shifter, keep in mind that the HDMI specification limits the DDC bus capacitance to ≤ 50-pF for both an HDMI source and sink. Therefore, care must be taken to make sure that the capacitance of the external DDC level shifter does not cause the total capacitance between source or sink and the HDMI receptacle to become greater than 50-pF.

3 Transmitter Configuration

AC_EN: In pin-strap mode, the AC pin selects between AC-coupled or DC-coupled transmitter

Table 3-1. AC_EN Pin Setting

AC_EN	Description
0	DC-coupled
1	AC-coupled

TXPRE: The TMDS1204 provides pre-emphasis/de-emphasis on the data lanes allowing the output signal pre-conditioning to offset interconnect losses between the TMDS1204 outputs and a TMDS/FRL receiver. De-emphasis is not implemented on the clock lane unless the TMDS1204 is in HDMI 2.1 FRL mode and at which time the clock lane becomes a data lane. Pre-emphasis is not implemented in HDMI 2.1 FRL mode. There are two methods to implement pre-emphasis, pin strapping or through I2C programming. TX pre-emphasis and de-emphasis control is only supported in limited mode.

The transmitter pre-emphasis and de-emphasis control is only supported in limited mode for HDMI 1.4 or HDMI 2.0. When the TDP1204 is operating as an HDMI 2.1 redriver pre-emphasis implementation is not available and only the de-emphasis is modified by the device based upon the DDC TXFFE snooped value. Therefore, when using pin-strap mode, the TXPRE pin controls four different global pre-emphasis/de-emphasis values for all data lanes when TMDS1204 is operating in limited mode for HDMI 1.4 or HDMI 2.0. However, in HDMI 2.1 FRL mode, the TXPRE pin has no effect.

Table 3-2. TXPRE Pin Setting

TXPRE	HDMI1.4 or 2.0	HDMI2.1 TXFFE Level
0	3.5 dB pre-emphasis	Refer to TXFFE Level
R	–2.5 dB de-emphasis	Refer to TXFFE Level
F	0 dB	Refer to TXFFE Level
1	6 dB pre-emphasis	Refer to TXFFE Level

FRL TX FFE Level	De-emphasis (dB)
TXFFE0	-2.5
TXFFE1	-3.5
TXFFE2	-3.7
TXFFE3	-4.6

TXSWG: The TMDS1204 transmitter swing level can be adjusted in both pin-strap and I2C mode.

In I2C mode, TX swing settings are controlled independently for each lane through the registers of the device. In pin strap mode, with limited mode enabled, the TXSWG pin adjusts the default 1000 mV swing. However, when linear mode is enabled, the linearity range is fixed at the highest level (1200mVpp) so TXSWG pin is not used.

In HDMI 1.4, the TXSWG controls the swing for both the data and clock lanes. In HDMI 2.0, the TXSWG pin controls the data lanes only and the clock lane remains at the default value. In HDMI 2.1, the TXSWG pin controls data and clock lanes.

Table 3-3. TXSWG Pin Setting

TXSWG pin	Limited Mode for HDMI 1.4	Limited Mode for HDMI 2.0	Limited Mode for HDMI 2.1	Linear Mode
0	Default (1000 mVpp)	Default (1000 mVpp)	Default + 10%	1200 mVpp
R	Default − 5%	Default − 5%	Default-5%	1200 mVpp
F	Default (1000 mVpp)	Default (1000 mVpp)	Default (1000 mVpp)	1200 mVpp
1	Default (1000 mVpp)	Default + 5%	Default + 5%	1200 mVpp

4 Receiver Configuration

CTLEMAP_SEL: The TMDS1204 in pin-strap mode has three CTLE HDMI Data rate Maps: Map A, Map B, and Map C. Map A and C must be used if TMDS1204 is used in a source application and Map B for a sink application.

	CTLEMAP_SEL PIN Setting			
	0	R	F	1
CTLE Data Rate Map	B	C	B	A

Receiver equalization: The receiver equalizer is used to clean up inter-symbol interference (ISI) jitter. TMDS1204 supports fixed receiver equalizer by setting the EQ0 and EQ1 pins in pin-strap mode or through I2C register. TMDS1204 also supports adaptive equalization (AEQ) for HDMI2.1 FRL as determined by the MODE pin configuration. The adaptive equalization starts when FRL link training begins. It will also re-adapt each time the data rate changes. The adaption will only occur during the TXFFE0 portion of FRL link training when LTP5, LTP6, LTP7, or LTP8 is being received.

DC Gain: The TMDS1204 has three sets of CTLE curves (3-Gbps CTLE, 6-Gbps CTLE, and 12-Gbps CTLE). This pin selects the DC gain setting to apply to each of the three sets of CTLE curves.

DC Gain Pin Level	CTLE DC Gain
0	-3 dB
R	-3 dB
F	0 dB
1	+1 dB

References

- Texas Instruments: *TMDS1204 12-Gbps, DC or AC-Coupled to TMDS® and FRL HDMI™ Hybrid Redriver*, data sheet.

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