

Working with DC coupled Clock pins in AFE7225

ABSTRACT

AFE7225 offers a wide range of features catering to multiple applications. It accepts the differential as well as single-ended input clock. However, in single-ended clock mode, it does not allow the AC coupling of clock pins with driver.

This application report provides information about how AFE7225 can be used in such applications where AFE7225 works in single-ended clock mode with AC coupled driver.

1 AFE7225 Clock Circuit in Single-Ended Clock Mode

SE (single-ended) clock buffer in AFE7225 is realized by chain of inverters. The V_L and V_H levels of inverter are located at 550 mV and 1.35 V respectively. This requires that signal at clock input should have minimum swing of ± 400 mV on common mode of 950 mV.

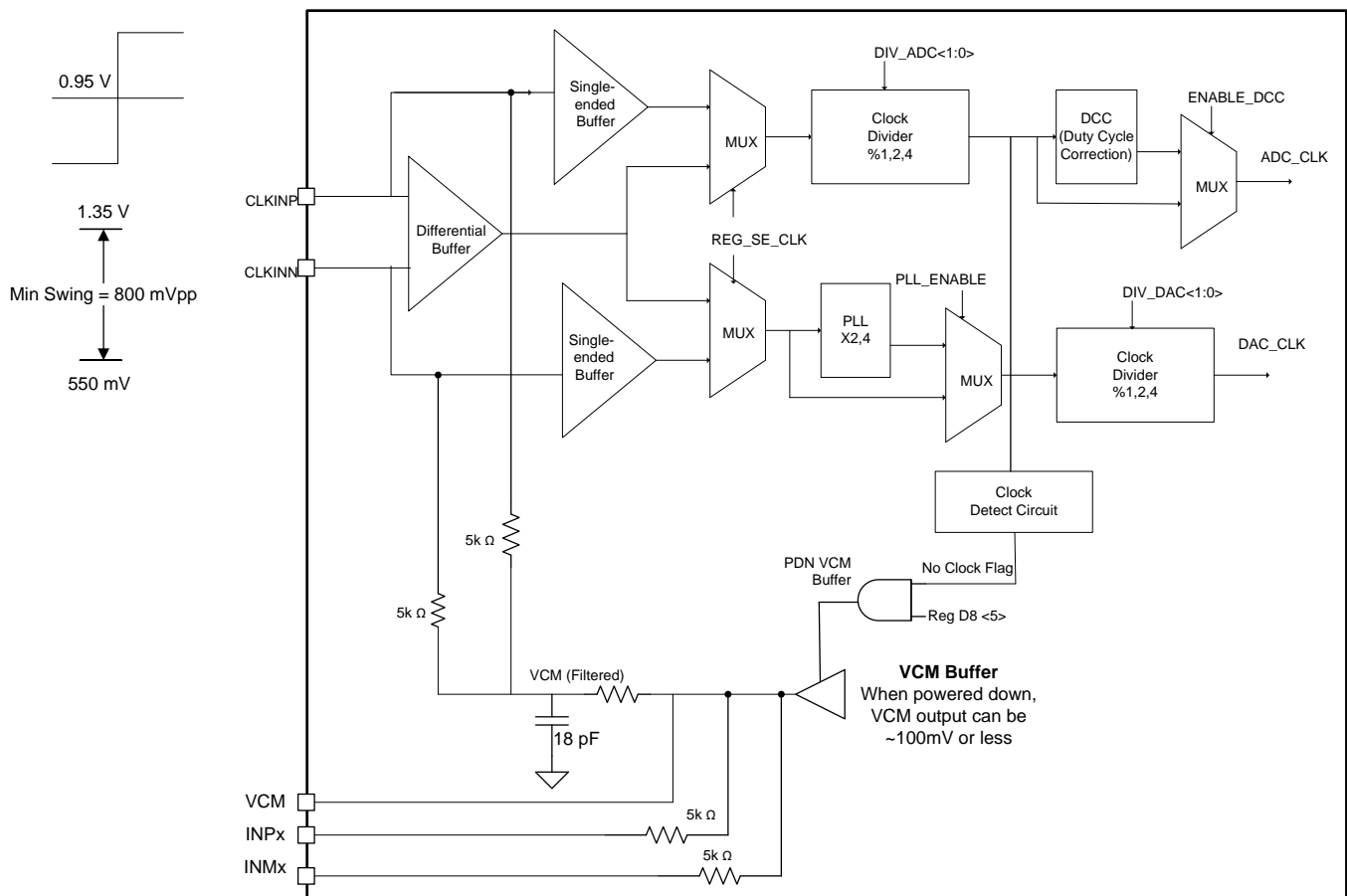


Figure 1. Internal Clock Circuit in AFE7225

In the event of AC coupling, the small amplitude signal at CLKIN[P|N] pin does not cross the valid logic levels, as a result inverter does not detect the clock.

In theory, a large (2.7 V) amplitude signal is needed before the AC coupling capacitor so the signal at CLKIN[P|N] crosses valid logic thresholds. A signal at the CLKIN[P|N] pin needs to cross V_L and V_H levels. When the driver is AC coupled to clock pin, the DC component is removed by a coupling capacitor. Therefore, before the coupling capacitor, at least $1.35 \times 2 = 2.7$ V amplitude is required, so that V_H is crossed by signal after the coupling capacitor at CLKIN[P|N], which is initially biased at 0 V, to generate ± 1.35 V at CLKIN[P|N].

See [Figure 2](#) for clarification.

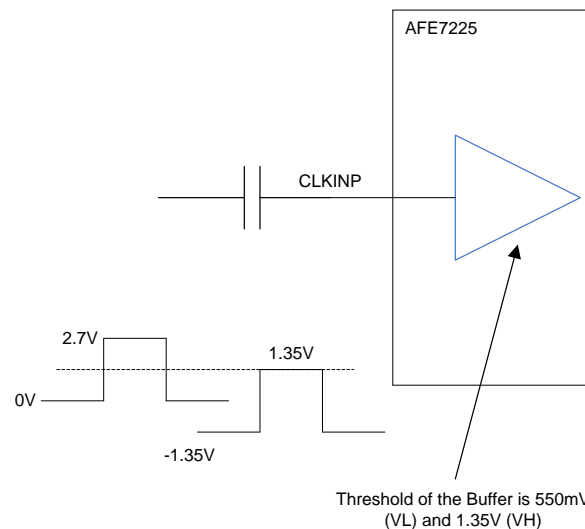


Figure 2. Single Ended Clock Buffer in AFE7225

2 Using Register address D8h bit 5

This problem can be solved as follows:

- The CLKIN[P|N] pin is internally biased to VCM voltage as shown in [Figure 1](#).
- The VCM buffer needs a valid clock signal at CLKINP in order to provide specified voltage (0.95 V typical).
- However, by setting register bit D<5> to '1', the VCM buffer can provide 0.95 V output even in absence of a valid clock signal at CLKINP pin.
- Once common mode voltage at CLKINP pin is set to 0.95 V, a clock signal with minimum amplitude of 800 mVpp can reliably be detected by single-ended clock buffer resulting in normal operation.
- Bit D8<5> can be set to '1' after the device is powered-up and reset is applied. Once set, this bit can remain at '1'.

Bit D8<5> was originally meant for design debug purpose. There is no known impact on performance or functionality of using this bit continually in operation. Under absence of a valid clock signal at CLKIN[P|N] pin, this bit can be used to provide VCM buffer output of 0.95 V.

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