



# High-Side Current Sensing

## With Benchmarq's Fast-Charge Control ICs

### Introduction

A low-side, current-sensing resistor in a fast-charge control circuit generates a small voltage drop between the low side of the battery pack and ground. This drop is not a problem in most cases; however, some applications, particularly mobile communications circuits, are intolerant of any potential difference between the low side of the battery pack and ground. Using a few additional components in the circuit, high-side current sensing solves this problem and allows the charging source, application circuit, and battery pack to share a common ground.

### Circuit Implementation

In a high-side sensing application, the sense resistor ( $R_1$ , usually 10–100m $\Omega$ ) is between the inductor and the positive battery-pack terminal. (See Figure 1.) The negative pack terminal is connected to ground. The voltage across  $R_1$  is translated to a ground-referenced signal for presentation at the current-sense pin of the fast-charge control IC by two complementary small signal transistors (Q1, Q2) that form a “voltage mirror.” The mirror reflects the voltage across  $R_1$  onto the much larger 1k $\Omega$  resistor  $R_2$  in the emitter of PNP transistor Q2. The collector current of Q2 (the “sense-resistor signal current”) will recreate the sense-resistor voltage each time it is passed through a 1k $\Omega$  resistor ( $R_3$  and  $R_4$ ) referenced to ground.

The mirror's transistor pair is biased by a current sink formed by an NPN transistor (Q3) with its base at  $V_{CC}$  and its emitter connected to ground through an 18k $\Omega$  resistor ( $R_5$ ). This arrangement assures that (1) the battery will not be loaded by the bias network when power is not

applied, and (2) the best voltage compliance will occur at the regulated value of charging current.

The inputs to both the pack-voltage monitoring pin (BAT) and temperature sensing pin (TS) of the fast-charge control IC must be translated up in voltage by the sense resistor voltage in order to simulate the fast-charge control chip's accustomed low-side sensing environment.

For the TS input, the sense-resistor signal current is intercepted by the emitter of another PNP transistor (Q5), the base of which is biased to the thermistor connection point. The 1k $\Omega$  resistor ( $R_3$ ) in the emitter path of Q5 creates a voltage equal to the sense-resistor voltage plus the base-emitter drop of Q5. Buffering this point with a complementary NPN transistor (Q4) subtracts this base-emitter drop and leaves the proper signal level to be applied to the TS input. Q4 requires a load: the 10k $\Omega$  resistor ( $R_6$ ) to ground in its emitter path.

Having flowed through Q5 and its emitter resistor, the sense resistor signal current now flows through the 1k $\Omega$  resistor ( $R_4$ ) in Q5's collector to ground, re-creating the voltage across the sense resistor ( $R_1$ ) for the SNS input.

BAT input-voltage is translated by connecting the battery pack voltage-divider pair between the high side of the sense-resistor and the SNS input. This configuration allows the BAT input to ride on top of the sense resistor voltage at SNS. The total bias current of the battery divider network must not significantly disturb current regulation; a bias current of 10A or less will contribute less than 4.3% error in this example circuit.

The principles of operation of this circuit can be applied to all of Benchmarq's Fast-Charge Control ICs.

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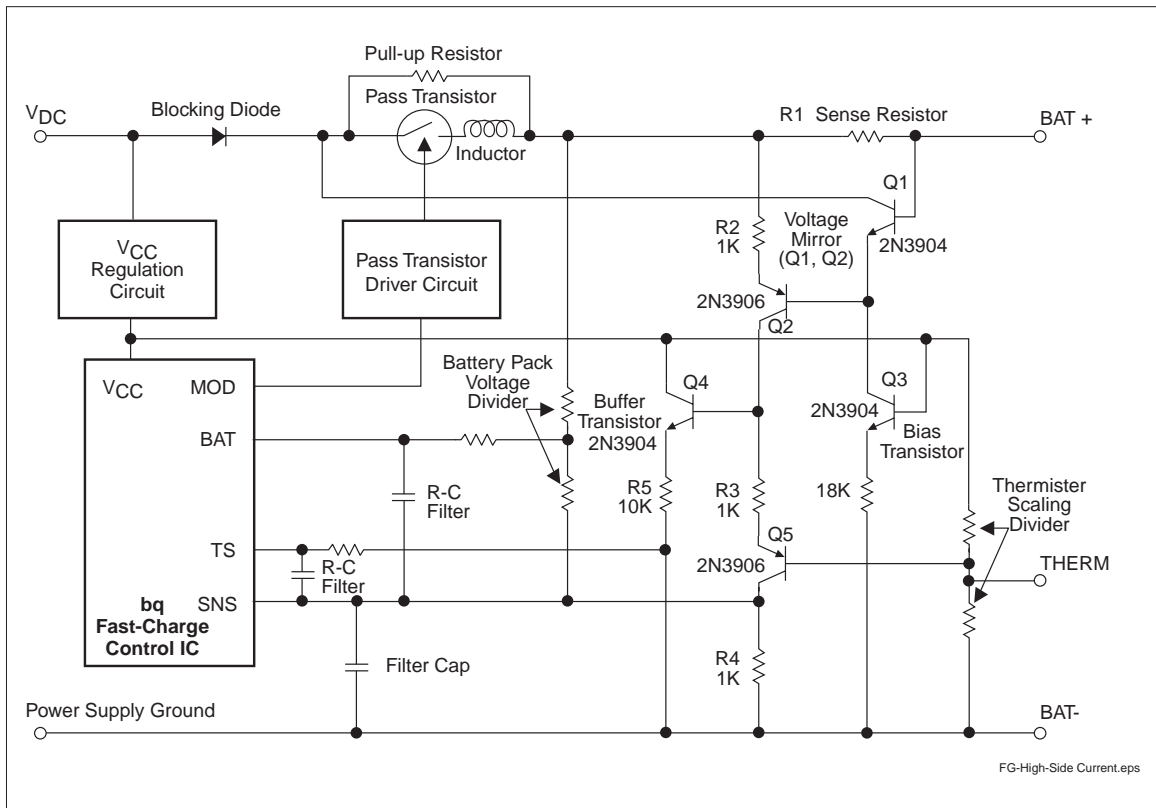


Figure 1. High-Side Sensed P-Channel Diagram

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