APPLICATION NOTE U-159

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BOOST POWER FACTOR CORRECTOR DESIGN WITH THE UC3853

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ABSTRACT

The UC3853 is designed to provide high performance power factor correction (PFC) for low to medium power applications with minimal complexity. It provides power supplies in the range of 10 to 200 watts with a low distortion, power factor corrected input current, a regulated output voltage and operation over a wide range of input voltages. The UC3853 uses average current mode control and works with either a boost or flyback converter. It was developed from the UC3854 family of PFC control circuits and has the same functionality in an 8-pin package. Much of the information available for the UC3854 family of integrated circuits is also applicable to the UC3853. In particular, Unitrode Application Note U-134 provides a good general introduction to power factor correction. U-134 contains an extended description of power factor correction, the boost PFC and the control circuits necessary to provide the correct programming of the current waveform. The reader is urged to review that note as well as this one before designing a boost power factor corrector.

This Application Note describes the features and functions of the UC3853 in detail. The design process for a boost power factor corrector is presented and the design details for a 100W output boost power factor corrector with a "universal" input voltage range of 80-270VAC are included. A table that extends the 100W boost converter example over the range of 25W to 200W is featured. A step-by-step summary of the design process is also provided so that the boost converter circuit may be customized for any application.

ABOUT THE UC3853 PFC CONTROLLER

The UC3853 has many similarities to the UC3854 based family of devices. It contains an average current mode control loop for a low distortion input current waveform, a multiplier to program an accurate current waveform and a voltage error amplifier to regulate the output voltage. The UC3853 also contains over-voltage protection for the output and has a fixed frequency internal oscillator which is synchronizable.

A block diagram of the UC3853 is shown in Figure 1. Due to its 8-pin simplicity, some pins serve more than one function and some functions are brought inside the chip altogether. The UC3853 begins operation when the voltage at the VCC pin is greater than 11.5V. An undervoltage lockout function (UVLO) keeps the device from operating before this voltage is reached. The UC3853 enters the UVLO state again when VCC drops below 9.5V. The hysteresis in the UVLO allows the device to be started from a capacitor which is trickle charged directly from the input voltage. When in UVLO, most of the internal circuits are not powered so the supply current is less than 500μA (250μA typical). The reference voltage in the UC3853 is internal to the device and is not brought out to a pin. The reference is divided down to 3.0V at the non-inverting input to the voltage error amplifier. The reference is trimmed to an accuracy of better than 2% at the FB pin of the voltage error amplifier so the reference voltage specification includes the offset of the amplifier. The total variation of the reference over temperature, including the set point accuracy, is 3.0V ±3.5%. For a typical 400V output the accuracy translates into an output variation of ±8V at room temperature, which is comparable to the ripple voltage amplitude on the output at full power.

The output of the UC3853 supplies 500mA peak current to the gate of the power MOSFET switch. A simplified schematic of the output driver is shown in Figure 2. The VCC pin provides the voltage feedforward signal needed by the multiplier/divider/squarer circuit and thus it has a wide input voltage range under normal operation. The output voltage

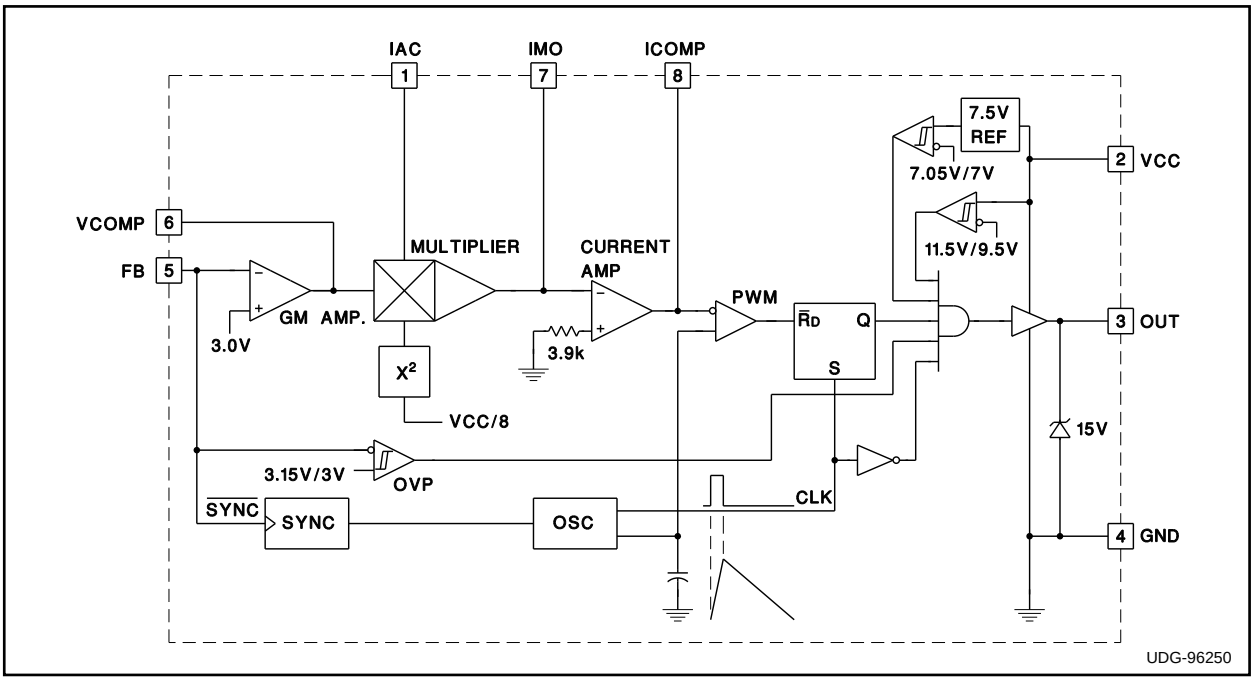

Figure 1. Block Diagram of UC3853

is therefore clamped near 15V to prevent the gate of the MOSFET switch from being driven beyond its breakdown voltage as VCC changes. When power is not applied to the device the output driver is self-biased to hold the output to within 1.5V of ground. When VCC is above the UVLO threshold the bias circuit is disabled and the output driver operates normally. This prevents the MOSFET from turning on when power is first applied to the converter. If the output were not held low, the gate to drain capacitance of the MOSFET would pull the gate high when power is applied and turn the device on, which often results in its destruction.

The PWM comparator uses the oscillator ramp and the output of the current amplifier to generate the gate drive output as shown in Figure 3. The output of the comparator is latched for the duration of the clock period to prevent false output pulses. The latch is set by the clock signal at the beginning of each clock period to drive the output high and is reset by the PWM comparator to drive the output low. The output is kept low by the status inputs to the AND gate that drives the output. The status inputs are the undervoltage lockout (UVLO), the reference valid and the output overvoltage status signal. The output is also held low during the clock interval.

The oscillator is internal to the UC3853, has a fixed 75kHz operating frequency and may be synchronized to an external source. The oscillator waveform is a reverse sawtooth because a negative slope ramp is required to provide the proper polarity for the PWM circuit and for the slope compensation of the average current loop. The current loop error amplifier inverts the current signal so the oscillator ramp must have a negative slope. The rel-

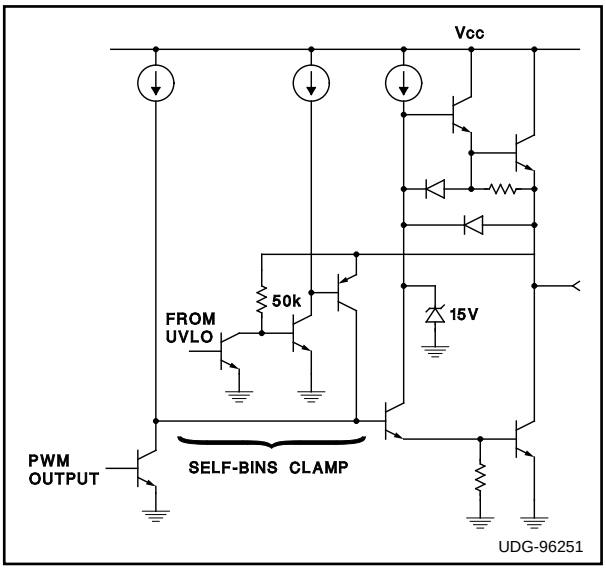

Figure 2. UC3853 Output Driver (Simplified Schematic)

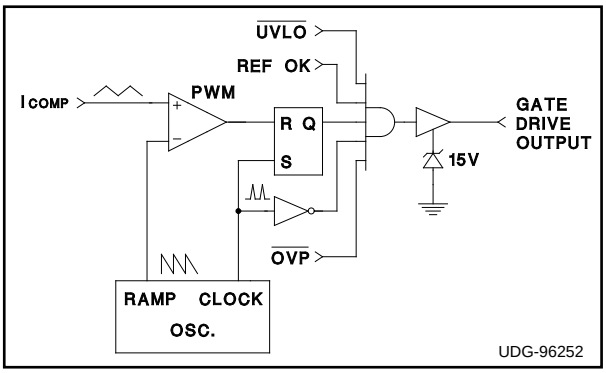

Figure 3. UC3853 PMW Circuit

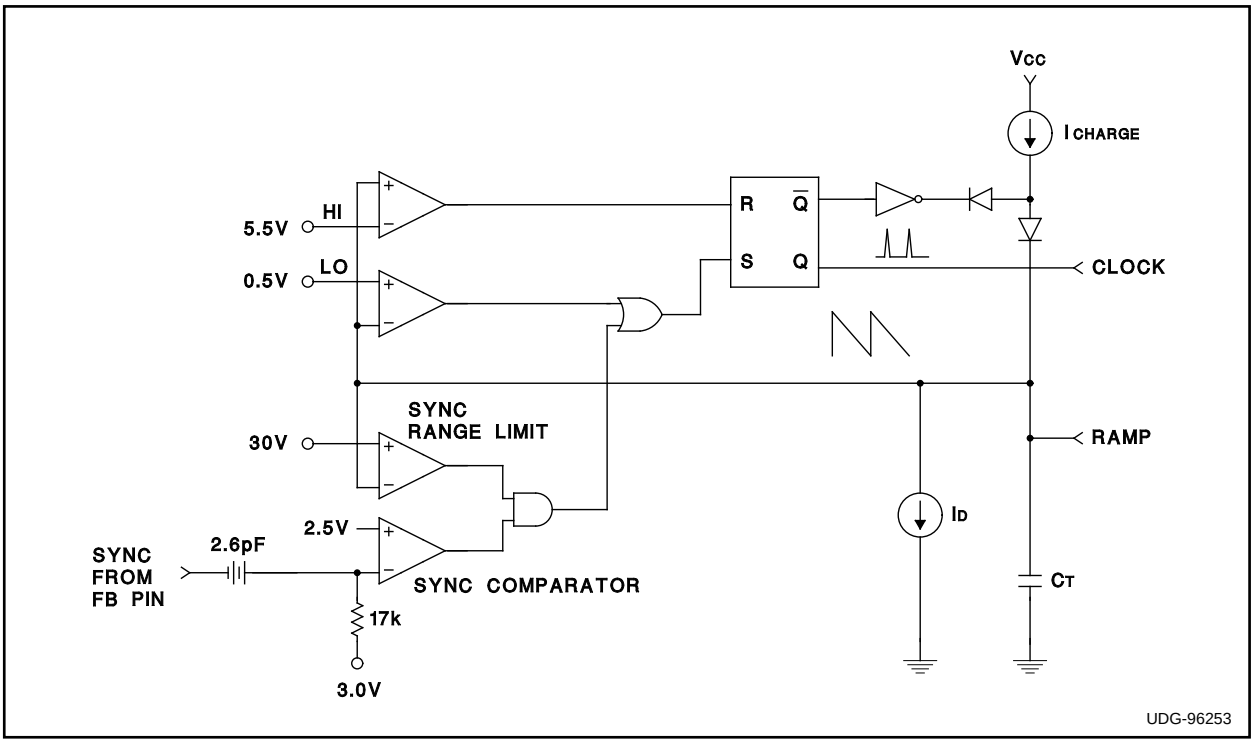

Figure 4. UC3853 Oscillator Equivalent Circuit

ative polarity of the two signals is therefore opposite, which is the correct orientation. This is all internal to the device. The width of the clock output pulse determines the minimum dead time of the output and is less than 1% of the clock period. An equivalent circuit for the oscillator and the sync circuit is shown in Figure 4.

The synchronizing pulse for the oscillator comes from the FB pin. The voltage feedback and the overvoltage protection are also connected to the FB pin. If the synchronizing signal is capacitively coupled into the FB pin it will not upset the DC output voltage value since the bandwidth of the amplifier is very small compared to the switching frequency. The compensation network on the output of the transconductance amplifier will eliminate the synchronizing signal from the output of the amplifier. The guaranteed synchronization frequency range is 95kHz to 115kHz. Circuits for synchronizing the oscillator are described later in this Application Note.

The voltage and current loop amplifiers, the squarer and the multiplier/divider circuits are shown in Figure 5. The current amplifier is a wideband operational amplifier and it has ground referenced inputs. The inverting input of the amplifier is a summing junction where the feedback, the input current signal and the current programming signal from the multiplier output come together. The current signal is negative and the output of the multiplier is positive so the current loop is adjusted to keep the voltage at the inverting input zero since the non-inverting input of the current amplifier is connected to ground through a 3.9kΩ resistor. This resistor provides DC balancing of the amplifier input bias currents. The amplifier has sufficient output drive capability to handle a wide range of feedback networks.

The squarer and multiplier/divider are the heart of the control circuit and are shown in Figure 5. This circuitry makes it possible to operate a boost PFC stage over a 3:1 input voltage range and still get excellent voltage loop bandwidth and fast response to input voltage variations. The multiplier/divider requires three inputs which are traditionally labeled A, B and C. The A input is the output of the voltage error amplifier which controls the average output voltage. The B input is the IAC signal which is a current from the input voltage and it is multiplied by the output of the voltage error amplifier to provide the current shape and amplitude needed to program the current loop. The C input is the divider input and it is the feed forward voltage that comes through the squarer. This input is proportional to the square of the average input voltage and it adjusts the gain of the multiplier to keep the gain of the voltage control loop constant. This is the secret to achieving a wide bandwidth control loop over a wide input voltage range. The squaring circuit takes its input from the VCC pin so the bias voltage for the UC3853 must be proportional to the input voltage for this feature to work properly.

The voltage error amplifier in the UC3853 is a transconductance amplifier and it has both a high

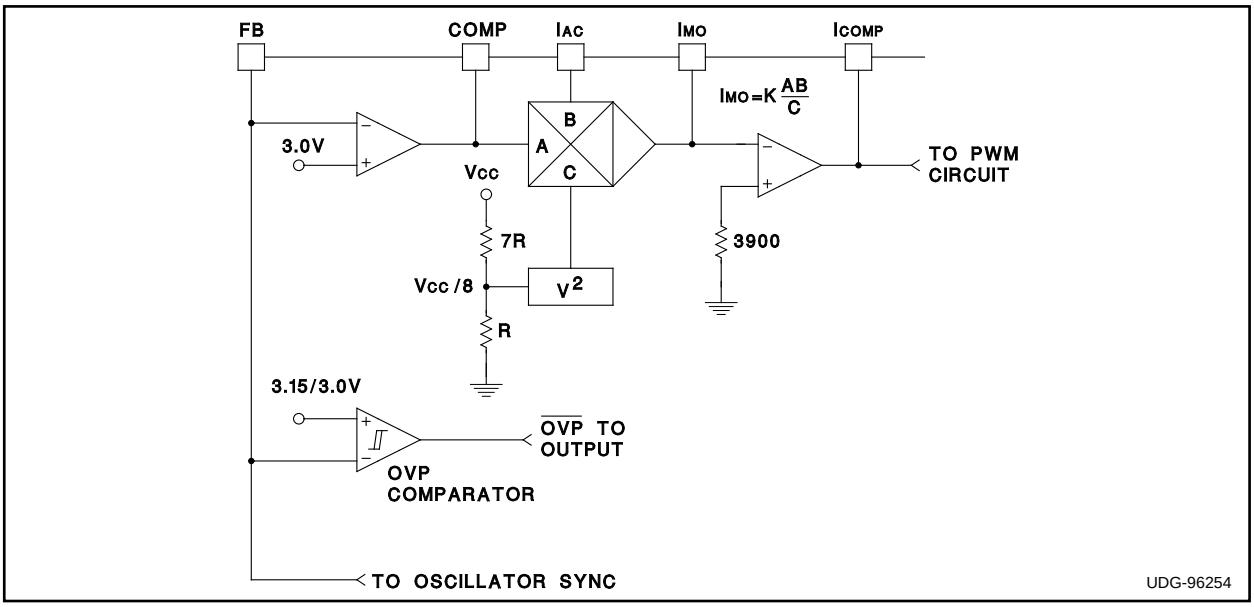

Figure 5. UC3853 Error Amplifiers, OVP Comparator and Multiplier, Divider, Squarer

input impedance and a high output impedance, which is a controlled current source output rather than the usual low impedance voltage source output. The gain of a transconductance amplifier is not given by the ratio of volts out to volts in. Instead it is given by the ratio of amperes out to volts in, which is a transconductance (the inverse of a resistance) and has the units of Siemens. The transconductance is a gain in this case and is often denoted by the symbol G_M. The gain of a transconductance amplifier can be changed into a voltage ratio by multiplying the transconductance gain by the load resistance. Hence, the voltage gain is set by an RC network to ground from the output of the amplifier. This allows the gain and frequency response of the amplifier to be determined by the load impedance without any components connected from the output of the amplifier to the input.

A transconductance amplifier was chosen to allow three functions to be combined on the FB pin. The oscillator sync input and the overvoltage comparator share the same input pin as the error amplifier so if a feedback network were connected around the amplifier the overvoltage comparator would be inaccurate. Since both the transconductance amplifier and the overvoltage comparator require only a simple voltage divider at their inputs for proper operation they can be combined into a single pin. The non-inverting input of the voltage amplifier is connected to a 3.0V DC reference which is the reference for the output voltage. The overvoltage comparator turns the output of the UC3853 off when the voltage at the FB pin exceeds 3.15V. The output turns back on when the voltage at the FB pin comes back to 3.0V.

BOOST PFC POWER STAGE DESIGN WITH THE UC3853

The circuit for a boost PFC is shown in Figure 6. The reference designators for the parts on the schematic match those in U-134 where the functions of the parts are the same. In all cases the reference designators are appropriate for the function of the device. A 100W boost power factor corrector is used as an example of the design process and this is the circuit that is shown in Figure 6. A table is provided at the end of this Application Note that extends the design over the range of 25W to 200W. The control circuits are the same whether at 25W or at 200W. The values of the control circuit components change only if the choices for circuit performance are different from those made here. The following design process allows the design to be modified to suit a wide variety of applications.

The design of a boost PFC begins with the specification for the system performance. The minimum and maximum input line voltages, the maximum output power, and the line frequency range must be specified. For the example circuit the specifications are:

- Maximum power output: 100 Watts
- Input line voltage range: 80-270VAC
- Line frequency range: 47-65Hz

The input line voltage and frequency range are a “universal” input range and allow this power factor corrector to operate from power lines anywhere in the world without switches or other adjustments.

The output voltage needs to be at least 5% higher than the peak voltage of the highest input line voltage. The peak of a 270VAC line will be about 380V

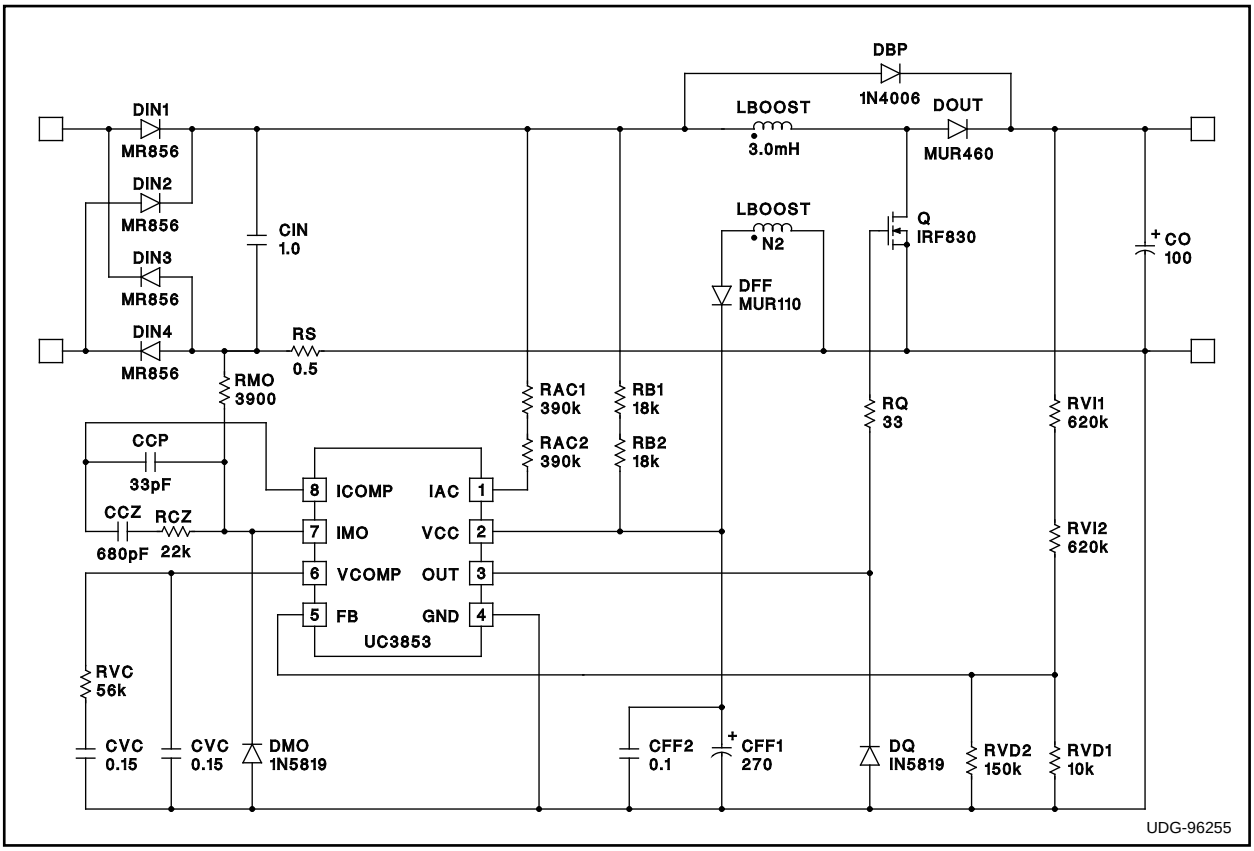

Figure 6. Schematic of a Boost Power Factor Corrector Using the UC3853

so 400V is chosen as the DC output voltage.

The switching frequency is an important consideration in the design process and the switching frequency is internally fixed in the UC3853 at 75kHz nominal and may be synchronized to an external 100kHz oscillator.

INDUCTOR SELECTION

The peak current that the inductor must carry is the peak line current at the lowest input voltage plus the peak high frequency ripple current. The peak line current is given by the following equation:

$$I_{LINEpk} = \frac{\sqrt{2} \bullet P}{V_{INmin}}$$

Where P is the maximum input power to the converter. Generally, using the output power is sufficiently accurate for this calculation since the efficiency of the converter should be greater than 90%. If greater accuracy in the design process is required, the design may be completed, the efficiency calculated and then the design process may be iterated using the calculated value for efficiency. For the example converter, the output power is 100W and V_{INmin} is 80VAC so I_{LINEpk} is 1.77A.

The high frequency ripple current, ΔI, must be kept reasonably small and is usually in the range of 15% to 25% of the peak line current given above. If the ripple current is too high the AC input filters required to filter out this noise become larger. If the ripple current is too low the value of the inductance is too large and the cusp distortion on the leading edge of the waveform will be large and the power factor will be low. For the example converter, the ripple current, ΔI, is chosen to be 20% of the peak line current or about 0.35A peak-to-peak. The peak current in the inductor, I_{Lpk}, is the sum of the peak line current and half of the peak-to-peak ripple current or 1.95A for the example converter.

The value of the inductor is determined by the peak current at low input line voltage, the duty factor, D, at that input voltage and the switching frequency. This value of the duty factor is given by the following equation:

$$D = \frac{V_O - \sqrt{2} \bullet V_{INmin}}{V_O}$$

Where V_{INmin} is the minimum RMS input line voltage and V_O is the DC output voltage. For the example converter V_{INmin} is 80V and V_O is 400V so D is 0.72.

The value of the inductor is given by the following equation:

$$L = \frac{\sqrt{2} \bullet V_{INmin} \bullet D}{\Delta I \bullet f_S}$$

Where V_{INmin} is the minimum RMS input voltage and D is given from the equation above. The switching frequency is fs and ΔI is the maximum peak-to-peak ripple current. For the example converter V_{IN} is 80V, D is 0.72, fs is 75kHz and ΔI is 0.35A peak-to-peak as determined above. This gives an inductance of 3.1mH. A value of 3.0mH nominal will be used.

Note that the ripple current changes with input voltage so it varies as the line voltage goes through its cycle. Under normal operation the ripple current can be significantly greater than the 20% specified here. The maximum ripple current occurs when the momentary value of the input voltage equals half the DC output voltage which corresponds to 50% duty ratio.

OUTPUT CAPACITOR SELECTION

C_O, the output capacitor generally falls in the range of 1 to 2µF per watt for typical 400V output applications. Since low cost is one of the targets of this converter, 1µF/W is chosen and thus a 100µF capacitor will be used for C_O. There are many factors that influence the value of the output capacitor. The output voltage hold-up time, the output ripple voltage, the loop transient response and the input current third harmonic distortion are all dependent to some degree on the value of the output capacitor and, in all cases except cost, a larger value of the output capacitance results in better performance. Nevertheless, a reasonable compromise can be reached with the 1µF/W value.

All power factor correction circuits have a large ripple current on their output at the second harmonic of the line current as highlighted in U-134. As the output capacitor becomes smaller, the output ripple voltage due to the second harmonic ripple current increases and the bandwidth of the voltage loop must be made smaller to keep the same level of distortion in the input current. A 1% second harmonic ripple voltage at the output of the voltage error amplifier becomes 0.5% third harmonic distortion of the input current. The only ways to reduce this source of distortion are to (1) increase the size of the output capacitor and (2) reduce the gain of the error amplifier at the second harmonic frequency by reducing the amplifier bandwidth. Reducing the loop bandwidth slows the transient response and increases its deviation.

The output capacitor may need to be larger for other reasons. If hold-up time is required, the capacitor may need to be larger than 1µF/W. The following equation may be used to calculate the size of the capacitor for a given hold-up time, power output and voltage change.

$$C_O = \frac{2 \bullet P \bullet \Delta t}{V_O^2 - V_{Omin}^2}$$

Where P is the rated power of the converter, Δt is the required hold-up time, V_O is the DC output voltage of the converter and V_{Omin} is the voltage to which the output decays at the end of the hold-up time. For the example converter, 100µF gives about 19 milliseconds of hold-up time for a 50V change in V_O or 35 milliseconds of hold-up for a 100V change.

CURRENT SENSE RESISTOR

R_S, the current sense resistor, is selected to provide 1.0V at the maximum current expected in the inductor. I_{LINEpk} plus half the peak-to-peak ripple current is the peak current through the inductor and was calculated above. The value of the current sense resistor is found from: $1.0V/I_{Lpk}$. For the example converter the peak current in the inductor is 2.0A maximum so the value of the sense resistor is 0.5Ω.

SWITCHES AND DIODES

The power switch must have a low R_{DSon} rating and a peak voltage rating greater than the output voltage of the converter with some margin for transient overshoot, ripple voltage on the output and appropriate levels of derating. A low R_{DSon} of the power switch will result in lower conduction losses but these devices also have high gate capacitances and may therefore have longer turn-on times, resulting in greater overall switch power dissipation. There is an optimum size switch for each application although the optima is rather broad. Suggestions for switches for a variety of power levels are contained in the table at the end of this application note. These are by no means the only possibilities and are simply generic choices. For the example converter an IRF830 was chosen.

The output diode must be rated for the peak output current and must be an incredibly fast diode. A reverse recovery time below 100 nanoseconds is strongly recommended and faster is much better. The reverse recovery time of the diode has a direct effect on the power dissipation in the switch. The switch must conduct full output current at full output voltage from the time it turns on until the diode turns off. For the example converter this will be 400V at 2.0A for a peak power of 800W. If this lasts for 100nsec the average power will be 6.0W at a 75kHz switching frequency. If a 35nsec recovery

diode is used the average power will be 2.1W. There are many diodes available that meet the requirements of this application. The temperature rise of the diode must be kept below maximum for the worst case conditions as well. The reverse recovery time of the diode becomes larger as the temperature increases and this increases the power dissipation of the switching transistor. Heat sinking of the diode may be required to control the maximum temperature. For the example converter either an MUR460 or a BYM26C is used.

INPUT DIODES

The input diodes are not particularly critical. They must have a current rating sufficient for the maximum current at low line and they must be held to a reasonable temperature rise. Fast recovery types generally prove to be a bit less noisy than standard recovery types. Avalanche breakdown types work better with noisy power lines. The exact choice of input diodes depends on many such factors as well as the amount of filtering present on the AC side of the bridge. For the example converter, MR856 or BYW95C diodes are used. Both are fast recovery types.

C_{IN} is part of the input filter even though it is after the input diodes. The value must be chosen in conjunction with the input filter and must be kept reasonably small. This capacitor carries most of the ripple current from the inductor so it needs to be a film type capacitor with a substantial high frequency ripple current capability. At light loads C_{IN} can have a large effect on the distortion of the input current because it is after the input diodes. At these low currents, especially near the input voltage zero crossing, the capacitor stores enough energy to maintain the output current and the input diodes turn off, thus introducing distortion into the input current. For the example converter, a 1.0µF capacitor was chosen to give less than 1V peak-to-peak ripple voltage at the switching frequency with 100W output.

CONTROL CIRCUIT DESIGN WITH THE UC3853

The heart of the UC3853 is the multiplier and it is quite easy to set the parameters for proper operation. The equation for the multiplier is given below and, even though it looks complex, it is quite straight forward.

$$I_{MO} = \frac{I_{AC} \bullet (V_{COMP} - 1.5)}{K_M \bullet \left(\frac{V_{CC}}{8}\right)^2}$$

I_{MO} is the output current from the multiplier. I_{AC} is the programming current that comes from the input through R_{AC} and is proportional to the input voltage. It tells the current loop what to do to maintain an input current which is proportional to the input voltage. V_{COMP} is the output of the voltage error amplifier and is the other input to the multiplier. K_M is the gain constant of the multiplier and is given in the data sheet for the UC3853. V_{CC} is the supply voltage to the UC3853 and it is divided by eight internally and then squared in the squaring circuit. This forms the divider input to the multiplier and is used to keep the gain of the voltage loop constant so that the loop bandwidth may be kept large and thus have a relatively fast transient response.

I_{AC} must be programmed to have a maximum value of 500µA when the AC line voltage is at its peak. The voltage at the IAC pin is 2.0V so it introduces very little error into the current if this voltage is ignored. For the example converter the maximum input voltage is 270VAC and this has a peak value of about 380V. A 760kΩ resistor will give 500µA. Most resistors are only rated to 250V so two resistors will be needed in series. The closest standard value is 390kΩ so this value is chosen for both R_{AC1} and R_{AC2}.

CURRENT LOOP COMPENSATION

The peak value of I_{MO} is about 250µA with the values of R_{AC} given above. If R_{MO} is made 3.9kΩ, the peak value of voltage across R_S will be 1.0V. This value of R_{MO} also matches the 3.9kΩ resistor internal to the UC3853 which is connected to ground from the non-inverting input of the current error amplifier. These two values provide the correct balance for the DC bias currents into the amplifier and give the correct input offset voltage. If the offset voltage is in the wrong direction the current loop could latch at zero output.

The PFC input current must track the current programming signal (I_{MO}) from the multiplier very closely to achieve a low distortion input current. Accurate tracking requires high gain in the current loop to minimize the errors. For the current loop to be stable, the frequency at which the gain of the loop is equal to one must be less than one thirds of the switching frequency and the gain must roll off with a single pole slope. The boost power stage has a single pole due to the main inductor and the current sense resistor. This L/R pole creates a stable loop with a fixed gain, wide bandwidth error amplifier. These two requirements can be accommodated by using pole zero compensation around the error amplifier. Pole zero compensation has high

gain at low frequencies and flat gain at high frequencies so that the input current tracks the programming signal accurately and is also stable at high frequencies. This is the essence of average current mode control and it is necessary for a low distortion PFC.

A block diagram of the current loop is shown in Figure 7. A bit of topological manipulation has been done to put the loop into this form. The switch, output diode and output capacitor have been moved to the other side of the inductor and lumped into the voltage source V_S, which is now a controlled source and is controlled by the duty factor d from the PWM circuit in the UC3853. The reason for showing the circuit model in this form is to highlight the source of the L/R pole in the current loop and to show how the pole zero compensation of the current error amplifier affects the loop.

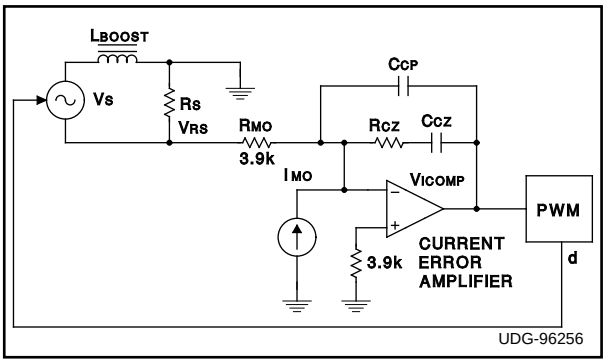

Figure 7. Simplified Block Diagram of a Boost PFC Current Loop

Figure 8 shows the control to output current gain of the current loop and the current amplifier compensation as well as the complete current loop gain. The graph ignores the double pole occurring at the switching frequency and the aliasing effects of the sampling system. The graph is based on a linear model to promote understanding of the loop dynamics and the compensation methods employed. The lower curve is the control to current transfer function of the boost stage and the pulse width modulator (V_{RS}/V_{Icomp}). The gain is moderate at low frequencies and shows the L/R corner frequency and single pole roll off up to half of the switching frequency. The pole zero compensation of the current error amplifier is shown along with the complete current loop response.

The design of the pole-zero compensation for the current loop begins with the equation for the control to output transfer function of the boost power stage. The control variables for this transfer function are the output of the current amplifier, V_{Icomp}, and the voltage across the current sense resistor, V_{RS}. The equation is:

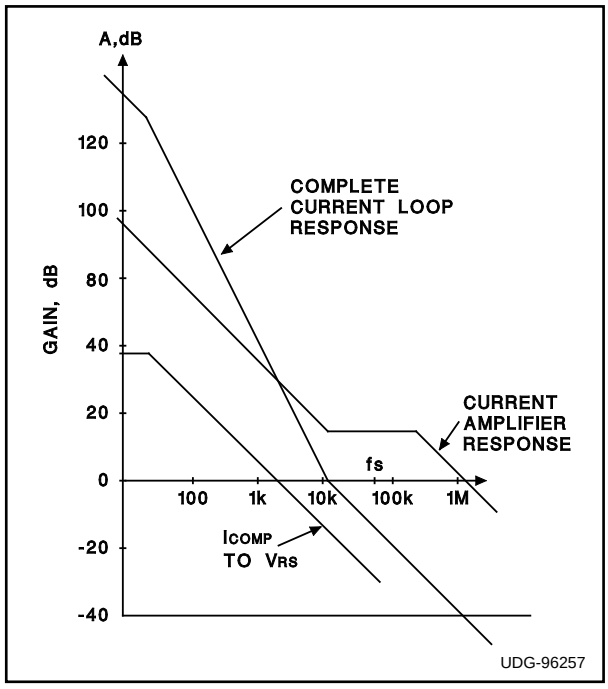

Figure 8. Current Loop Transfer Functions for 100W Example Boost Converter

$$\frac{V_{RS}}{V_{Icomp}} = \frac{V_O \bullet R_S}{V_{OSC} \bullet (R_S + X_L)}$$

Where V_O is the DC output voltage of the converter, R_S is the sense resistor value, V_{OSC} is the peak-to-peak amplitude of the oscillator ramp voltage and X_L is the impedance of the boost inductor ($2 \bullet \pi \bullet f \bullet L$).

The current loop is a very wide bandwidth loop and stability is achieved by adjusting the current amplifier gain so that the natural roll off from the L/R_S pole of the boost stage crosses 0dB gain at the appropriate frequency. Because the bandwidth is large, slope compensation must be added to the loop to compensate for the double pole which occurs at the switching frequency. In average current mode control the slope compensation is provided by the oscillator ramp, which is one of the inputs to the PWM comparator. If the gain of the error amplifier is correct, the amplitude of the oscillator ramp will introduce the correct amount of slope compensation. The procedure is to match the down slope of the inductor current with the slope of the oscillator ramp. That gives the correct value for the loop gain at the switching frequency to maintain stability. A capacitor is then added in series with the resistor for pole-zero compensation which gives the maximum amplifier gain at low frequencies.

The maximum down slope of the inductor current occurs when the input voltage is near zero. The equation for the inductor yields the slope of the current.

$$\frac{dI}{dt} = \frac{V_O}{L}$$

Where dI/dt is the slope of the inductor current in amperes per second, V_O is the DC output voltage of the converter and L is the value of the boost inductance. This current flows through the sense resistor and becomes a voltage so the equation is modified as follows:

$$\frac{dV}{dt} = \frac{V_O}{L} \bullet R_S$$

Where R_S is the sense resistor value. For the example converter the output voltage is 400VDC and the inductance is 3.0mH so the dI/dt is 0.133A/µsec, and R_S is 0.5Ω so dV/dt is 0.066V/µsec.

The oscillator in the UC3853 has a peak-to-peak amplitude of 5.0V and the period is 13.3µsec so the slope is 0.375V/µsec (the slope does not change with synchronization). The gain of the current amplifier at the switching frequency is determined by the ratio of the oscillator voltage slope divided by the current slope. The gain of the current amplifier at the switching frequency is the ratio of R_{CZ} to R_{MO}. For the example converter the current slope is 0.066V/µsec and the oscillator slope is 0.375V/µsec so the gain is 5.625. R_{MO} is 3.9kΩ so R_{CZ} is 22kΩ.

The value of the capacitor C_{CZ}, which introduces a zero into the current error amplifier response, is set by the current loop crossover frequency. The zero must be at or below that frequency to maintain the phase margin of the current loop. The equation for f_{CI} given below is simplified somewhat but is accurate over this frequency range.

$$f_{CI} = \frac{V_O \bullet R_S \bullet R_{CZ}}{2 \bullet \pi \bullet L \bullet R_{MO} \bullet V_{OSC}}$$

Where V_O is the DC output voltage of the converter, R_S is the value of the current sense resistor and R_{CZ} is the current amplifier feedback resistance determined above. V_{OSC} is the peak-to-peak oscillator ramp voltage, L is the value of the boost inductor and R_{MO} is the current amplifier input resistance. For the example converter, V_O is 400VDC, R_S is 0.5Ω, R_{CZ} is 22kΩ, V_{OSC} is 5V, L is 3.0mH and R_{MO} is 3.9kΩ resulting in an f_{CI} of 12kHz.

C_{CZ} must have an impedance equal to or less than R_{CZ} at f_{CI}. This is easily found from:

$$C_{CZ} = \frac{1}{2 \bullet \pi \bullet f_{CI} \bullet R_{CZ}}$$

For the example converter, f_{CI} is 12kHz and R_{CZ} is 22kΩ so C_{CZ} must be greater than 600pF. A 680pF capacitor is chosen to give a bit of extra phase margin.

C_{CP} is included to suppress high frequency noise in the current amplifier and it must have an impedance of at least 2 • R_{CZ} at the switching frequency. Substituting f_S for f_{CI} into the equation above gives C_{CP}.

$$C_{CP} = \frac{1}{2 \bullet \pi \bullet f_S \bullet 2 \bullet R_{CZ}}$$

For the example converter C_{CP} must be less than 50pF. A value of 33pF is chosen to accommodate a 100kHz synchronization frequency.

A hard current limit is not necessary to protect the switch in an average current mode controlled system. The gain of the current amplifier is set so that the maximum change of current in the inductor results in at most a 20% change of the current during one clock period. This makes it impossible for the control circuit to cause the switch to be on long enough to enter an overcurrent condition. The current programming signal is also limited so the inductor current can not exceed this value.

HARMONIC DISTORTION BUDGET

Once the current loop is stable the next two tasks are setting the voltage loop compensation and the feedforward compensation. Both of these are determined by the amount of harmonic distortion each contributes to the input current. The voltage loop contributes 0.5% third harmonic distortion to the input current for each 1% ripple voltage at the output of the error amplifier. The feedforward compensation comes from the voltage supplied to the UC3853 and each 1% ripple on this input contributes 1% third harmonic distortion to the input current.

The choice of input current harmonic distortion limit and the allocation of this distortion to the two major sources is somewhat arbitrary. For the example converter, the THD will be limited to 5% of the input current. The voltage loop is allowed to contribute 2% of the distortion and the feedforward voltage is allowed to contribute 2% of the distortion. The remaining 1% will be allocated to other sources such as cusp distortion and possible multiplier nonlinearity. 5% THD gives a power factor of 0.99875.

VOLTAGE LOOP COMPENSATION

A simplified block diagram of the voltage loop is shown in Figure 9. Average current mode control turns the power stage of the boost converter into a voltage controlled current source driving a capacitor, C_O, in parallel with the load resistance. The cur-

rent loop therefore becomes a transconductance amplifier with a voltage input and current output. The voltage gain of the current loop is given by $G_{CL} \bullet Z_L$ where G_{CL} is the transconductance of the current loop and Z_L is the parallel combination of C_O and R_L, the load resistance. The frequency response of the current loop has a DC gain given by $G_{CL} \bullet R_L$ and a single pole roll off due to C_O and R_L within the frequency range of interest. Theoretically, if the voltage loop is closed around the current loop with a fixed gain error amplifier, the voltage loop will be stable because there is only a single pole from C_O and R_L within the loop. As the gain of the amplifier increases, the bandwidth of the voltage loop also increases. Although this solution is very appealing, it is not feasible with the UC3853 because the limited current capability of the voltage error amplifier. Therefore, the error amplifier compensation will have a zero below and a pole at the crossover frequency of the voltage loop.

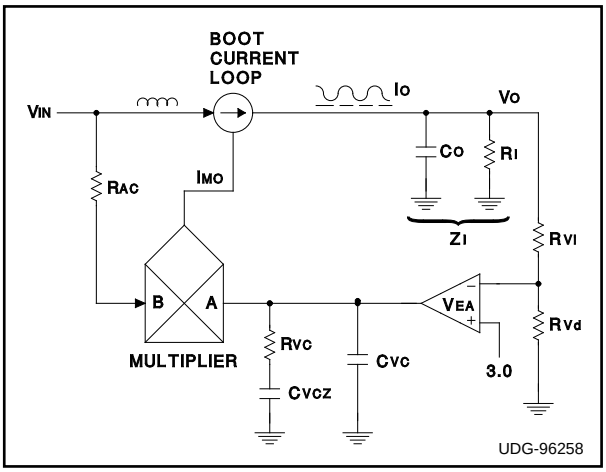

Figure 9. Simplified Block Diagram of a Boost PFC Voltage Loop

The multiplier in the voltage loop adds the current programming signal from the line frequency and it acts like a switching frequency. Therefore the bandwidth of the voltage loop must be kept below $(2 \bullet f_L/\pi)$ to maintain voltage loop stability where f_L is the line frequency. The gain of the error amplifier needs to be high to maintain wide bandwidth in the voltage loop and thus fast transient response but if it is too high the loop will go unstable due to the line frequency introduced by the programming signal in the multiplier. If the gain of the amplifier in the loop is set with a fixed gain to give maximum bandwidth, the DC gain of the loop is reasonable and the output voltage regulation is within a percent or two of the set point.

The relatively wide bandwidth of the loop gives good transient response but also gives little attenuation of the second harmonic ripple voltage on the output capacitor. This voltage modulates the input current so the harmonic distortion of the input current will be too high. Reducing the harmonic distortion requires reducing the gain of the loop at the second harmonic of the power line frequency, which is the ripple voltage frequency on the output capacitor. The bandwidth of the loop must also be kept as high as possible to maintain good transient response. If the loop is closed with an error amplifier having an extra pole just after the unity gain crossover frequency, it is possible to reduce the harmonic distortion and still maintain good loop bandwidth and adequate phase margin.

Figure 10 is a Bode diagram of the resulting loop response. The loop response has a pole at low frequency due to the load resistance and the output capacitance and then rolls off smoothly with a first order slope due to the output capacitor. Just after the gain of the loop crosses 0dB at f_{VI}, a second pole takes the slope to a second order roll off and this reduces the loop gain to the required level at the second harmonic of the line frequency. For greater DC regulation of the output voltage and because of the requirements of the voltage error amplifier on the UC3853, a zero is added to the loop at low frequencies to compensate for the load resistance and output capacitance pole.

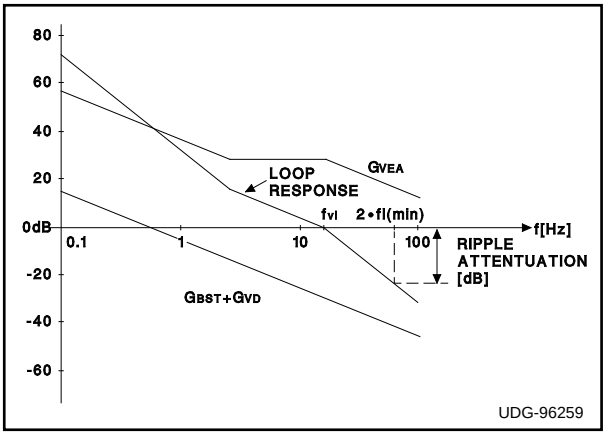

Figure 10. Transfer Functions of Voltage Loop

The design of the voltage loop compensation begins at the output capacitor. The voltage loop compensation reduces the amplitude of the ripple voltage from the output capacitor to a level, at the output of the voltage error amplifier, which is consistent with the harmonic distortion specification. The amount of ripple voltage on the output capacitor, C_O, is given by the following equation.

$$\Delta V_{Opk} = \frac{P}{2 \bullet \pi \bullet 2 \bullet f_{Lmin} \bullet C_O \bullet V_O}$$

Where P is the maximum input power of the converter. Use of the input power in place of the output power is a reasonable compromise since the efficiency of the converter is high. The lowest power

line frequency is f_{Lmin}, the output capacitor value is C_O and V_O is the DC output voltage. For the example converter, P (approximately P_{OUT}) is 100W, f_{Lmin} is 47Hz, C_O is 100µF and V_O is 400VDC. ΔV_{Opk} is therefore 4.2Vpk. Note that this is half the peak-to-peak value. Mathematically, this is the amplitude of the ripple voltage vector. At low line frequencies the ripple voltage is larger as is the gain of the error amplifier because of the loop compensation requirements. If performance is to be maintained over the range of line frequencies, then the lowest frequency must be used for the design.

The gain of the voltage error amplifier and the voltage divider preceding it are determined by the harmonic distortion budget for the voltage loop and the amount of ripple voltage on the output capacitor. The amount of ripple voltage allowed on the output of the voltage error amplifier is equal to twice the percentage of the distortion. Each 1% of second harmonic ripple voltage on the output of the amplifier results in 0.5% third harmonic current on the input. The %ripple on the output of the voltage error must be translated into an absolute voltage to find the gain of the voltage error amplifier and the voltage divider at the second harmonic of the line frequency. The %ripple is multiplied by the range of the output voltage (ΔV_{COMP}) to get the amplitude of the ripple voltage on the output of the amplifier. This is divided by the amplitude of the ripple voltage on the output capacitor to give the combined gain of the voltage error amplifier and the voltage divider. The equation for the gain is:

$$G_V = \frac{\Delta V_{COMP} \bullet \%ripple}{\Delta V_{Opk}}$$

Where G_V is the gain of the voltage divider and the voltage error amplifier, ΔV_{COMP} is the range of the voltage error amplifier output, %ripple is the percentage of ripple voltage allowed in the output of the voltage error amplifier and ΔV_{Opk} is given previously. For the example converter, ΔV_{COMP} is actually the active range of the input to the multiplier rather than the output range of the amplifier. On the UC3853 the active input range of the multiplier is between 1.5V and 6.0V so ΔV_{COMP} is 4.5V. The percent THD of the input current allowed from the voltage loop according to the harmonic distortion budget is 2% which results in 4% ripple voltage at the output of the voltage error amplifier. The numeric value of 0.04 must be used in the equation. The value of ΔV_{Opk} is 4.2V. Therefore:

$$G_V = \frac{4.5 \bullet 0.04}{4.2} = 0.043$$

The voltage divider is composed of R_{VI} and R_{VD} and is determined by the ratio of the DC output voltage to the internal reference voltage in the UC3853, which is 3.0V. The impedance of the voltage divider is somewhat arbitrary. For the example converter the output voltage is over 250V so two resistors are used in series to get the necessary voltage rating. 1.24MΩ is chosen as the divider impedance so two 620kΩ resistors are used for R_{VI}. R_{VD} is determined from the voltage divider equation and the value is just below 10kΩ so a 10kΩ resistor is used with a 150kΩ resistor in parallel. The gain of the voltage divider is given by the following equation:

$$G_{VD} = \frac{R_{VD}}{R_{VD} + R_{VI}}$$

The gain of the voltage divider, G_{VD}, is 0.0075 in the example. The gain of the divider and the voltage amplifier together must be 0.043. The gain of the amplifier at twice the line frequency (low line frequency is 47Hz) must be 5.7 for the example converter.

The gain of a transconductance amplifier is given by $A = G_M \bullet Z_A$. Where A is the voltage gain of the amplifier, G_M is the transconductance of the amplifier and Z_A is the load impedance from the V_{COMP} pin to ground. The transconductance of the amplifier in the UC3853 is 485µmhos. The gain needed for this application is 5.7, so the load impedance is 11.75kΩ. At the second harmonic of the line frequency, the gain of the amplifier is determined by C_{VC}, the voltage compensation capacitor. For the example converter, a capacitor with an impedance of 11.75kΩ at 94Hz has a value of 0.15µF and this is the value used.

The value of R_{VC} is found by extrapolating from the second harmonic frequency back to find the frequency at which the gain of the voltage loop is unity, f_{VI}. R_{VC} is then found by writing the equation for the gain of the loop, setting it to unity and solving the resulting equation for R_{VC}. The loop equation is the product of the gain of the current loop and load impedance, G_{BST}, the gain of the voltage amplifier, G_{VEA}, and the voltage divider, G_{VD}.

The gain of the boost stage is given by the following equation:

$$G_{BST} = \frac{P \bullet X_{CO}}{\Delta V_{COMP} \bullet V_O}$$

Where P is the input power and is here taken to be the output power because of the assumption of high efficiency. X_{CO} is the impedance of the output capacitor and varies with frequency. ΔV_{COMP} is the range of the voltage error amplifier output and is equal to 4.5V on the UC3853. V_O is the DC output voltage. By using the output power ($V_O \bullet I_O$) in the equation, all of the terms that are associated with the multiplier and divider drop out of the equation.

The gain of the voltage divider, G_{VD}, is given above. The gain of the transconductance amplifier and its load are given by the following:

$$G_{VEA} = G_M \bullet X_{CVC}$$

Where G_M is the transconductance of the amplifier and X_{CVC} is the impedance of the compensation capacitor C_{VC}.

Finally, the equation for the loop can be written from these equations as:

$$G_V = \frac{P \bullet X_{CO} \bullet G_M \bullet X_{CVC} \bullet G_{VD}}{\Delta V_{COMP} \bullet V_O}$$

By setting $G_V = 1$ the equation can be solved for frequency since all other variables are known at this point. Note that there are two terms in the equation which vary with frequency, X_{CO} and X_{CVC}. The loop has a second order roll off at this point so the equation is solved for the square of the frequency. The unity gain crossover frequency, f_{VI}, is found from the following equation.

$$f_{VI}^2 = \frac{P \bullet G_M \bullet G_{VD}}{(2 \bullet \pi)^2 \bullet C_O \bullet C_{VC} \bullet \Delta V_{COMP} \bullet V_O}$$

For the example converter f_{VI} is 18.6Hz. The value of R_{VC}, which is what we have been trying to determine all along, is equal to the impedance of C_{VC} at f_{VI}. For the example converter, this is 57kΩ, so a 56kΩ standard value resistor is chosen.

The last step is the addition of a low frequency zero in the feedback loop. It is accomplished by adding C_{VCZ} in series with R_{VC} as shown in the schematic. From an operational standpoint, the effect of C_{VCZ} is to double the peak-to-peak variation of the output voltage during a step load transient. The overvoltage protection circuit built into the UC3853 will prevent the output voltage from exceeding the maximum value by turning the switch off until the output voltage is back within range. The undervoltage transient caused by a step load change will be unaffected.

The value of C_{VCZ} is not especially critical. However, since it adds both a pole and an zero to the loop gain, the zero must be far enough away in frequency from the C_{VC} and R_{VC} pole so that it does not contribute extra phase shift at the unity gain frequency, f_{VI}. This requires that the zero be at least two octaves below f_{VI}. For the example converter, the zero has been placed almost a full decade below f_{VI} and the value of C_{VCZ} is chosen as 1.0µF.

THE FEEDFORWARD VOLTAGE AND STARTUP CIRCUIT

The UC3853 makes use of a divider and squaring circuit to compensate the gain of the voltage loop for changes of the input voltage as shown in Figure 5. The input to the squarer and divider is the supply voltage to the UC3853 and is called V_{FF}. The function of the supply voltage, besides powering the chip, is to feed-forward information about the input voltage to the voltage loop. This means that V_{FF} must be proportional to the average value of the input voltage and must also have low ripple voltage because 1% ripple on this voltage will create 1% harmonic distortion on the input current.

The V_{FF} input is generated by a winding on the boost inductor that operates like a transformer. When the switch is turned on, the voltage across the inductor is equal to the input voltage. This voltage is tapped off by using an additional winding on the inductor to supply the control circuits. The current drain of the control circuits, I_{CC}, is typically about 15mA of which 10mA are allocated to the UC3853 and 5mA are allocated to the MOSFET gate drive current. These currents are constant and do not change appreciably with a change of the supply voltage.

The supply voltage range of the UC3853 is great enough to cover a 3:1 input voltage range. To provide the best utilization of the V_{FF} programming range the supply voltage to the UC3853 should be set to provide 10.5V when the input voltage is at low line. If a narrower range is being used for the input voltage than is used for this example, it may be desirable to set the minimum voltage slightly higher, in the range of 12V to 15V, to provide more voltage for the gate drive at lower line voltages and thus lower R_{DSon}. For the example converter, a turns ratio of 10:1 on the inductor will provide the correct value of V_{FF}. The minimum voltage is about 10.5V, with an input line voltage of 80VAC, after all of the diode drops have been taken into account. The UVLO threshold for turning the UC3853 off is 9.5V so a 10.5V minimum value of V_{FF} leaves some margin in the design for component variation.

The diode D_{FF} must block 80V, carry an average current of 15mA for the example converter and have a very fast recovery time. Small 100V diodes, such as BYD71B or MUR110 are suitable devices for this application.

The amount of harmonic distortion allocated to the V_{FF} input of the UC3853 is 2%, so the ripple voltage must be held to 2% of the minimum value of V_{FF}. For the example converter, the minimum voltage is 10.5V so the allowable ripple voltage is 0.21V. This is not the peak-to-peak value of the ripple but is the peak value of the second harmonic of the line frequency. The peak-to-peak ripple voltage, ΔV_{FF}, is this value multiplied by π. For the example converter, ΔV_{FF} is therefore 0.66V peak-to-peak.

The value of C_{FF} can be found from the equation for a capacitor and the current drain of the control circuits, I_{CC}.

$$C_{FF} = \frac{I_{CC}}{\Delta V_{FF} \bullet 2 \bullet f_{Lmin}}$$

Where C_{FF} is the value of the V_{FF} bypass capacitor, I_{CC} is the current drain of the control circuits, ΔV_{FF} is the peak-to-peak ripple voltage on V_{FF} and f_{Lmin} is the minimum line frequency. For the example converter the value is 240µF. A standard value of 270µF is chosen and it is bypassed with a 0.1µF ceramic capacitor.

This value for C_{FF} also gives sufficient time to start the circuit since one half cycle of the input line frequency is needed to reach full operation. The turn-on threshold of the UC3853 is 11.5V and the turn-off threshold is 9.5V so there is more than sufficient energy stored to begin circuit operation.

$$\Delta t = \frac{C_{FF} \bullet (V_{TN} - V_{TF})}{I_{CC}}$$

Where Δt is the amount of time available for start-up, C_{FF} is the capacitance on V_{FF}, V_{TN} is the turn on threshold of the UC3853 (11.5V), V_{TF} is the turn off threshold (9.5V), and I_{CC} is the current drain of the control circuits. For the example converter Δt is 36 milliseconds.

Startup of the UC3853 is accomplished by charging V_{FF} to 11.5V through R_B. The value of R_B must be small enough to provide a reasonably short turn-on delay after power is applied and yet large enough to keep power dissipation low. The current through R_B at V_{INmin} must also be greater than the UC3853 startup current (500µA). For the example converter a 1 second delay at turn-on requires a bias current of approximately 3mA from the low input line voltage. The equivalent resistance is about 36kΩ. This resistance needs to be split into two equal resistors since the peak input voltage will exceed 250V so two 18kΩ resistors are used. At high line this gives about 6.8mA of bias current to V_{FF}. This is less than the current required by the UC3853 so this value of R_B is acceptable. If the current at high line were too great, V_{FF} would not accurately reflect the input voltage and performance would suffer. A larger value of R_B resulting in a longer turn-on delay is required in that case. At high line each of the 18kΩ resistors dissipates 0.82W. A 2W rating is specified.

The gate drive voltage of the UC3853 is limited to 15V by an internal clamp. This allows V_{FF} to change without causing the gate voltage to exceed the rating of the MOSFET. The UC3853 is designed to drive moderate size MOSFET switches, and the gate drive current is limited to 500mA(pk). This is more than sufficient to obtain the fast rise and fall times needed for high efficiency. R_Q is the resistor in series with the gate of the MOSFET. Its value of 33Ω is chosen to limit the peak gate current to about 350mA under normal operating conditions. In addition, this is the minimum value for which D_Q, the gate drive clamp, is NOT required under most circumstances. In general, if R_Q is made small there will not be sufficient damping of the resonance of the parasitic circuit inductances with the MOSFET gate capacitance, so the output of the UC3853 could be drawn below ground. Keeping R_Q in the range of 30Ω to 60Ω prevents this, eliminates the need for D_Q and at the same time provides ample output current for fast rise and fall times on the drain of the MOSFET. It is wise practice to leave room for D_Q on the circuit board until it can be verified in the laboratory that it is not needed.

OVER CURRENT PROTECTION

The boost converter is inherently unprotected against any overload situation. Because the switch is connected in parallel with the input source, the DC current path through the inductor, diode and the load impedance (parallel combination of C_O and R_L) can not be interrupted. The result is practically unlimited current flowing from the input to the output of the converter when the output voltage falls below the input voltage. This happens every instance when power is being applied to the converter at startup and when the load requires more power than the circuit was originally designed for. Unfortunately, these situations can not be avoided, but there are certain measures which can protect the circuit from a catastrophic failure.

The diode, D_{BP} in Figure 6 provides protection for the boost inductor and for the output rectifier, D_{OUT}. During the initial charging of the output capacitor at startup and in case of an overload, a high surge current flows from the input to the output of the converter. This high peak current would flow through the boost inductor and the very sensitive high speed epitaxial diode used for rectification. This high surge current can saturate the inductor and damage the diode causing a disastrous failure eventually. D_{BP} prevents the high current flowing in the inductor-diode path by providing a lower impedance direct path between the input and the output. The additional benefit of the D_{BP} diode is the protection against input voltage transients. When other high power loads are connected to the same distribution branch of the power line, their turn off generates huge inductive spikes appearing at the input of the power factor corrector power supply. This can cause the input voltage of the boost converter to be higher than its output voltage even under normal operating conditions. The voltage

spikes impose an increased voltage stress on the input rectifier diodes and it might cause the boost inductor to saturate depending on the duration and the amplitude of the line transient. The addition of the D_{BP} diode clamps the input voltage to the output capacitor voltage which will also absorb the transient energies without passing high current through the boost inductor and rectifier diode.

In normal circumstances D_{BP} has no effect on the circuit operation. Note that the diode D_{BP} can not prevent the circuit from developing high currents from the input to the output. It simply provides a safe passage for the high current to pass through the circuit. Once the high current is flowing, it has to go through the current sense resistor, R_S. Higher than nominal currents will develop negative voltage across R_S in excess of the 1V maximum value used in the design. Since the I_{MO} current is limited to 0.5 • I_{AC}, the IMO pin of the UC3853 will be pulled below ground. This could present a problem for the integrated circuit because of reverse biasing the substrate. When the IMO pin is pulled 0.3V below ground (to -0.3V), the OUT pin goes high turning on the main switch of the boost converter. Since the current can not be limited, the only way to avoid the parasitic turn on of the output is to limit the negative voltage on the IMO pin of the IC. It is accomplished by the Schottky diode, D_{MO} connected between the IMO pin of the UC3853 and circuit ground, as shown in Figure 6.

ABOUT SYNCHRONIZATION

Synchronization of the UC3853 oscillator requires a fast falling edge on the FB pin. The minimum requirements for the falling edge of the waveform are that it must have a slope of at least 20V/µsec and an amplitude of at least 1.0V. Faster fall times and greater amplitudes are strongly recommended. The amplitude of the sync signal must be kept below 3.0V so that the FB pin is not driven below ground. The sync signal must be capacitively coupled into the FB pin so that the DC feedback is not disturbed by the synchronization. The capacitor must be large enough so that it does not gain enough voltage during the pulse to trip the overvoltage comparator of the UC3853 on the rising edge of the sync waveform. These requirements are easily met with the circuit of Figure 11 as shown below.

In most applications the UC3853 will be synchronized to another PWM integrated circuit used to control the DC output voltage of the power supply. A few PWM integrated circuits, such as the UC3526A, have inverted pulse sync outputs and these can be interfaced to the UC3853 with just a small capacitor. Other PWM circuits have an output pulse which is positive and has a narrow pulse width. This signal needs to be inverted and conditioned to interface with the UC3853. If the pulse is more than 100nsec wide then the signal must be shortened as well. Some PWM integrated circuits do not have a sync output but these can still be synchronized with a little ingenuity and a few small parts.

A schematic of a generic sync circuit is shown in Figure 11. This circuit accepts a positive input pulse and provides the correct output pulse to the FB pin of the UC3853. The pulse is capacitively coupled to the FB pin through C_{SYNC}. The value of this capacitor is chosen so that the voltage change across it during a 2.5V pulse of 100 nanoseconds duration is about 100mV. This precludes the sync pulse having a significant effect on the UC3853 output voltage. If R_{VD} in Figure 6 is about 10kΩ then C_{SYNC} will be about 220pF. A larger value for C_{SYNC} may be used but the capacitor adds a pole to the feedback loop and the pole must be kept above the switching frequency. The voltage divider R_{SVD1} and R_{SVD2} reduce the effect of the pole by providing a compensating zero so their impedance must be relatively high. A value of 22kΩ was chosen to present a 10k impedance to the feedback network and thus keep the additional pole and zero relatively close together. The 5V source for the voltage divider is supplied from another PWM integrated circuit.

An NPN transistor is shown in Figure 11 to invert the input signal and drive the FB pin of the UC3853. Any fast general purpose small signal transistor will work in this application. The network chosen for the base of the transistor depends on the clock that it is being interfaced to. The base network shown in Figure 11 allows the circuit to work with a wide variety of inputs. C_{ST} and R_{ST} form a 100nsec time constant which will limit the width of the sync pulse output. The resistor R_{SB} and diode D_{SB} provide reset for the sync input time constant. A relatively fast rising edge on the input pulse is required for proper circuit operation.

As an example of synchronization, the sync circuit in Figure 11 may be used with the UC3525B by

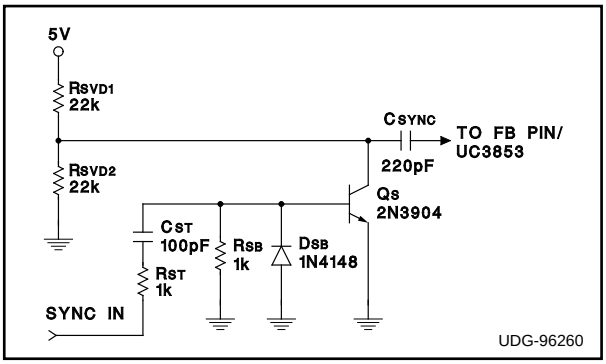

Figure 11. Synchronization Circuit for Positive Edge Sync Signals

connecting the sync circuit input to the CLOCK output. The UC3525B has a positive going clock pulse whose width is equal to the discharge time of the timing capacitor. If the clock pulse width is small, below 100nsec, the input capacitor to the sync circuit, C_{ST}, may be eliminated.

Figure 12 shows a sync circuit for the UCC3802. This circuit may be modified for use with other PWM control circuits that do not have an oscillator sync output. The UCC3802 discharges the timing capacitor C_T with a 1.8mA current. The sync circuit is configured so that when C_T discharges, a negative voltage appears across R_{ST}. The emitter of Q_S is connected here and when the C_T is being discharged most of the current flows through Q_S and takes it into saturation. The collector of Q_S is connected to the FB pin of the UC3853 through the same network described above. The base of Q_S is biased above ground because the timing capacitor C_T will not discharge completely in this circuit due to the voltage offset of the emitter base junction of Q_S. This offset voltage changes the amplitude of the oscillator voltage and its frequency. By raising the base of Q_S above ground, the offset voltage is minimized. The offset voltage also has a temperature coefficient and D_S compensates for this so that the oscillator frequency drift over temperature will be reduced. All of the base components are optional but they do improve the performance of the sync circuit.

Further information about synchronization in general may be found in Unitrode Application Note U-111. Several of the circuits there may be adapted to the UC3853 synchronization circuits shown here.

LAYOUT CONSIDERATIONS

The UC3853 is a high speed circuit generally operating in a high noise environment. It requires careful layout and grounding to operate correctly. A ground plane extending at least 1 inch on each side of the device is recommended to control noise pickup. Do not let power currents in the ground plane run beneath the device. A split in the ground plane is acceptable to control the flow of current and divert it around the device if necessary. It is worthwhile to keep low level signals as far away from high noise signals, such as the output gate drive, as possible. Good bypassing of the VCC pin is essential. A 0.1µF ceramic capacitor connected between VCC and GND should be located within 0.5 inch of the UC3853 and connected with short, direct connections. The IMO pin and the FB pin are especially sensitive to noise because they are high impedance nodes. Keep the amount of printed circuit board trace connected to these pins as short as possible. The total length should be kept less than 1 inch. The general rule of thumb for printed circuit board layout is to place the UC3853 in the desired position and then to place the ceramic bypass capacitor as close to the VCC pin as possible. Then, and only then, proceed with placing the other components.

DISCONTINUOUS CONDUCTION MODE AND LIGHT LOAD OPERATION

The boost converter described in this Application Note normally runs in continuous inductor current mode but enters discontinuous conduction mode when the input voltage is low and when the load current is light. In discontinuous conduction mode the gain of the boost power stage is reduced which can lead to reduced performance. The UC3853 uses an average current control technique where the boost power stage is embedded in a feedback loop that includes a high gain opamp which compensates for the changes in gain. The average current control loop regulates the input current in the converter and maintains the correct input current

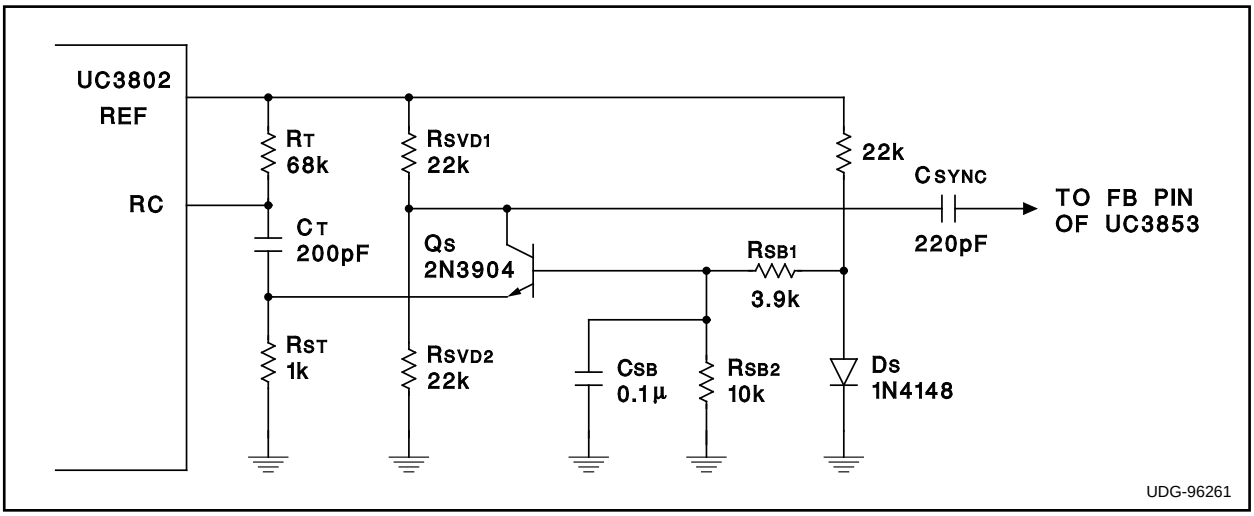

Figure 12. Synchronization Circuit for PMW Control Circuits Without a Clock Output

wave shape even though the current through the inductor is not continuous.

During operation of the converter at light loads, the input filters can contribute phase shift to the input current that reduces the power factor. Careful design is required to maintain high power factor at light loads. A capacitor, generally included after the input diodes as part of the input filter, is necessary to keep the high frequency ripple current from the boost converter out of the power lines. At light loads this capacitor holds charge as the input voltage goes through zero volts and turns the diode bridge off, introducing distortion into the input current. This is why the input capacitor value must be carefully selected.

It is possible to design a power factor corrector using the UC3853 which operates only in discontinuous inductor current mode. Such a converter will have good power factor and low distortion input current but it will also have high input ripple current which must be filtered out to pass EMI requirements. The design of a discontinuous conduction mode boost power factor corrector is not covered in this Application Note.

Another application of the UC3853 is with a flyback converter to produce a power factor corrected input current and a regulated and, optionally, isolated output voltage. Any power factor corrected converter produces a sinusoidal output current at the second harmonic of the input line frequency so a large amount of filtering or secondary regulation may be necessary to provide a useful output in most applications. The flyback converter may be operated in either continuous or discontinuous conduction modes. Both modes have large amounts of high frequency input current that must be filtered out to meet EMI requirements and the filter produces phase shift of the input current and reduces the power factor. The design of a flyback converter for power factor correction is not covered by this Application Note although the design is not particularly difficult.

DESIGN SUMMARY

This section summarizes the design process for a boost power factor corrector using the UC3853. The 100W design example with “universal” input voltage range used in the body of this Application Note is repeated here.

1. Specifications: Determine the operating requirements for the boost power factor corrector.

   Example:

   P_{OUTmax} = 100 Watts
   V_{OUT} = 400VDC
   Line voltage range = 80 to 270VAC
   Line frequency range = 47 to 65Hz
   Maximum THD = 5%
   Power Factor = 0.99

2. Switching frequency: The switching frequency is fixed at 75kHz but may be synchronized in the range of 95kHz to 115kHz. See the text for further information on synchronization.

3. Inductor selection:

   A. Find the maximum peak line current. Assume $P_{IN} = P_{OUT}$ and use P for the power rating.

   $$Ipk = \frac{\sqrt{2} \bullet P}{V_{INmin}}$$

   Example:

   $$Ipk = \frac{\sqrt{2} \bullet 100W}{80V} = 1.77Apk$$

   B. Find ΔI, the peak-to-peak high frequency ripple current. See the text for information on the selection of the ripple current. The typical range is 15 to 25% of Ipk.

   $\Delta I = 0.2 \bullet Ipk$

   Example:

   $\Delta I = 0.2 \bullet 1.77Apk = 0.35Apk\text{-}pk$

   C. Find the minimum duty factor, D, at $V_{INmin(pk)}$. This occurs at Ipk.

   $$D = \frac{V_O - \sqrt{2} \bullet V_{INmin}}{V_O}$$

   Example:

   $$D = \frac{400V - \sqrt{2} \bullet 80V}{400V} = 0.72$$

   D. Calculate the inductor value.

   $$L = \frac{\sqrt{2} \bullet V_{INmin} \bullet D}{f_S \bullet \Delta I}$$

   Example:

   $$L = \frac{\sqrt{2} \bullet 80V \bullet 0.72}{75 \bullet 10^3 Hz \bullet 0.35A} = 3.1mH$$

   Round this value to 3.0mH.

4. Output capacitor selection: If hold-up time is important use the equation below. Typical

values for a 400V output are 1µF to 2µF per Watt. If hold-up is not required, use the second harmonic ripple voltage and capacitor power dissipation to determine the minimum size of the capacitor. Δt is the hold-up time in seconds and V_{Omin} is the voltage to which the output decays at the end of the hold-up time.

$$C_O = \frac{2 \bullet P \bullet \Delta t}{V_O^2 - V_{Omin}^2}$$

Example: V_{Omin} is 350V and Δt is 19msec.

$$C_O = \frac{2 \bullet 100W \bullet 19 \bullet 10^{-3}sec}{(400V)^2 - (350V)^2} = 100\mu F$$

5. Current sense resistor selection: Select the current sense resistor to give 1.0V at the maximum peak input current.

$$R_S = \frac{1V}{Ipk + \frac{\Delta I}{2}}$$

Example:

$$R_S = \frac{1V}{1.77A + 0.5 \bullet 0.35A} = 0.5\Omega$$

6. Switch and diode selection: The switches and diodes may be selected from the table which follows this section or may be chosen by any other standard design criteria. The text discusses selection criteria.

   The output drive of the UC3853 provides about 500mA peak current. Choose R_Q to limit the current under normal operating conditions. A value of 33Ω or more will provide adequate control of the gate charge current, give good rise and fall times for small switches and eliminates the need for D_Q. If a lower value of R_Q is chosen, then D_Q is required.

7. Input diode and capacitor selection: Fast recovery rectifiers are recommended for D_{IN}. The faster the diode reverse recovery the lower the input current distortion will be. Choose a diode type rated for the maximum voltage at high line and for the maximum current at low line. It must also have adequate power dissipation capability.

   The choice of C_{IN} is a compromise between power factor and EMI performance. The value may not be too large or input distortion increases. The value may not be too small or EMI increases. Choose a device which will handle the full high frequency ripple current from the boost converter. A film or ceramic type is generally recommended. See the text for further selection information.

8. Multiplier set up: I_{AC} is 500µA maximum. R_{AC} is determined by Ohm's law.

$$R_{AC} = \frac{\sqrt{2} \bullet V_{INmax}}{0.5 \bullet 10^{-3}A}$$

   Example:

$$R_{AC} = \frac{\sqrt{2} \bullet 270V}{0.5 \bullet 10^{-3}A} = 764k\Omega$$

   Choose two standard value 390kΩ resistors in series to allow for voltage stress ratings.

9. Current amplifier gain at the switching frequency:
   A. Calculate ΔV_{RS}, the voltage change across the sense resistor due to the down slope of the inductor current if V_{IN} = 0 (at the zero crossing).

$$\Delta V_{RS} = \frac{V_O \bullet R_S}{L \bullet f_S}$$

   Example:

$$\Delta V_{RS} = \frac{400V \bullet 0.5\Omega}{3 \bullet 10^{-3}H \bullet 75 \bullet 10^{3}Hz} = 0.89V$$

   B. The gain of the current amplifier at the switching frequency is the ratio of the oscillator voltage and ΔV_{RS}. The oscillator voltage in the UC3853 is 5.0Vpk-pk.

$$G_{CA} = \frac{V_{OSC}}{\Delta V_{RS}}$$

   Example:

$$G_{CA} = \frac{5V}{0.89V} = 5.625\ (15.0dB)$$

10. Current amplifier compensation:
    A. R_{MO} selection: R_{MO} = 3.9kΩ
    B. R_{CZ} selection: R_{CZ} sets the gain of the amplifier at the switching frequency.

       $R_{CZ} = G_{CA} \bullet R_{MO}$
       Example:
       $R_{CZ} = 5.625 \bullet 3.9k\Omega = 22k\Omega$
    C. C_{CZ} selection: Calculate the unity gain crossover frequency of the current loop if C_{CZ} were not present.

$$f_{CI} = \frac{V_O \bullet R_S \bullet R_{CZ}}{V_{OSC} \bullet 2 \bullet \pi \bullet L \bullet R_{MO}}$$

Example:

$$f_{CI} = \frac{400V \bullet 0.5\Omega \bullet 22 \bullet 10^3\Omega}{5V \bullet 2 \bullet \pi \bullet 3 \bullet 10^{-3}H \bullet 3.9 \bullet 10^3\Omega}$$

$$= 12 \bullet 10^3Hz$$

Choose the value of C_{CZ} to have an impedance equal to or less than R_{CZ} at f_{CI}.

$$C_{CZmin} = \frac{1}{2 \bullet \pi \bullet f_{CI} \bullet R_{CZ}}$$

Example:

$$C_{CZmin} = \frac{1}{2 \bullet \pi \bullet 12 \bullet 10^3Hz \bullet 22 \bullet 10^3\Omega}$$

$$= 600 \bullet 10^{-12}F$$

Choose a larger value of capacitance to increase the phase margin. C_{CZ} = 680pF.

D. C_{CP} selection: The C_{CP} and R_{CZ} pole must be greater than the switching frequency.

$$C_{CPmax} = \frac{1}{2 \bullet \pi \bullet f_S \bullet R_{CZ}}$$

Example:

$$C_{CPmax} = \frac{1}{2 \bullet \pi \bullet 75 \bullet 10^3Hz \bullet 22 \bullet 10^3\Omega}$$

$$= 100 \bullet 10^{-12}F$$

Choose a smaller value of capacitance.

C_{CP} = 68pF

11. Harmonic Distortion Budget: The allocation of the allowed THD among the main error sources is somewhat arbitrary. The feedforward voltage contributes 1% third harmonic distortion for each 1% second harmonic on the bias supply to the UC3853. The voltage loop contributes 0.5% third harmonic distortion for each 1% second harmonic voltage on the output.

    Example: The specification is for 5% THD maximum. 2% is allocated to the feedforward voltage, 2% is allocated to the voltage control loop and 1% to miscellaneous sources.

12. Voltage amplifier: The voltage loop amplifier is a transconductance amplifier so its compensation is a bit different from other types of amplifiers.

    A. Voltage Divider: R_{VI} and R_{VD}. This voltage divider sets the DC output voltage. The UC3853 reference voltage is 3.0V. Choose a value for R_{VD} and calculate the value for R_{VI} from the equation.

$$R_{VI} = R_{VD} \bullet \left(\frac{V_O}{V_{FB}} - 1\right)$$

Example:

Choose R_{VD} = 10kΩ.

$$R_{VI} = 10 \bullet 10^3\Omega \bullet \left(\frac{400V}{3V} - 1\right) = 1.3 \bullet 10^6\Omega$$

Choose two standard value 620kΩ resistors in series for R_{VI} to allow for the resistor voltage rating.

Solve for a parallel resistance to R_{VD} to get correct output voltage.

$$R_{VD} = \frac{R_{VI} \bullet V_{FB}}{V_O - V_{FB}}$$

Example:

$$R_{VD} = \frac{1.24 \bullet 10^6\Omega \bullet 3V}{400V - 3V} = 9.37 \bullet 10^3\Omega$$

This is 10kΩ in parallel with 150kΩ.

B. Voltage divider gain: The gain of the voltage divider is given from the following equation:

$$G_{VD} = \frac{V_{FB}}{V_O}$$

Example:

$$G_{VD} = \frac{3V}{400V} = 0.0075 \text{ (-42.5dB)}$$

C. Output ripple voltage: Output ripple voltage is given by the following equation where f_{Lmin} is the minimum line frequency. Low line frequency will give the greatest value of V_{Opk}.

$$V_{Opk} = \frac{P}{2 \bullet \pi \bullet 2 \bullet f_{Lmin} \bullet C_O \bullet V_O}$$

Example:

$$V_{Opk} = \frac{100W}{2 \bullet \pi \bullet 2 \bullet 47Hz \bullet 100 \bullet 10^{-6}F \bullet 400V}$$

$$= 4.2V$$

D. Amplifier Gain: This gain calculation includes the gain of the voltage divider. The

input range to the multiplier is the active range of the amplifier output voltage on the UC3853. ΔV_{COMP} is 4.5V on the UC3853. The %ripple used in the equation below is the amplitude of the ripple at the output of the voltage amplifier as a percentage of ΔV_{COMP} and the percentage is twice that specified for second harmonic voltage since the ripple is reduced by half in the power circuits. The equation uses %ripple in its numeric form.

$$G_V = \frac{\Delta V_{COMP} \bullet \%ripple}{V_{Opk}}$$

Example:

$$G_V = \frac{4.5V \bullet 0.04}{4.2V} = 0.043\ (-27.3dB)$$

The gain of the voltage error amplifier alone is G_V divided by the gain of the voltage divider.

$$G_{VEA} = \frac{G_V}{G_{VD}}$$

Example:

$$G_{VEA} = \frac{0.043}{0.0075} = 5.73\ (15.2dB)$$

E. Amplifier Compensation: A network connected from the output of a transconductance amplifier to ground determines its gain and frequency response. The gain of the amplifier is set for loop stability without regard to DC gain or THD. Those considerations come next. The gain of the amplifier is:.

$$G_{VEA} = G_M \bullet X_{CVC}$$

Where G_M is the transconductance of the UC3853 voltage amplifier as specified in the data sheet as 485µS. X_{CVC} is the impedance of C_{VC} at the second harmonic of the line frequency ($2 \bullet f_{Lmin}$). Solve the equation for X_{CVC} then convert the impedance to a capacitance value.

$$C_{VC} = \frac{G_M}{2 \bullet \pi \bullet 2 \bullet f_{Lmin} \bullet G_{VEA}}$$

Example:

$$C_{VC} = \frac{485 \bullet 10^{-6}S}{2 \bullet \pi \bullet 2 \bullet 47Hz \bullet 5.73} = 0.15 \bullet 10^{-6}F$$

F. Unity Gain Voltage Loop Crossover Frequency: The unity gain frequency of the now completed voltage control loop is found next. The following equation gives the frequency at which the loop gain is equal to one. Solve for f_{VI}.

$$f_{VI}^2 = \frac{P \bullet G_M \bullet G_{VD}}{(2 \bullet \pi)^2 \bullet C_O \bullet C_{VC} \bullet \Delta V_{COMP} \bullet V_O}$$

Example:

$$f_{VI} = \frac{1}{2 \bullet \pi} \bullet \sqrt{\frac{100W \bullet 485 \bullet 10^{-6}S \bullet 0.0075}{100 \bullet 10^{-6}F \bullet 0.15 \bullet 10^{-6}F \bullet 4.5V \bullet 400V}}$$

$$= 18.6Hz$$

G. R_{VC}: R_{VC} is added to the loop compensation to give a pole at f_{VI}. The value of R_{VC} is the resistance equal to the impedance of C_{VC} at f_{VI}. This gives approximately 45° of phase margin. A smaller value of R_{VC} will increase the phase margin at the expense of loop bandwidth.

$$R_{VC} = \frac{1}{2 \bullet \pi \bullet f_{VI} \bullet C_{VC}}$$

Example

$$R_{VC} = \frac{1}{2 \bullet \pi \bullet 18.6Hz \bullet 0.15 \bullet 10^{-6}F}$$

$$= 57 \bullet 10^3\Omega$$

The closest standard value is 56kΩ.

H. C_{VCZ}: C_{VCZ} is added in series to R_{VC} to break the DC current path from the output of the voltage error amplifier to ground because the limited current capability of the transconductance amplifier stage. The zero added to the loop compensation increases the DC regulation of the output at the expense of increased peak-to-peak voltage excursions during transients. This zero introduced by C_{VCZ} must be set at least two octaves below f_{CI} to maintain a reasonable phase margin. The value of C_{VCZ} must therefore be at least four times the value of C_{VC}.

$$C_{VCZ} = 4 \bullet C_{VC}$$

Example:

$C_{VCZmin} = 4 \bullet 0.15µF = 0.6µF$

Choose C_{VCZ} = 1.0µF to give increased phase margin.

13. Voltage Feedforward: The feedforward voltage comes from the bias supply V_{FF}, which is supplied by a winding on the inductor. For the example converter, the turns ratio is set to give 10.5VDC with minimum input voltage after all parasitic losses are taken into account. The second harmonic ripple voltage must be held to 2% peak of V_{FFmin} according to the THD budget in step #10 above. The numeric value of THD is used in the equation. See the text for further information. The peak-to-peak ripple voltage is given by:

$$V_R = \pi \bullet V_{FF} \bullet THD$$

Example:

$$V_R = \pi \bullet 10.5V \bullet 0.02 = 0.66Vpk\text{-}pk$$

The current drawn by the control circuits is about 15mA. The value of C_{FF} is given by:

$$C_{FF} = \frac{I_{FF}}{V_R \bullet 2 \bullet f_{Lmin}}$$

Example:

$$C_{FF} = \frac{0.015A}{0.66V \bullet 2 \bullet 47Hz} = 242 \bullet 10^{-6}F$$

Choose a standard value of 270µF.

14. Starting Resistors: C_{FF} must be charged to 11.5V to start the UC3853 and it is trickle charged from V_{IN} by the current through R_B. The current through R_B at high line must not exceed the bias current of the UC3853 or V_{FF} will not track the input voltage and feedforward will be lost. The value of R_B may not be too large or the delay between the application of power and the start of the circuit will be too long. If the current through R_B is less than 500µA at low line the circuit will never start. A 1sec delay at low line is chosen as the maximum value. This is an arbitrary decision within the guidelines given.

$$R_B = \frac{t_{DELAY} \bullet \sqrt{2} \bullet V_{INmin}}{V_{FF} \bullet C_{FF}}$$

Example:

$$R_B = \frac{1sec \bullet \sqrt{2} \bullet 80V}{11.5V \bullet 270 \bullet 10^{-6}F} = 36 \bullet 10^{3}\Omega$$

Split this into two 18kΩ resistors because the voltage at high line is greater than 250V peak. At high line this gives 6.8mA of bias current which is less than I_{FF} (15mA) so this value is acceptable.

15. This completes the design of the boost power factor corrector.

INDUCTOR DESIGN

The 3.0mH inductor may be built as follows:

Core: Micrometals T157-8/90 — OD = 1.57in.
ID = 0.95in. Ht = 0.57in. m = 35
Main winding: 250 turns #20AWG
Auxiliary winding: 25 turns #28AWG

DESIGN TABLE FOR "UNIVERSAL" INPUT VOLTAGE RANGE

P_{OUT}	25	50	75	100	125	150	200	(Watts)
L	12	6.0	4.0	3.0	2.5	2.0	1.5	(mH)
C_O	25	50	75	100	125	150	200	(µF)
R_S	2.0	1.0	0.68	0.5	0.39	0.33	0.25	(Ω)
C_{IN}	0.22	0.5	0.68	1.0	1.0	1.0	1.0	(µF)
Q	IRF820 ---------->		I RF830 ---------->					
D_{OUT}	MUR160 -------->|		MUR460 ----->|		MUR860 ---------->|		
	BYV26C -------->|		BYM26C ------>|				
D_{IN}	1N4005 --------->|		MR856 ---------->|				
	1N4937 --------->|		BYW95C ---------->|				

Note: The values of the control circuit components remain the same and do not change with power output as long as the main component values are selected from the table. The control circuit components do change value under several circumstances: 1) The main component values are different from those given in the table. 2) The input voltage range or frequency range is different from that specified for the example converter. 3) The THD budget is different. 4) The output voltage is different.

The core is an iron powder toroid. The two windings must be phased properly for correct operation of the converter. The main winding is best wound with bank or progressive winding rather than layer winding. Progressive or bank winding starts at one point on the core and winds progressively around the core until all the turns are in place. A small amount of backing up is required to get the wires to lay evenly on the core. The object is to get the turn-to-turn voltage to be as low as possible. This reduces the effective capacitance of the winding and increases the resonant frequency as well as eliminating the possibility of corona in the winding. The auxiliary winding needs to be insulated from the main winding and is wound outside the main winding.

HEAT SINK

The switch in the example converter dissipates approximately 8W at low line input. The heat sink is an Aavid 529802 and has a thermal resistance of 5°C/W.

REFERENCES

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[5] W. Andreycak, "Practical Considerations in Current Mode Power Supplies," Unitrode Applications Note U-111.

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APPENDIX A: WHAT IS POWER FACTOR?

If a resistor is connected to a sinusoidal AC power line, the current will be sinusoidal and it will be in phase with the voltage. Any deviation from this ideal results in distortion of the current waveform. The apparent power delivered to the load is the sum of the real power and the distortion. The ratio of the apparent power delivered to the load and the real power delivered is the power factor and has a value between zero and one. The current through a purely resistive load has no phase shift and no harmonic distortion and so has a power factor of 1.0. Power factor is given by the following equation:

$$PF = \frac{\text{Real Power}}{V_{RMS} \bullet I_{RMS}}$$

The distortion of the input current has two components, a linear component which is the phase shift between the voltage and current and a non-linear component which is the harmonic distortion of the current waveform. The above equation for power factor may be solved for the phase distortion and the result becomes:

$$PF = \cos(\Theta)$$

Where Θ is the angle between the voltage sinusoid and the current sinusoid. This is the classic definition of power factor as used by electric utilities and it is the major form of distortion created by linear circuits such as motors.

The equation for power factor may also be solved for the harmonic distortion and the equation becomes:

$$PF = \frac{1}{\sqrt{1 + (THD)^2}}$$

Where THD is the Total Harmonic Distortion of the current. This equation is the one with which we are most concerned in power electronics.

In a typical power electronics application the sinusoidal voltage from the power line is rectified and filtered to produce a high DC voltage which is then changed by a DC/DC converter to some other voltage which is useful to the system. The current from the rectifier and input filter generally has little phase shift but has much distortion. A choke input filter will produce a square wave input current with a power factor of about 0.9 and a THD near 50%. A capacitor input filter will produce a train of sharp current spikes with a power factor near 0.5 and THD over 100%. A power factor corrected input will produce a sinusoidal current which has a power factor of greater than 0.99 and harmonic distortion well below 5% at nominal load.

Power factor correction is required in much of the European Community for many electronic products. Power factor correction simplifies the distribution of electric power and thus reduces the cost to the consumer. It is expected that the requirement for power factor correction will grow in the future.

The boost power factor corrector is a boost converter whose control circuit programs the input current to be proportional to the input voltage and thus the input impedance appears resistive. It is the most common type because the boost converter has continuous input current and thus requires the least amount of filtering for the switching frequency ripple current.

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