

# **Programming the UCC3809 for 90% Maximum Duty Cycle Clamp**

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## **ABSTRACT**

Normally, the UCC3809 programmable duty cycle clamp feature is limited to 70% maximum duty cycle. The described technique shows how the maximum duty cycle clamp can be programmed to achieve a 90% on-time of the switching period.

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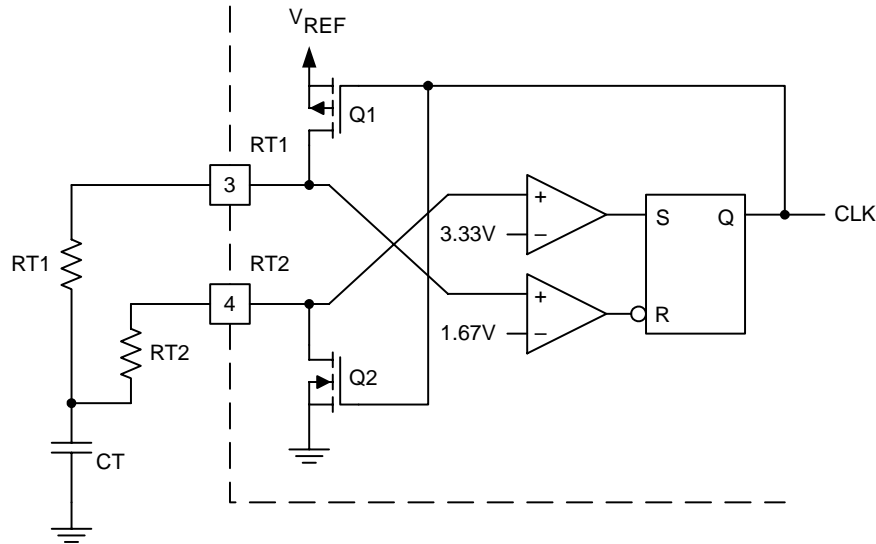
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## **1 Introduction**

Because of the propagation delays through the oscillator comparators, the RS latch, and the N-channel and P-channel FET drivers, the UCC3809 Economy Primary Side Controller is theoretically limited to 70% maximum duty cycle at frequencies of up to 1 MHz. The 30% off-time allows for accurate sensing of the upper and lower voltage thresholds of the external timing capacitor,  $C_T$ , and allows for lot-to-lot process variations of the device to have minimal impact on the programmed switching frequency.

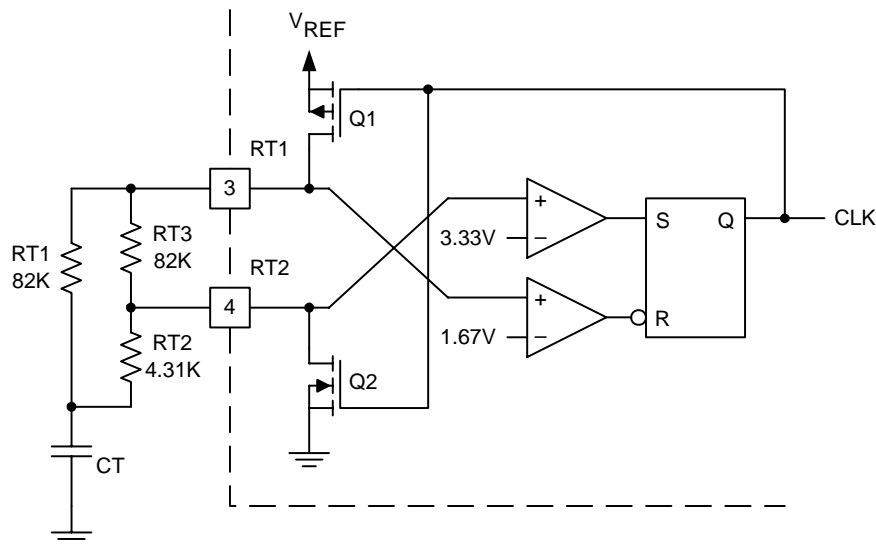
## **2 Operation**

Under typical operating conditions, two resistors and one capacitor are used to set the oscillator frequency. As shown in Figure 1, the timing resistor, RT1, provides a current path through the  $R_{DS(on)}$  of P-channel FET, Q1, when the CLK signal is low, thereby setting the positive ramp time. During this  $C_T$  charging time, Q2 is off and pin 4 is used to sense the voltage of  $C_T$ . At the upper trip point of 3.33 V, the RS latch is set and the CLK signal goes high. This signal turns off Q1 and turns on N-channel FET, Q2.  $C_T$  then has a discharge path through RT2 and the  $R_{DS(on)}$  of Q2. Pin 3 is used as the sense pin, resetting the oscillator latch when  $C_T$  discharges to 1.67 V. RT1 should not be less than 10 k $\Omega$ . RT2 should not be less than 4.31 k $\Omega$ . These minimum values for the timing resistors maintain a 10:1 ratio with the on-resistances of Q1 and Q2, respectfully, resulting in a negligible change in frequency due to temperature variations.



**Figure 1. Standard Maximum Duty Cycle Clamp Configuration for the UCC3809 Oscillator**

Unfortunately, many converters require a duty cycle greater than 70% for optimal efficiency. The UCC3809 can be configured for a 90% maximum duty cycle clamp for frequencies of 250 kHz or less with the addition of a single resistor, RT3, as shown in Figure 2. RT2 is kept at its minimum recommended value of 4.31 k $\Omega$ . RT1 and RT3 are set to be 82 k $\Omega$  each; the parallel combination of which results in an approximate ratio of 9:1 with RT2, establishing the 90% duty cycle. Figure 3 shows the CT capacitor value for the desired oscillator frequency when the configuration in Figure 2 is used with the resistor values given.



**Figure 2. UCC3809 Oscillator and 90% Maximum Duty Cycle Clamp Configuration**

Under the operating conditions of Figure 2, the charging path for CT is through the parallel combination of RT1 and (RT2+RT3). Pin 4 monitors the voltage at the RT3–RT2 node. Because RT2 is very small compared to RT3, the voltage of this node at the conclusion of the charge cycle is approximately equal to the voltage of CT. The charge cycle is relatively long at 90% of the total switching period resulting in little chance of voltage overshoot of this threshold. RT3 also adds a loop to the discharge path of CT. The voltage at the RT1–RT3 node triggers the comparator to conclude the discharge cycle. This initiates a charge cycle sooner than if sensed at CT directly. CT actually only discharges to a voltage that is equal to the threshold voltage of pin 3 plus one-half the voltage drop across RT2. If the threshold was sensed directly at CT, the charge cycle would not begin until after CT discharges to 1.67 V and the signal travels through the comparators, the RS latch, and the large internal FETs. This time delay is substantial when compared to the relatively fast discharge time, causing the lower threshold to be over shot to an unpredictable level.

Frequencies above 250 kHz are not recommended for duty cycles over 70%; the brief off-time of these faster switching frequencies, if configured for greater than 70% duty cycles, does not give adequate margin for the propagation delay through the internal oscillator components. To configure higher duty cycles at frequencies in excess of 250 kHz, the CT capacitor would be unreasonably small while trying to maintain the minimum impedance at each node. Although hardened against variation due to temperature deviation, any stray capacitance would negatively impact the desired switching frequency.

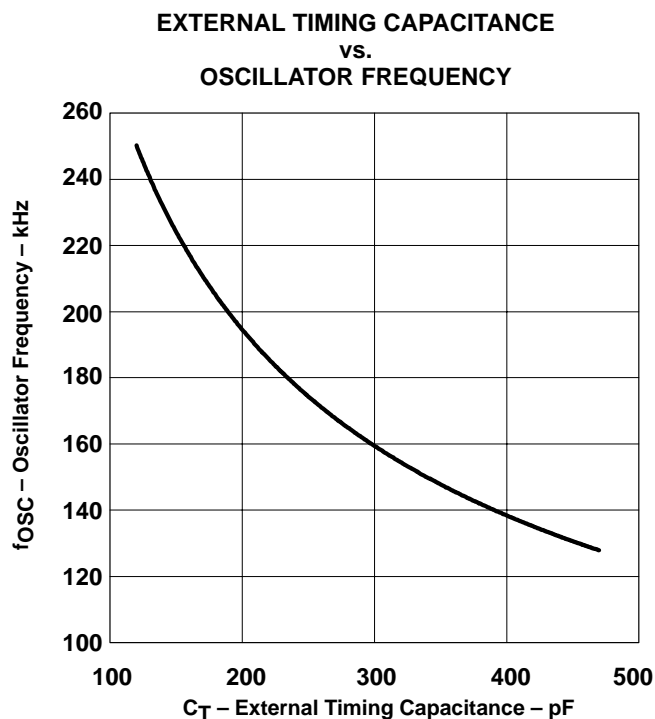


Figure 3

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