

Optimizing Efficiency and Standby Power With the UCC28056x in Offline Applications

ABSTRACT

Modern product regulations require lower standby power and greater efficiency. Strategies for meeting these requirements can require complex power sequencing to shut down portions of the power system to elevate the light-load efficiency. In addition, shutting down portions of the power system, such as the PFC stage, requires a downstream power converter to be designed for a wide input voltage range. The UCC28056x architecture and features such as burst mode, empowers designs to meet these modern power requirements. This allows the PFC stage to remain on in all power modes.

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1 Introduction

Efficiency and standby power have become greater points of emphasis in offline applications, as product regulations continue to demand enhanced performance in these key areas. This emphasis has resulted in sophisticated power strategies to satisfy these requirements, such as shutting down the PFC stage when in low-power modes. While effective, this strategy greatly increases the complexity of the system design. This burdens the design of the DC/DC converters downstream of the PFC, forcing them to be able to handle a wider input voltage range. The UCC28056x device is specifically designed to address this issue and to maintain high efficiency across the entire load range, allowing the designer to leave the PFC on – even in low power modes. This application report examines design decisions for optimizing a transition-mode PFC design for efficiency and standby power using the UCC28056x.

2 Power Standards

Table 1 and Table 2 summarize the power requirements of the United States Department of Energy (DOE) Level VI for applications with nameplate output power of 50 mW and above.

Table 1. DOE Level VI (50 W to 249 W)

DOE LEVEL VI (50 W to 249 W)	
Standby Power	< 210 mW
Regulates Efficiency Performance at:	25%, 50%, 75%, 100% Load
Minimum 4 Point Efficiency Average	88%

Table 2. DOE Level VI (>250 W)

DOE LEVEL VI (> 25 W)	
Standby Power	< 210 mW
Regulates Efficiency Performance at:	25%, 50%, 75%, 100% Load
Minimum 4 Point Efficiency Average	88%

Table 3 summarizes the power requirements of the European Union Code of Conduct (CoC) Tier II for applications with nameplate output power of 50 W to 250 W. Requirements for nameplate output power greater than 250 W are not available at the time.

Table 3. CoC Tier II Power Requirement

CoC TIER II (50 W to 249 W)	
Standby Power	< 150 mW
Regulates Efficiency Performance at:	10%, 25%, 50%, 75%, 100% Load
Minimum 4 Point Efficiency Average	89%

Note that CoC Tier II takes into account a light-load efficiency point at 10% load, where efficiency typically suffers due to static losses and lower output power. A lower efficiency at 10% load then facilitates the need for even greater efficiency at the other four regulated efficiency points to meet the minimum average efficiency.

4 Burst Mode Operation

The UCC28056x implements a burst mode function to further enhance light-load efficiency and standby power. Furthermore, the on-time pulse width is ramped over the first four switching cycles upon entering burst mode. In addition, the on-time pulse width is ramped down over the last four switching cycles before exiting burst mode. This soft-on and soft-off strategy ramps up the line current over the first four cycles upon entering burst mode and ramps down the line current over the last four cycles. This feature limits audible noise and disturbance to the EMI filter in light-load conditions.

Entering and exiting burst mode is implemented as two comparator thresholds applied to the COMP pin voltage. The average voltage of the two comparator thresholds is approximately 10% of V_{COMP_Max} , meaning the power delivered during each burst period is approximately 10% of the maximum output power for the UCC28056. [Table 4](#) showcases the burst mode threshold for all the UCC28056x devices:

Table 4. Burst Mode Variation

DEVICE	BURST MODE THRESHOLD
UCC28056	10%
UCC28056A	15%
UCC28056B	15%
UCC28056C	10%

During the burst-on period, efficiency of the PFC stage is approximately equal to the efficiency of the PFC converter at 11% load. During the burst-off period, current consumption of the UCC28056x drops to 125 μ A. Power loss during the burst-off period, when no switching action occurs, is primarily dominated by static power losses within the PFC stage. [Equation 1](#) provides an approximation of the standby power performance

$$P_{Standby} \approx \frac{P_{INBurst} \cdot t_{BurstON_time} + P_{StaticLoss} \cdot t_{BurstOFF_time}}{t_{BurstON_time} + t_{BurstOFF_time}} \quad (1)$$

As the load on the PFC stage decreases below 10%, the frequency of burst periods also decreases to maintain high efficiency in light load.

5 Limiting Static Losses

Static losses from components within the circuit contribute to a higher standby power. Conduction losses in the bridge rectifier, boost diode, and MOSFET are a few examples. This section provides guidance for selecting appropriate values to minimize power loss in the PFC stage.

5.1 VOSNS Divider

The VOSNS pin is connected to the inverting input of an internal transconductance amplifier and is used to set the PFC stage output regulation point through a resistive divider. As the typical PFC output voltage is approximately 400 V, the static power loss in the feedback divider can be significant and is one of the primary contributors to high standby power. [Equation 2](#) is the static power loss in the VOSNS divider:

$$P_{VOSNS} = \frac{V_{BLK}^2}{R_{OS1} + R_{OS2}}$$

where

- V_{BLK} is the output voltage of the PFC stage
 - R_{OS1} is the top resistor of the divider
 - R_{OS2} is the bottom resistor of the divider
- (2)

For an output voltage of 400 V and a total feedback resistance of 1 M Ω , the static loss from the feedback divider is 160 mW. As such, it is advantageous to use the largest feedback resistance possible. Larger values of R_{OS1} result in degradation of regulation accuracy. However, due to the effect of the V_{OSNS} bias current, $I_{OSNSBias}$, [Equation 3](#) shows the relationship between regulation accuracy and the resistance of R_{OS1} .

$$\frac{\Delta V_{\text{BLKReg}}}{V_{\text{BLKReg}}} = \frac{I_{\text{OSBias}} \cdot R_{\text{OS1}}}{V_{\text{BLKReg}}}$$

where

- I_{OSBias} is the bias current of the VOSNS pin (3)

The maximum I_{OSNSBias} current is 100 nA. Equation 4 ensures output voltage regulation degrades less than 1% due to I_{OSNSBias} .

$$R_{\text{OS1}} \leq 1\% \cdot \frac{V_{\text{BLKReg}}}{I_{\text{OSBias_max}}} \quad (4)$$

For an output voltage of 390 V, the maximum value of R_{OS1} is 39 M Ω . The corresponding value of R_{OS2} can be calculated using Equation 5.

$$\frac{R_{OS1}}{\left(\frac{V_{BLKReg}}{V_{OSReg}} - 1\right)} = R_{OS2}$$

where

- V_{OSReg} is the reference voltage, 2.5 V (5)

If $3 \times 10\text{-M}\Omega$ resistors are used as R_{OS1} and a $100\text{ k}\Omega + 93.1\text{ k}\Omega$ is used as R_{OS2} , the total standby power from the VOSNS divider is 5 mW.

5.2 UCC28056x and UCC25630x Feedback/BLK Divider

For AC/DC systems using a LLC converter downstream of the PFC stage, it is possible to configure the V_{OSNS} resistor divider to function as both the feedback divider for the transition mode boost PFC stage and the BLK pin divider for the LLC controller UCC25630x, as shown in Figure 2. This approach greatly reduces static power loss by eliminating an additional high-voltage divider from the total AC/DC system solution.

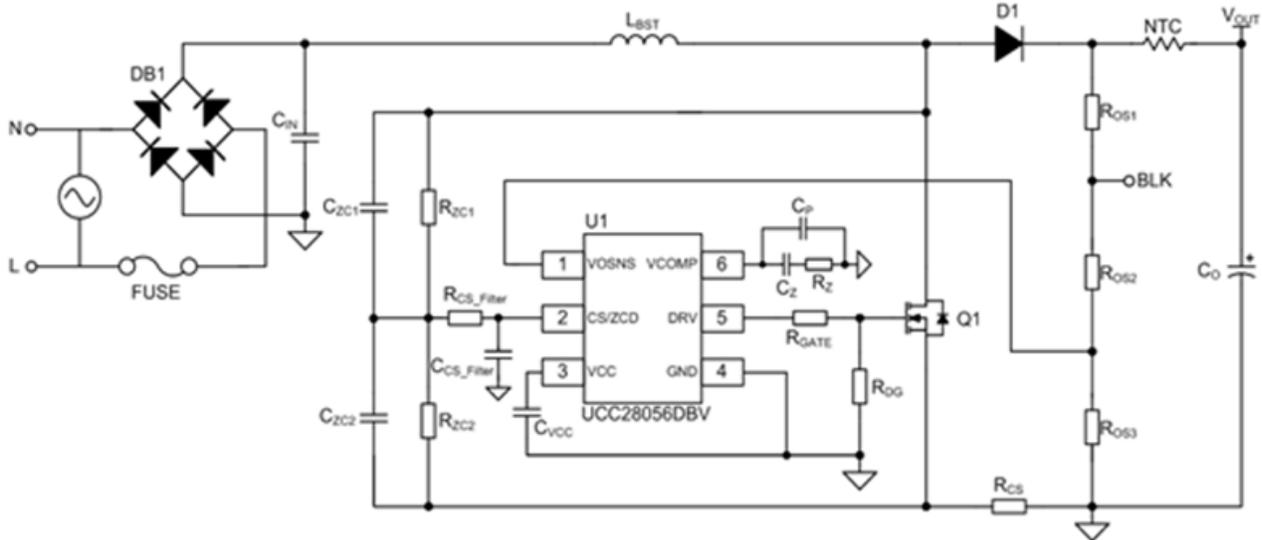


Figure 2. Combining High-Voltage Dividers for UCC28056x and UCC25630x

To accommodate the different resistor division ratios of UCC28056A/B and UCC25630x, two resistor taps are necessary. With the PFC bulk voltage set to 390 V, the VOSNS divider ratio, K_{OS} , equals 156 as Equation 6 shows. K_{BLK} is determined by the minimum PFC bulk voltage at which the LLC is expected to turn on. With a bulk-turn-on threshold of 3.05 V and desired turn-on threshold of 340 V, the BLK divider ratio, K_{BLK} , is equal to 111.5, as shown in Equation 7.

$$K_{OS} = \frac{V_{BLKReg}}{V_{OSReg}} = \frac{R_{OS11} + R_{OS12} + R_{OS2}}{R_{OS2}} = 156 \tag{6}$$

$$K_{BLK} = \frac{V_{ON_LLC}}{V_{BLKTh}} = \frac{340V}{3.05V} = \frac{R_{OS11} + R_{OS12} + R_{OS2}}{R_{OS12} + R_{OS2}} = 111.5 \tag{7}$$

For this example, select an upper divider resistor, R_{OS11} , consisting of three series-connected 3.24 M Ω , 1206 SMT resistors, as Equation 8 shows.

$$R_{OS11} = 3 \cdot 3.24M\Omega = 9.72M\Omega \tag{8}$$

Solving equations [Equation 6](#) and [Equation 7](#) simultaneously yields [Equation 9](#).

$$R_{OS12} = \frac{R_{OS11}}{K_{OS}} \cdot \left(\frac{K_{OS} - 1}{K_{BLK} - 1} - 1 \right) = 25.092k\Omega \quad (9)$$

The corresponding R_{OS2} is then found using [Equation 10](#).

$$R_{OS2} = \frac{R_{OS11} + R_{OS12}}{K_{OS} - 1} = 62.87k\Omega \quad (10)$$

These two resistances can be implemented using standard resistor values, as [Equation 11](#) and [Equation 12](#) show.

$$R_{OS12} = 47.5k\Omega / 52.3k\Omega = 25.183k\Omega \quad (11)$$

$$R_{OS2} = 124k\Omega / 127k\Omega = 62.74k\Omega \quad (12)$$

The total power dissipation of this combined resistor divider is 15.5 mW.

5.3 ZCD/CS Divider

Power dissipation in the ZCD/CS divider is highest during the burst-off condition. In this state, the drain voltage approximates a DC voltage equal to the line voltage peak. [Equation 13](#) shows the peak power dissipation of the ZCD/CS divider.

$$P_{ZCMax} = \frac{2 \cdot V_{LineRMSMax}^2}{R_{ZC1} + R_{ZC2}}$$

where

- R_{ZC1} is the resistance of the top resistor of the ZCD/CS divider
 - R_{ZC2} is the resistance of the bottom resistor of the ZCD/CS divider
- (13)

Much like the V_{OSNS} divider, the resistance of R_{ZC1} and R_{ZC2} can be increased with a small trade-off in ZCD pin sense accuracy. [Equation 14](#) limits the accuracy degradation due to ZCD bias current to less than 1%:

$$R_{ZC1} \leq \text{Error}\% \cdot \frac{K_{ZC} \cdot V_{ZCBoRise}}{I_{ZCBias}} = 1\% \cdot \frac{401 \cdot 0.3V}{100nA} = 12.03M\Omega \quad (14)$$

The upper resistor in the divider chain, R_{ZC1} , must withstand the peak output voltage under a surge test. For a rugged solution, the resistors in this location should have a voltage rating above the avalanche rating of the boost MOSFET. A series chain of three 1206 SMT, 3.24 M Ω satisfies the accuracy requirement and provides a voltage withstand capability above 600 V. Use [Equation 15](#) and [Equation 16](#) to determine appropriate values for R_{ZC1} and R_{ZC2} :

$$R_{ZC1} = 3 \cdot 3.24M\Omega = 9.72M\Omega \quad (15)$$

$$R_{ZC2} = \frac{R_{ZC1}}{R_{ZC1} - 1} = 24.3k\Omega \quad (16)$$

With a maximum input voltage of 265 Vrms, the peak power dissipation during one half cycle is 14.41 mW.

5.4 X Capacitor Selection

X capacitors are a key component of EMI filters, and are connected line to line to suppress EMI noise. As the capacitor is charged and discharged, power is dissipated across the equivalent series resistance of the capacitor, as shown in [Equation 17](#).

$$P_{XCap} = I_{XCap}^2 \cdot R_{ESR_XCap} \quad (17)$$

The rms capacitor current flowing through the capacitor is dependent on the line rms voltage, the frequency of the line, and the total capacitance in an X capacitor configuration. Neglecting parasitic inductance, the impedance presented to the line by the X capacitor can be calculated with [Equation 18](#).

$$Z_{XCap} = \sqrt{\left(\frac{1}{2 \cdot \pi \cdot F \cdot C}\right)^2 + (R_{ESR_XCap})^2} \quad (18)$$

The power loss in X capacitance can be calculated using [Equation 19](#).

$$P_{XCapMax} = \left(\frac{\sqrt{2} \cdot V_{LineRMSMax}}{Z_{XCap}}\right)^2 \cdot R_{ESR_XCap} \quad (19)$$

For a maximum line voltage of 265 Vrms and 0.33 μ F in parallel, each with a dissipation factor of 0.00022, the power dissipated in the X capacitance is 6.4 mW.

5.5 Active X Capacitor Discharge

Some applications require a method to discharge the line-to-line capacitors used in EMI filters to a reasonable voltage within a specified time. This is to ensure that high voltage does not remain on the AC plug indefinitely. There are several standards which govern the discharge time, such as IEC60950, IEC60065, and IEC62368. [Table 5](#) summarizes these standards.

Table 5. X Capacitor Discharge Standards

STANDARD	DISCHARGE TIME CONSTANT FROM AC UNPLUG (SECONDS)
IEC60950	1s
IEC60065	1s
IEC62368	2s

A prevailing practice is to place bleed resistors in parallel to the X capacitors. A general guideline is every that 100 nF of capacitance requires a maximum bleed resistor of 10 M Ω be added in parallel. For an X capacitance of 330 nF, a bleed resistance of at least 3.3 M Ω is needed.

While this is a cost-effective approach, it leads to additional static power loss in the system and an increase in standby power. For an input voltage range of 85 VAC to 265 VAC, the power loss in a 3.3-M Ω bleed resistor divider is 21.2 mW. A more efficient approach is to use an active X capacitor discharge function that only engages when an AC disconnect is detected. For AC/DC systems using a downstream LLC stage, such a feature is integrated into the UCC256301 and UCC256304 resonant controllers. The UCC256301 and UCC256304 are able to sense the AC line through a high-voltage pin and, when an AC disconnect event is detected, discharge the X capacitance. During steady state, the maximum leakage of the HV pin is 7.55 μ A. Every 720 ms, the UCC25630x converter applies a test current staircase to the line. This checks for zero crossing, and determines an AC unplug event. Assuming the voltage applied to the HV pin is a rectified sine wave equal to the AC line voltage, the worst-case power dissipation can be calculated using [Equation 20](#):

$$P_{XCapDischarge} = V_{HVPin} \cdot I_{HVPin_leakageMax} + P_{TestCurrent} = 265V \cdot 7.55\mu A + 9mW = 11mW \quad (20)$$

5.6 Bridge Rectifier

Power losses in the bridge rectifier are a result of the forward voltage during the conduction period, and the parasitic resistance of each diode. The total power loss in each diode is expressed in [Equation 21](#).

$$P_{Diode} = V_F \cdot I_{Diode_avg} + R_{Diode} \cdot I_{Diode_RMS}^2 \quad (21)$$

The worst-case power loss occurs at minimum line voltage and maximum load. For a peak input current of 2.1 A, forward voltage of 1 V and parasitic resistance of 80 m Ω , the total power loss per diode can be calculated using [Equation 22](#).

$$P_{Diode} = 1V \cdot 1.34A + 0.08\Omega \cdot 1.48A^2 = 1.515W \quad (22)$$

[Equation 23](#) shows the total loss in the bridge rectifier.

$$P_{Rectifier} = 4 \cdot P_{Diode} = 6.06W \quad (23)$$

The forward voltage of a diode is dependent on temperature. Forward voltage decreases as the junction temperature of the diode increases. As such, there exists a trade-off between allowable rise in junction temperature, and lower conduction losses in the bridge rectifier.

5.7 MOSFET Selection

Total power loss in the boost switching element can be described by the conduction loss. This is due to the on-resistance of the switch and the switching loss from driving the gate of the MOSFET. The conduction loss can be calculated with [Equation 24](#).

$$P_{\text{Cond}} = I_{\text{MOS_RMS}}^2 \cdot R_{\text{DS_on}} \cdot Co_{\text{temp}}$$

where

- $I_{\text{MOS_RMS}}$ is the rms current of the MOSFET
 - $R_{\text{DS_on}}$ is the on resistance of the MOSFET
 - Co_{temp} is the temperature coefficient associated with the on resistance
- (24)

Maximum current in the switch occurs at full load and minimum input voltage can be calculated with [Equation 25](#).

$$I_{\text{MOS_RMSMax}} = \frac{110\% \cdot P_{\text{loadmax}}}{V_{\text{LineRMSMin}}} \cdot \sqrt{\frac{4}{3} - \frac{32 \cdot \sqrt{2} \cdot V_{\text{LineRMSMin}}}{9 \cdot \pi \cdot V_{\text{BLK}}}}$$
(25)

The on resistance increases as the junction temperature of the MOSFET increases, and is represented in the conduction loss equation by Co_{temp} . Reducing temperature rise in the MOSFET during operation minimizes the conduction loss. Switching losses in the MOSFET are summarized with [Equation 26](#) through [Equation 28](#).

$$t_{\text{rise}} = \frac{(Q_{\text{gs}} - Q_{\text{g(th)}}) \cdot R_{\text{gate_total}}}{V_{\text{gs}} - \frac{V_{\text{miller}}}{2} - \frac{V_{\text{gs(th)}}}{2}} + \frac{Q_{\text{gd}} \cdot R_{\text{gate_total}}}{V_{\text{gs}} - V_{\text{miller}}}$$
(26)

$$t_{\text{fall}} = \frac{Q_{\text{gd}} \cdot R_{\text{gate_total}}}{V_{\text{miller}}} + \frac{(Q_{\text{gs}} - Q_{\text{g(th)}}) \cdot R_{\text{gate_total}}}{\frac{V_{\text{miller}}}{2} + \frac{V_{\text{gs(th)}}}{2}}$$
(27)

$$P_{\text{switching}} = V_{\text{DS}} \cdot \frac{F_{\text{SW}}}{2} \cdot (t_{\text{rise}} \cdot I_{\text{FET,min}} + t_{\text{fall}} \cdot I_{\text{FET,max}})$$
(28)

It is advantageous to minimize the gate charge of the MOSFET to lower the rise and fall transition times. However, for 600-V MOSFETs, the choice is limited in this regard.

6 Standby Power Measurement Tips

Real power consumed by the PFC stage can be calculated using [Equation 29](#).

$$P_{\text{real}} = V_{\text{Line}} \cdot I_{\text{Line}} \cdot \text{PF}$$
(29)

Due to the burst mode behavior of UCC28056x, input power variation is often quite high. It can be difficult to measure accurately from an instantaneous power measurement. Using a power meter with an integration function allows the user to integrate mWh over a set time interval, and then perform a simple calculation to obtain the average input power consumed by the PFC stage. [Figure 3](#) shows the proper connections for standby power measurement on the UCC28056EVM-296.

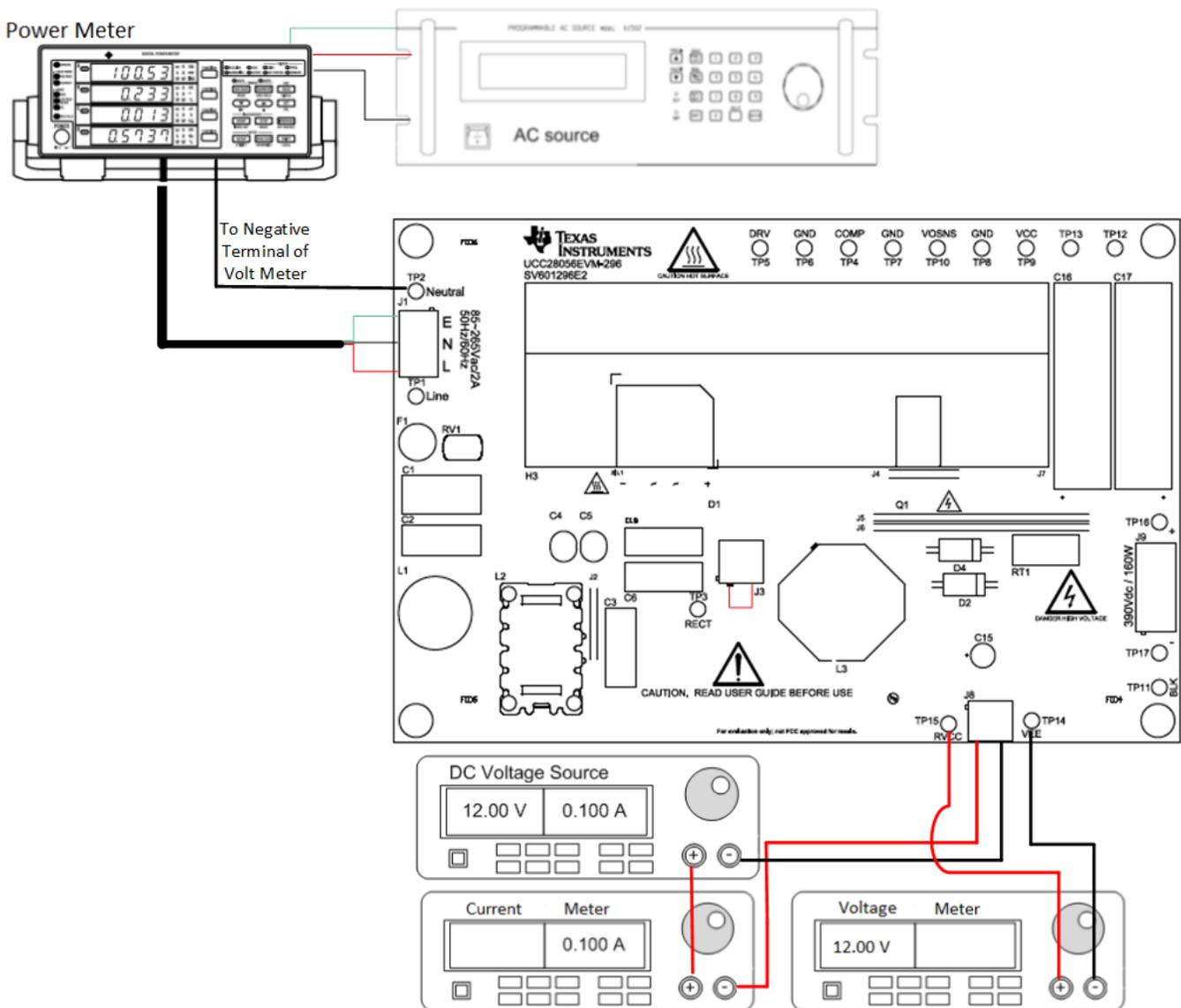


Figure 3. Standby Power Measurement Connections

6.1 Power Meter Connections and Settings

It is strongly advised to physically disconnect the output of the PFC stage from any measurement instrumentation, such as electronic loads or voltmeters. Because the output of the PFC stage is relatively high voltage, leakage current drawn by a measurement instrument can result in a light load of 10s of mW, which artificially inflates the standby power measurement. It is also important to connect the positive terminal of the voltage measurement to the cord facing the AC source. This is to prevent power consumption of the AC line voltage measurement from inflating the standby power results. As very little current is drawn by the PFC stage while in standby, the measurement error of the line voltage is minimal, and can be neglected. Connect the ammeter in the neutral line to avoid high-frequency noise and capacitive coupling from adding to the current measurement reading.

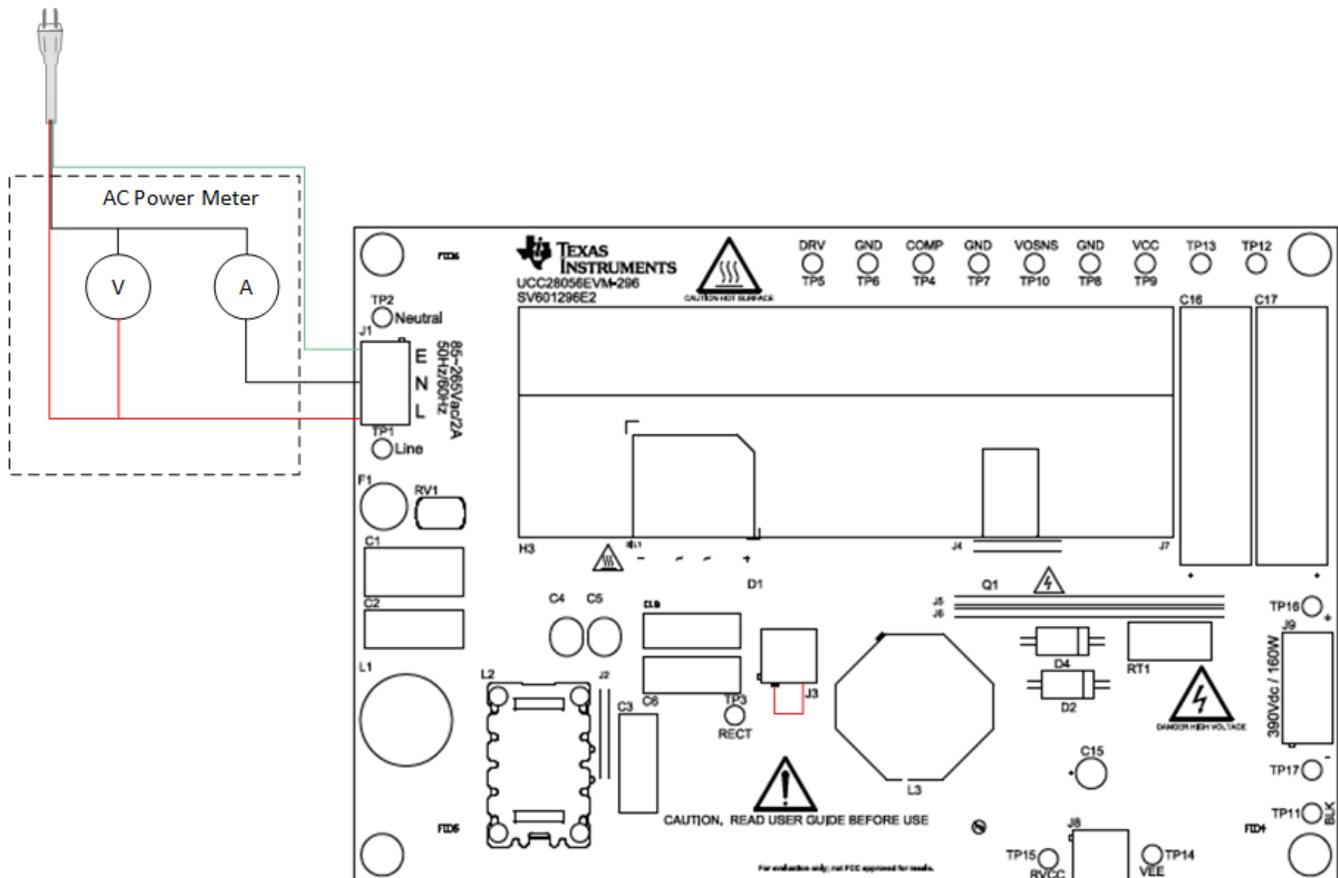


Figure 4. AC Power Meter Connections

Greater precision in both the line voltage and line current measurement lowers the noise floor of the measurement and minimizes the amount of error that is integrated over the measurement interval. Using the lowest possible voltage range is recommended. The current range must be large enough to measure the peak line current during the burst period. It is recommended to use a current probe to measure the peak line current and select a current range just above the maximum measured line current.

6.2 Average Input Power Calculation

In integration mode, the power meter calculates the amount of mWh the PFC stage consumes during the measurement interval. The average input power can then be calculated using Equation 30.

$$P_{avg} = \frac{mWh_{measured} \cdot 60_{minutes}}{t_{interval}(minutes)} \quad (30)$$

6.3 Standby Power and Efficiency Measurement

Table 6 summarizes the standby power measurement of the PFC design from 85 VAC to 265 VAC.

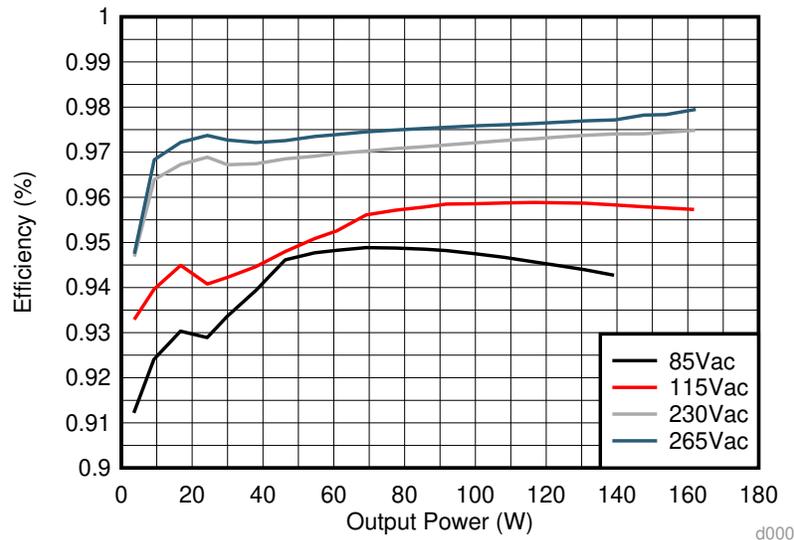
Table 6. Standby Power Measurement of UCC28056

INPUT VOLTAGE (Vrms)	INPUT POWER (mW)	VCC VOLTAGE	VCC CURRENT (µA)	TOTAL STANDBY POWER (mW)
85	23	12.0074	104.034	24.249
115	24	12.0101	107.022	25.285
230	39	12.0632	105.630	40.268

Table 6. Standby Power Measurement of UCC28056 (continued)

INPUT VOLTAGE (V _{rms})	INPUT POWER (mW)	VCC VOLTAGE	VCC CURRENT (μA)	TOTAL STANDBY POWER (mW)
265	45	12.0630	105.902	46.272

Figure 5 summarizes the efficiency performance across line and load of UCC28056.


Figure 5. Efficiency versus Output Power of the UCC28056

7 Summary

The UCC28056x offers superior standby power and efficiency performance across the entire load range, and empowers designs to meet the latest power standards. Burst mode operation of the UCC28056x allows for high light-load efficiency which enables the design to keep the PFC on even in low-power modes. By allowing the PFC to always be on, it simplifies the overall system complexity and simplifies the design of downstream converters by allowing for a tighter input voltage range.

8 References

1. Texas Instruments, [A Design Review of a Full-Featured 350-W Offline Power Converter Technical Reference](#)
2. Texas Instruments, [Power Stage Designer™ User's Guide](#)
3. Texas Instruments, [UCC28056x Selection Guide Application Note](#)

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (August 2019) to B Revision	Page
• Edited application report for clarity	1
• Updated Figure 1 to reflect new boost inductance value	3

Changes from Original (February 2018) to A Revision	Page
• Replaced UCC28056 to UCC28056x.....	1
• Changed specifics for UCC28056 in Section 4	4
• Added burst mode variation for various devices	4
• Changed specifics to UCC28056 in Table 6	11
• Added link to selection guide.....	12

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