Application Report
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Power Factor Correction design for On-Board Chargers in Electric Vehicles

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ABSTRACT

This application note discusses the design comparison of a Continuous Conduction Mode (CCM) Power Factor Controller (PFC) versus a two-phase interleaving CCM PFC for on-board chargers in electric vehicles. An on-board charger (OBC) is generally a two-stage design with a boost topology power factor correction (PFC) stage followed by an isolated DC-DC stage.

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Trademarks

1 Introduction

A common AC/DC block diagram solution for the on-board charger is shown in Figure 1. [1] An OBC takes as input AC voltage from the grid and converts to DC voltage in order to charge the electric vehicle traction battery. This AC-DC system is located within the hybrid electric vehicle and electric vehicle (HEV/EV). Figure 1 is not detailing isolation boundaries however the UCC21521-Q1 can be used to cross the isolation barrier and drive the Phase-Shifted Full-Bridge (PSFB) MOSFETs.

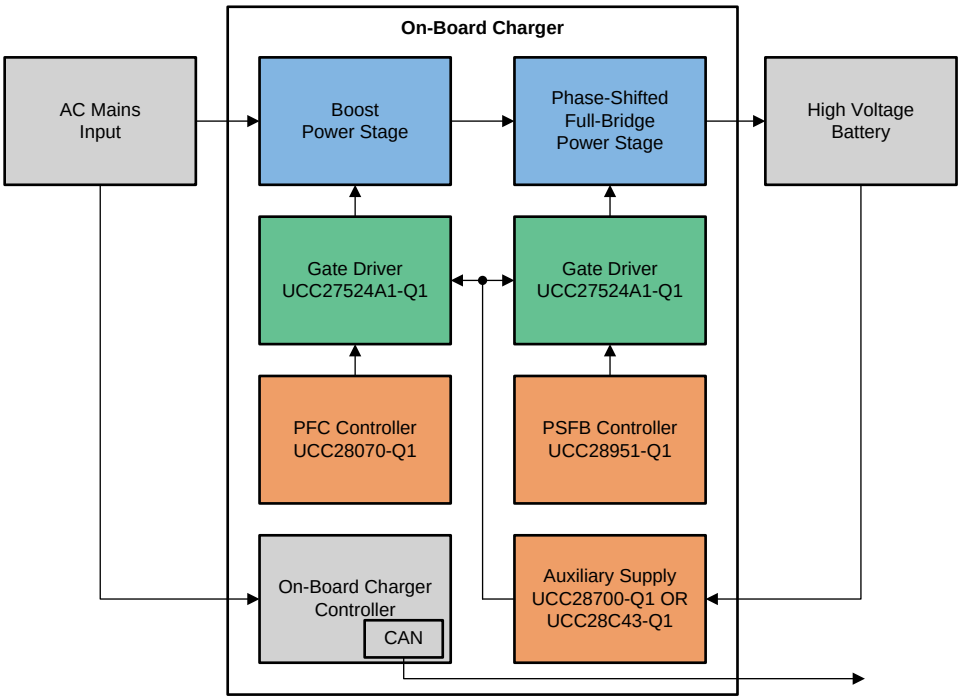

Figure 1. On-Board Charger Block Diagram Example

The same AC-DC system may be found in electric vehicle charging stations, also known as electric vehicle service equipment (EVSE), where non-automotive grade components can be utilized. When HEV/EV OBCs are serviced by an EVSE, the Society of Automotive Engineers standard has established Levels 1 and 2: Level 1 is 120/230 VAC at 12 to 16 A input while Level 2 uses 208 ~ 240 VAC at 15 to ~ 80 A input. These EVSE charger powers are therefore up to ~ 3 kW for level 1 versus ~ 20 kW for level 2. [2]

At these input power levels, the boost power stage should be designed using a PFC controller. Depending on the power level output from the OBC, a single-phase UCC2818A-Q1 controller or a two-phase interleaved UCC28070-Q1 controlled can be selected; both are analog based controllers operating in CCM PFC mode.

There are also Level 3 EVSEs that consists of an external charger supplying high voltage 300 to 750 VDC up to 400 A to the automobile. For these power levels a digital based system is preferred still requiring a PFC where the PFC is typically a Vienna Rectifier. [3] Digital based systems may also be preferred in Level 2 systems. [4] There are also digital bridgeless PFC GaN designs. [5, 6] These design solutions will not be included in this application report.

The remainder of this application report will detail the equations to design the CCM PFC power stage components for the single-phase versus two-phase interleaved designs, an example design will be used as a comparison on the component choices, followed by some reference design examples.

2 Single-phase CCM PFC Design

A typical circuit showing a CCM boost PFC is shown in Figure 2 using a single-phase UCC2818A-Q1 controller; note input filtering or inrush limiting components are not shown. If non-automotive grade components are preferred then the UCC28180 or the UCC28019 controllers can be selected.

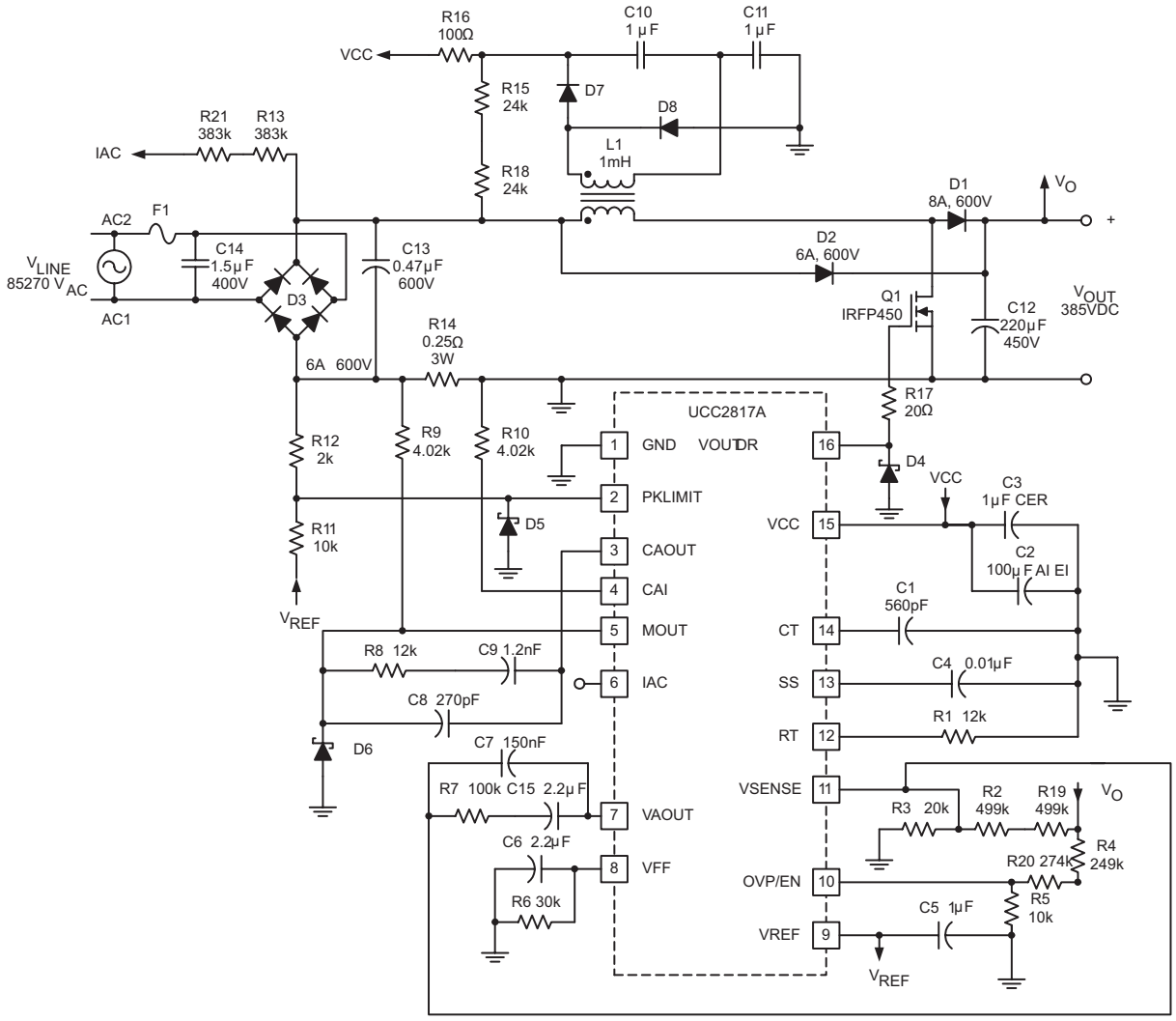

Figure 2. Typical Application Circuit that can be used with the UCC2818A-Q1

In addition to providing the key power train component design equations, an example calculation will be provided based on the design specifications shown in Table 1. The 1 kW output is used in the example in order to compare to reference designs found later in this application note. The following key power train component design equations are also provided in the UCC28180 datasheet.

Table 1. Design Specifications for Calculated Example

	PFC
Input Voltage Range (V_{RMS})	90 - 265
Output Voltage (V)	380, 300 minimum during t_{HOLDUP}
Output Power (W)	1000
Efficiency (η) Target	97 %
Power Factor (PF) Target	0.99

The bridge rectifier (D3) must be rated to handle the $I_{IN(max)}$ and $I_{IN\_AVG(max)}$ current after derating criteria:

$$I_{IN(max)} = \sqrt{2}\frac{P_{OUT(max)}}{\eta V_{IN(min)} PF} = \sqrt{2} \times \frac{1000}{0.97 \times 90 \times 0.99} = 16.4\,A$$

$$I_{IN\_AVG(max)} = \frac{2}{\pi} I_{IN(max)} = \frac{2}{\pi} \times 16.4 = 10.4 \text{ A}$$

Where η is the target efficiency for the design which can be better estimated after the first pass design is completed using calculated power loss values to determine the new efficiency and PF is the target power factor for the design

The boost inductor (L1) maximum current and inductance value are determined by the following equations:

$$I_{L\_PEAK(max)} = I_{IN(max)} + \frac{\Delta I}{2}$$

$$L_{BOOST} \geq \frac{V_{OUT}\, D(1-D)}{\Delta I f_s}$$

Where V_{OUT} is the output voltage of the PFC stage, D is duty cycle, ΔI is inductor ripple current, and f_s is switching frequency.

Assuming the boost inductor ripple current is 40 % of $I_{IN(max)}$, a duty cycle of 0.5, and a switching frequency of 60 kHz, the boost inductor minimum is calculated to be:

$$I_{L\_PEAK(max)} = 16.4 + \frac{0.40 \times 16.4}{2} = 19.7 \text{ A}$$

$$L_{BOOST} \geq \frac{380 \times 0.5 \times 0.5}{0.40 \times 16.4 \times 120{,}000} = 120 \ \mu\text{H}$$

The output capacitor (C12) is in part based on holdup time required for supporting the load after input ac voltage is removed and is given by the following equation:

$$C_{OUT} \geq \frac{2 P_{OUT(max)}\, t_{HOLDUP}}{V_{OUT}^{\ 2} - V_{OUT(min)}^{\ 2}}$$

Where P_{OUT} is the output power from the PFC stage, t_{HOLDUP} is the desired holdup time when there is loss of input grid power to allow the OBC to safely shutdown in a know state, and V_{OUT} and $V_{OUT(min)}$ are the capacitor voltage change during the holdup time.

The output of the PFC stage should not fall below 300 V during one line cycle (20 ms at 50 Hz) in this design example, therefore the minimum calculated output capacitor is:

$$C_{OUT} \geq \frac{2 \times 1000 \times 0.020}{380^{\,2} - 300^{\,2}} = 735 \ \mu\text{F}$$

However, in practice the capacitor output ripple voltage, the capacitor ESR, or the capacitor RMS ripple current rating may require a capacitor value resulting in a different capacitance value then calculated based on t_{HOLDUP} alone.

The total rms capacitor current contributed by the PFC stage for D > 50 % is approximated by:

$$i_{1\varnothing} = \frac{P_{OUT}}{V_{OUT}} \sqrt{\frac{16\ V_{OUT}}{3\pi\sqrt{2} V_{IN\_MIN}} - 1} = \frac{1000}{380} \sqrt{\frac{16 \times 380}{3 \times \pi \times \sqrt{2} \times 90} - 1} = 5.3\,\text{A}$$

The rms capacitor current consists of a low frequency ripple current at twice the line frequency as well as a high frequency ripple current at the PFC switching frequency and its harmonics. The rms current calculation is a slightly modified version of the formula in Erickson and Maksimovic's "Fundamentals of Power Electronics" to calculate the RMS total capacitor ripple current. This formula ignores the effect of inductor switching-frequency ripple current and thus underestimates the current when compared to a numerical simulation. This underestimation becomes proportionally greater at high line, but because ripple currents are greatest at low line, The $i_{1\varnothing}$ equation is accurate to better than about 10%. [7] For a more detailed set of current equations, reference "Analytic Expressions for currents in the CCM PFC stage." [8]

The current through the power MOSFET (Q1) is given by the following equation:

$$I_{DS\_RMS} = \frac{P_{OUT(max)}}{\eta V_{IN\_RECTIFIED(min)}} \sqrt{2 - \frac{16 V_{IN\_RECTIFIED(min)}}{3\pi V_{OUT}}}$$

Where: $V_{IN\_RECTIFIED(min)}$ is $\sqrt{2}V_{IN(min)}$

Following with the calculation example inputs,

$$I_{DS\_RMS} = \frac{1000}{0.97 \times \sqrt{2} \times 90} \times \sqrt{2 - \frac{16 \times \sqrt{2} \times 90}{3 \times \pi \times 380}} = 9.7 \text{ A}$$

The current through the boost diode is

$$I_{OUT(max)} = \frac{P_{OUT(max)}}{V_{OUT}} = \frac{1000}{380} = 2.6 \text{ A}$$

The MOSFET gate drive selection details can be found in the TI Tech Note "Pairing the PFC controller with Gate Drivers in On-Board Chargers for Electric Vehicles" [1]

Specific to the rest of the UCC2818A-Q1 design and component selection on controller settings, feedback, start-up, etc., reference the datasheet. [9]

3 Two-phase Interleaved CCM PFC Design

A typical circuit showing a two-phase interleaved CCM boost PFC is shown in Figure 3 using a single-phase UCC28070-Q1 controller. The following key power train component design equations can be found in the design note "UCC28070 300-W Interleaved PFC Pre-Regulator Design Review." [10]

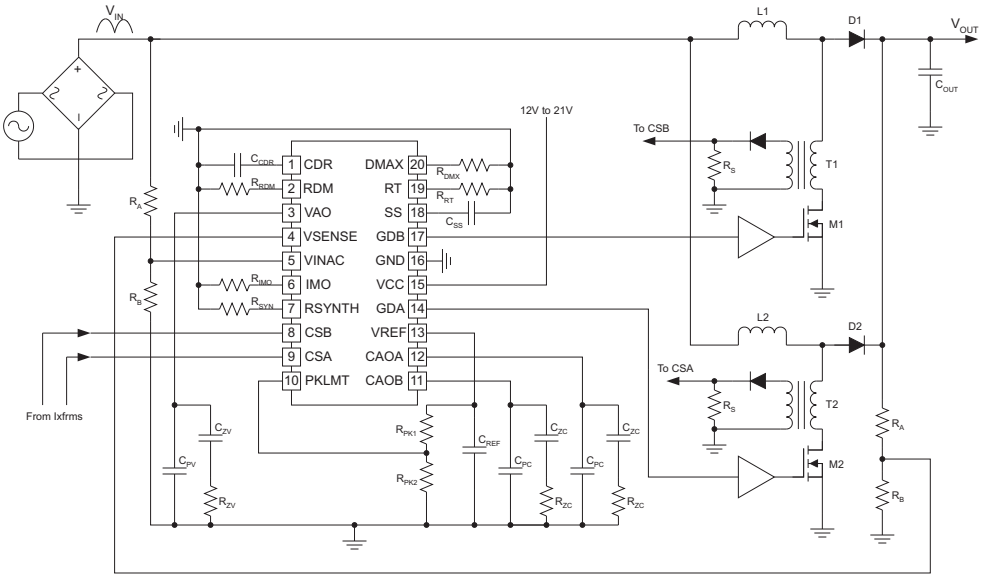

Figure 3. Typical Application Circuit sing the UCC28070-Q1

The benefit to an interleaved boost PFC is the inductor ripple current reduction seen by the input and output capacitors of the boost stage. Figure 4 shows K(D), the ratio of input ripple current (ΔI_{IN}) to individual inductor ripple current (ΔI_{L1}), for a two-phase interleaved PFC as a function of duty cycle (D).

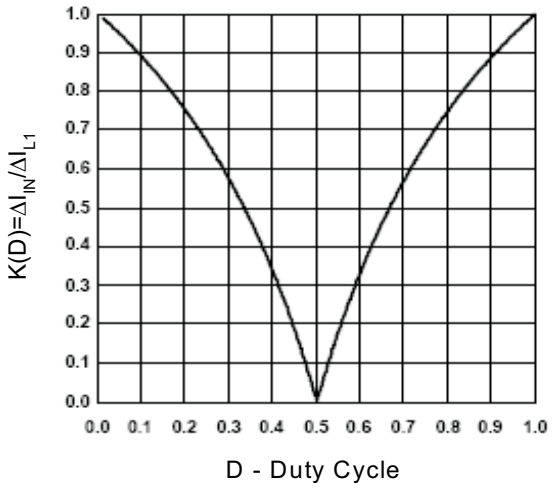

Figure 4. Input Inductor Ripple Current Cancellation

The duty cycle is not constant and varies with changes in line phase input voltage. At low line the duty cycle will vary from 100 % to 69 % and at high line the duty cycle will vary from 100 % to 2 %. Therefore, the inductor ripple current cancellation will not be 100 % throughout the line cycle. [11] Notice that if the interleaved boost PFC could operate only at 50 % duty cycle then the ripple current reduction is completely cancelled. Duty cycles other than 50 % still result in smaller ripple currents as seen on the input and output capacitors. The ripple current at twice line frequency is unaffected by interleaving therefore to a rough approximation there is no reduction in low frequency (100 Hz to 120 Hz) ripple and about 50% reduction in the high frequency ripple.

The equations for K(D) are:

$$K(D) = \frac{\Delta I_{IN}}{\Delta I_{L1}}$$

$$K(D) = \frac{1-2D}{1-D} \text{ if D is} \leq 0.5$$

$$K(D) = \frac{2D-1}{D} \text{ if D is} > 0.5$$

In the design example so far:

$$D = \frac{V_{OUT} - \sqrt{2}V_{IN\_MIN}}{V_{OUT}} = \frac{380 - \sqrt{2} \times 90}{380} = 0.66$$

$$K(D) = \frac{2 \times 0.66 - 1}{0.66} = 0.48$$

The bridge rectifier must be rated to handle the $I_{IN(max)}$and $I_{N\_AVG(max)}$ current after derating criteria:

$$I_{IN(max)} = \sqrt{2}\,\frac{P_{OUT(max)}}{\eta V_{IN(min)} PF} = \sqrt{2} \times \frac{1000}{0.97 \times 90 \times 0.99} = 16.4 \text{ A}$$

$$I_{IN\_AVG(max)} = \frac{2}{\pi} I_{IN(max)} = \frac{2}{\pi} \times 16.4 = 10.4 \text{ A}$$

The boost inductors (L1 and L2) value is determined by the following equations with a 30 % assumption on the inductor ripple current ΔI and a 120 kHz switching frequency:

$$\Delta IL = \frac{\sqrt{2}P_{OUT}\,\Delta I}{\eta V_{IN(min)} K(D)} = \frac{\sqrt{2} \times 1000 \times 0.3}{0.97 \times 90 \times 0.48} = 10.1$$

$$L_1 = L_2 = \frac{\sqrt{2}V_{IN(min)} D}{\Delta IL\, f_s} = \frac{\sqrt{2} \times 90 \times 0.66}{10.1 \times 120{,}000} = 69\ \mu H$$

$$I_{L\_pk(max)} = \frac{\sqrt{2}}{2}\frac{P_{OUT}}{\eta V_{IN_{MIN}}} + \frac{\Delta I}{2} = \frac{\sqrt{2} \times 1000}{2 \times 0.97 \times 90} + \frac{10.1}{2} = 13.1 \text{ A}$$

Notice when compared to the previous single-phase CCM boost inductor design, the inductance value is smaller even though there is a larger amount of ripple current in each inductor resulting in a smaller over all sized inductor. An interleaved design can accommodate a larger inductor ripple current and can operate at high switching frequencies due to the ripple cancellation effect.

The output capacitor (C_{OUT}) is in part based on holdup time required for supporting the load after input ac voltage is removed and also keeping the capacitor ripple voltage within acceptable limits. A capacitance value of approximately 0.6 uF per Watt of output power is sometimes used for an initial estimate on the capacitor sizing. In the design example the output capacitance estimation is 600 uF. Either method for calculating the output capacitor can be utilized; the interleaved design is 600 uF versus the single phase design which is calculated to 735 uF. The capacitor output ripple voltage, ESR value, and RMS ripple current may result in a capacitor sizing different from this 0.6 uF per Watt estimation.

The advantage in a two-phase interleaved CCM PFC design is when considering the ripple current reduction in C_{OUT} between single- and two-phase interleaved CCM.

$$i_{2\varnothing} = \frac{P_{OUT}}{V_{OUT}}\sqrt{\frac{16V_{OUT}}{6\pi\sqrt{2}V_{IN\_MIN}} - 1} = \frac{1000}{380}\sqrt{\frac{16\times380}{6\times\pi\times\sqrt{2}\times90} - 1} = 3.3\ A$$

With the capacitor RMS current smaller, smaller sized capacitors may be chosen based on the ESR rating of the capacitor. Note that in the literature, The $i_{2\varnothing}$ equation has several different factors for the first term under the square root but circuit simulations and ultimately verification on the final design will be performed and these calculations are meant to start component selections. [12,13] For a more detailed set of current equations, reference "Analytic Expressions for currents in the CCM PFC stage." [8]

The current though the power switches (M1 and M2) is given by the following equation:

$$I_{DS\_RMS} = \frac{P_{OUT(max)}/2}{\eta V_{IN\_RECTIFIED(min)}} \times \sqrt{2 - \frac{16V_{IN\_RECTIFIED(min)}}{3\pi V_{OUT}}}$$

Where $V_{IN\_RECTIFIED(min)}$ is $\sqrt{2}V_{IN(min)}$

Notice how only half the power is used for each power switch current calculation.

Following with the calculation example inputs,

$$I_{DS\_RMS} = \frac{1000/2}{0.97\times\sqrt{2}\times90} \times \sqrt{2 - \frac{16\times\sqrt{2}\times90}{3\times\pi\times380}} = 4.8\ A$$

This is lower rms current per MOSFET then in the single-phase CCM PFC design so a higher R_{DSON} MOSFET can be utilized in each phase. Higher R_{DSON} MOSFETs tend to have lower capacitances resulting in lower switching losses.

The current through each boost diode is

$$I_{OUT(max)} = \frac{P_{OUT(max)}/2}{V_{OUT}} = \frac{1000/2}{380} = 1.3\ A$$

The MOSFET gate drive selection details can be found in the TI Tech Note "Pairing the PFC controller with Gate Drivers in On-Board Chargers for Electric Vehicles" [1]

Specific to the rest of the UCC28070-Q1 design and component selection on controller settings, feedback, start-up, etc., reference the datasheet. [14]

4 Transition-Mode PFC Design

The transition-mode (TM), also known as boundary conduction mode (BCM) or critical conduction mode (CrCM), PFC could also be considered in OBC PFC designs however it is not recommended for designs greater than 300 W loading. GaN based designs may allow TM up to higher powers. The TM PFC can also be interleaved using the UCC28061-Q1 and can then be used in designs up to 1000 W loading. TM PFC designs would find applications in HEV/EV special-purpose vehicles that have OBC requirements less than found in a Level 1 system. These vehicles include small task-oriented vehicles (carts, utility task, and all-terrain) and personal transportation devices (e-bikes, scooters, wheelchairs, even skateboards).

Since Level 1 OBCs are typically up to ~3 kW, TM PFCs are not considered because of the advantages of a CCM PFC design. The key difference between the TM and CCM PFC design is the amplitude and ripple profile on the input current to the PFC stage (the current after the EMI filter). Reference the Power Supply Design Seminar "Designing High-Power Factor Off-Line Power Supplies" [15] and the High Voltage Interactive Training Series "PFC for not dummies" [16] to get a better understanding on differences between TM and CCM PFC. In short, there is larger ripple current in a TM PFC affecting the switching

losses in the power switch and the boost inductor however the boost diode power losses are higher in the CCM PFC due to reverse recovery which can be lowered when a SiC boost diode is used, in fact using a SiC diode is almost mandatory at OBC power levels. CCM PFC could reduce the EMI filter design not just in consideration of lower ripple currents but CCM mode uses fixed frequency control versus variable frequency control in TM PFC designs.

5 Single-phase versus Two-phase Interleaved CCM PFC BOM Comparison based on Example Design

Tabulating the example design calculations for the single and two-phase interleaved PFC CCM, Table 2 compares the different results. The previous Table 1 states the design requirements used for the comparison data.

Table 2. BOM Comparison for Calculated Example

	Single-phase CCM PFC		Two-phase Interleaved CCM PFC	
	Quantity	Description	Quantity	Description
Switching Frequency		120 kHz		120 kHz - the individual phases run at 60 kHz
Input Rectifier	1	$I_{IN\_AVG(max)}$ = 10.4 A I_{IN_MAX} = 16.4 A	2	$I_{IN\_AVG(max)}$ = 10.4 A I_{IN_MAX} = 16.4 A
Boost Inductor	1	Ripple current = 40 % $I_{L\_PEAK(max)}$ = 19.7 A Inductance = 120 µH	2	Ripple current = 30% $I_{L\_PEAK(max)}$ = 13.1 A Inductance = 69 µH
Power Switch	1	9.7 A	2	4.8 A
Boost Diode	1	2.6 A	2	1.3 A
Output Capacitor	1	735 µF Ripple current = 5.3 A	1	600 µF Ripple current = 3.3 A
Gate Driver	1	Single Low-Side	2	Single Low-Side

Referring to Table 2, the differences between a single-phase versus two-phase interleaved CCM PFC is:

- Each boost inductor is smaller in the two-phase interleaved design resulting in the possibility of a smaller printed circuit board area needed for the total boost inductor design even though two inductors are needed in the two-phase interleaved design.
- The power switch current is less in the two-phase interleaved boost converter so a smaller R_{DSON} MOSFET could be used even though two MOSFETs are required.
- Interleaving can reduce the ripple current in the output capacitor so a smaller capacitor could be used in the two-phase interleaved design provided the capacitor output ripple voltage, ESR value, and RMS ripple currents are within the design goal and capacitor derating.
- Two MOSFET gate drivers and two boost diodes are needed in the two-phase interleaved design.
- There is less power dissipated in the inductor and power switches in the two-phase interleaved design and this makes thermal management easier since not only could the total power losses be smaller but the heat is distributed across more components increasing the surface area for component cooling design.

In the reference "An Interleaved PFC Preregualtor for High-Power Converters" [11] several benefits of a two-phase interleaved design were concluded:

- The overall input ripple current of a two-phase interleaved PFC boost will be 55 % of what it would have been in the same power and inductance for a single-phase PFC design.
- Up to a 25 % reduction in magnetic transformer volume with a two-phase interleaved PFC.
- The EMI filter could also be decreased in size not only due to the reduction in ripple current on the input but also if reducing the switching frequency is considered.

These differences are key items to consider in deciding when to using the two-phase interleaved CCM PFC versus a single-phase CCM PFC design. For a given design, a quick calculation for single-phase versus two-phase interleaved CCM PFC should be conducted using the above quick calculations followed by a component optimization selection based on the component Figure-of-merits, i.e. capacitor ESR, MOSFET R_{DSON}, boost inductor sizing, etc. Once the critical power train components are selected, a cost estimate can be examined to determine the optimal PFC design.

6 Single-phase and Two-phase Interleaved CCM PFC Reference Designs

Two reference designs provide real examples to compare trends between a single-stage versus two-phase interleaved CCM PFC designs: PMP11062 Universal AC Input, 380V/1kW CCM Boost Power Factor Regulator Reference Design [17] as the single-phase CCM PFC design and PR779A 1.2kW Universal Input Interleaved CCM PFC Power Board [18] as the two-phase interleaved CCM PFC design. Also included will be the TIDM-2PHILPFC Two-Phase Interleaved Power Factor Correction Converter with Power Metering [19] reference design to provide comparison comments between analog versus digital solutions. Note that the reference designs are not optimized to compare the three designs on an equivalent performance design point but are used to highlight design trends with the BOM. These reference designs are only ~1000 W in order to compare back to the previous design calculations and see component optimization trade-offs.

The 1 kW outputs are not power load limits to a CCM PFC design but rather are reference designs that were designed for the 1 kW power output. A CCM PFC can be used in much higher power outputs, i.e. there is the reference design PMP4311 5 KW Interleaved CCM Power Factor Correction Converter [20] using the non-automotive version of the UCC28070 in a two-phase interleaved CCM PFC demonstrating higher power designs where the automotive version of the controller can be substituted for the non-automotive version of the controller.

Table 3 is a comparison on the design specifications for the three reference designs being compared. The three designs are similar “enough” in order to provide some comments on the component BOMs.

Table 3. Design Specifications for the three reference designs

	Single-phase CCM PFC	Two-phase Interleaved CCM PFC	Digital Two-phase Interleaved CCM PFC
Reference Design	PMP11062	PR779A	TIDM-2PHILPFC
Input Voltage (V_{RMS})	120 / 230	120 / 230	120 / 230
Output Voltage (V)	380	390	400
Output Watt (W)	1000	1200	750
Maximum Efficiency	96 % peak @ 120 VAC / 60 Hz 98 % peak @ 230 VAC / 50 Hz	95 % peak @ 115 VAC / 60 Hz 97 % peak @ 230 VAC / 50 Hz	97 % peak
CCM Controller	UCC28180 analog	UCC28070-Q1 analog	C2000 digital

Table 4 compares the three different BOMs.

Table 4. BOM Comparison for the three reference designs

	Single-phase CCM PFC		Two-phase Interleaved CCM PFC		Digital Two-phase Interleaved CCM PFC	
	Quantity	Description	Quantity	Description	Quantity	Description
Input Rectifier	2	600 V, 25 A with HS	1	600 V, 25 A	1	600 V, 15 A
Boost Inductor	1	2.54 mH, 79x43 mm	2	78 uH, 23.2x29,5 mm	2	150 uH
Power Switch	2	650 V, 24 A, 95 mΩ, TO-247	4	500 V, 20 A, 250 mΩ, TO-220V	2	560 V, 12 A, 250 mΩ, TO-220
Boost Diode	1	650 V, 20 A, SiC TO-220	2	600 V, 6A, UltraFast TO-220AC	2	600 V, 10 A, Schottky, TO263-2

Table 4. BOM Comparison for the three reference designs (continued)

Output Capacitor	3	180 uF ALUM, 450 V, 22x25 mm Ripple current rating: 1.8 A @ 120 Hz and 2.5 A @ 10 kHz	3	330 uF ALUM, 450 V, 35x30 mm Ripple current rating: 2.0 A @ 120 Hz and 2.8 A @ 10 kHz	3	100 uF ALUM, 450 V, 18x40 mm Ripple current rating: 0.8 A @ 120 Hz and 1.8 A @ 100 kHz
Controller	1	UCC28180D, SOIC-8	1	UCC28070PW, TSSOP-20	1	TMS320F28035, VQFN-56
Gate Driver	1	UCC27511DBVR Single Low-Side, 4A/8A, SOT-23	4	UCC27322DGN, Single Low-Side, 9A, MSOP8	1	UCC27524DR, Dual Low-Side, 5A, SOIC-8

Comments on the BOM examples:

- The combined surface area of the two-phase interleaved CCM PFC inductors are smaller than the single-phase CCM PFC inductor design.
- The power switches in the two-phase interleaved CCM PFC are smaller than the single-phase CCM PFC power switch but with the paralleling of the MOSFETs in the interleaved design results in the same effective R_{DSON}.
- The digital two-phase interleaved CCM PFC design takes advantage of the reduction in output capacitor ripple current to use smaller valued capacitances.

For the digital based design, Figure 5 shows the TIDM-2PHILPFC block diagram. [21]

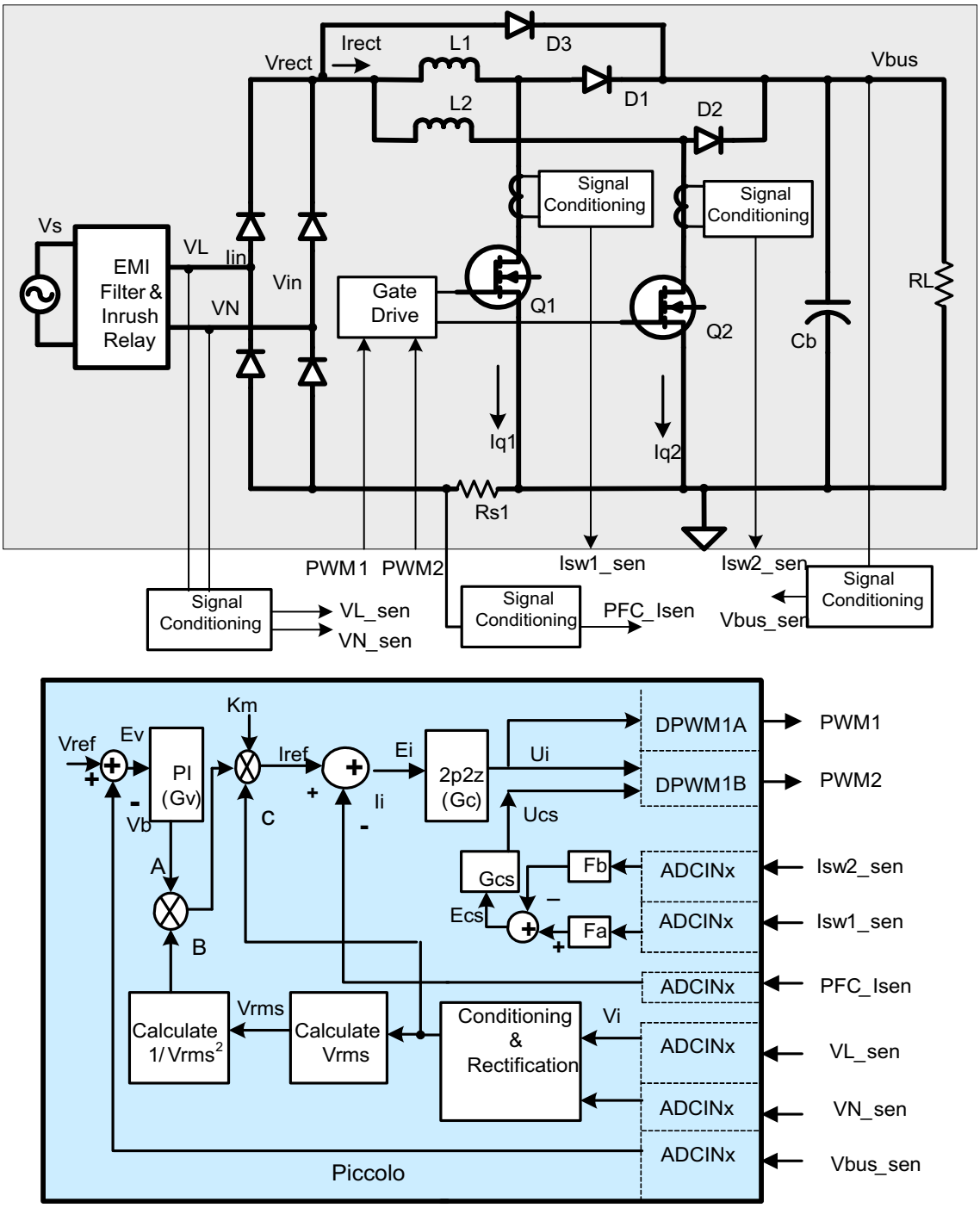

Figure 5. Digital Two-phase Interleaved CCM PFC

To implement digital control, the power train components are still the same. With the analog controller replaced by a digital controller, the digital controller requires signal conditioning blocks shown in Figure 5 to be implemented using discrete components and operational amplifiers. To learn more about the types of operational amplifiers required in a digital design, go to "Selecting operational amplifiers for HEV/EV powertrain systems" [22] of visit the "On-Board (OBC) & Wireless Charger" [23] application support page on TI.com. The largest difference in a digital versus analog design is in the support required for the digital firmware development and the ISO26262 safety certification but the tradeoff is in the flexibility to design in features or operating modes not part of the analog solution.

7 Increasing the Interleaving Count and Paralleling for a CCM PFC

Another important design question is how to achieve greater power outputs from the CCM PFC solution. The UCC28070-Q1 controller can be paralleled as shown in Figure 6. In this configuration, the design uses a single phase line input.

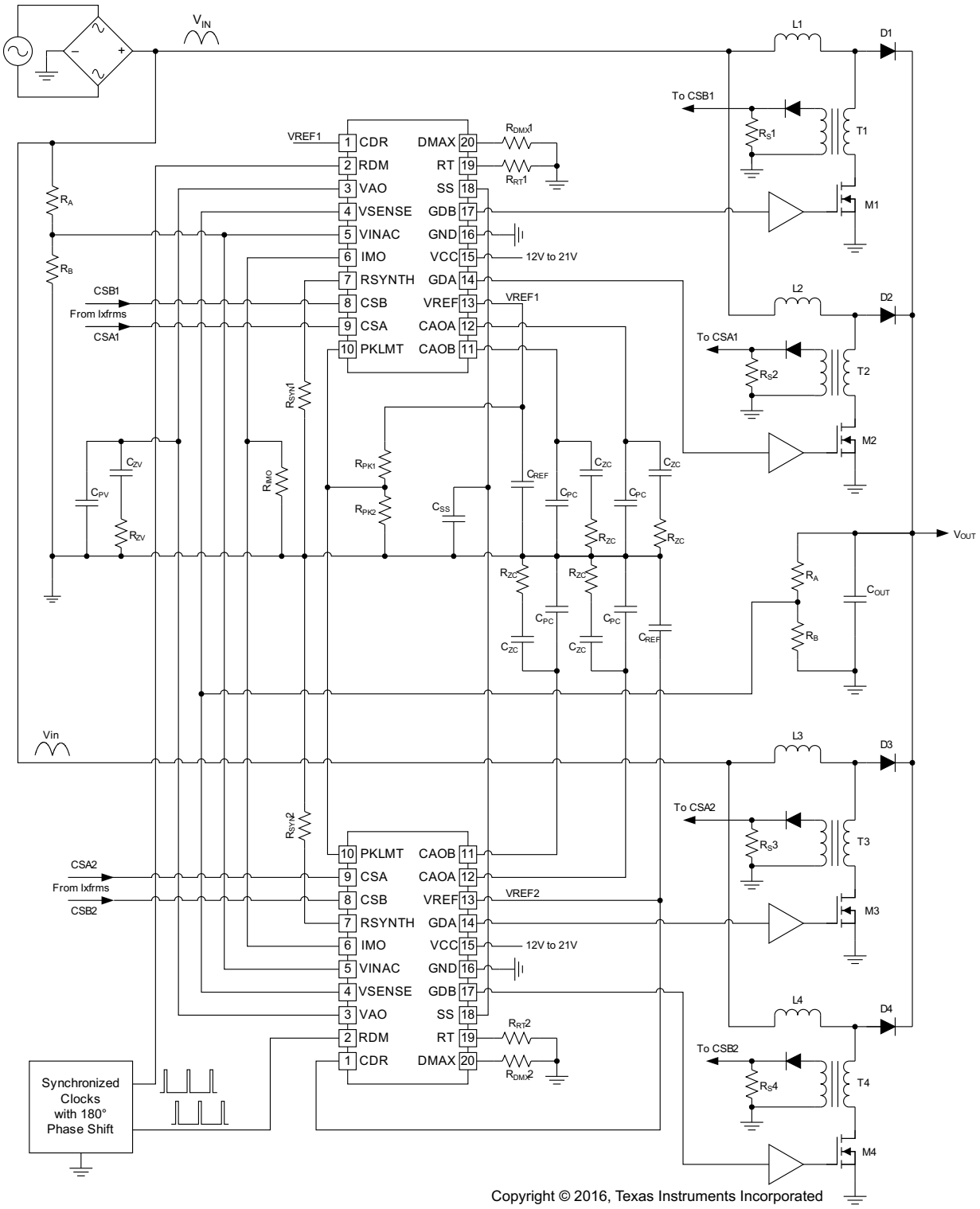

Figure 6. Simplified Four-phase Interleaved Application Diagram Using Two UCC28070 Devices

Figure 6 is a synchronization of two-separate two-phased interleaved CCM designs. A 4-phase interleaved CCM PFC design, where all 4 phases are operating 90 ° from each other, reduces the inductor ripple current further when compared to a 2-phase interleaved CCM PFC design, the two phase are 180 ° from each other, and the reader is directed to section IX in "An Interleaved PFC Preregualtor for High-Power Converters" for information on the ripple reduction. [11]

Another option is to parallel OBC designs for 1 AC input phase across 2 or 3 different AC input phases as shown in Figure 7.

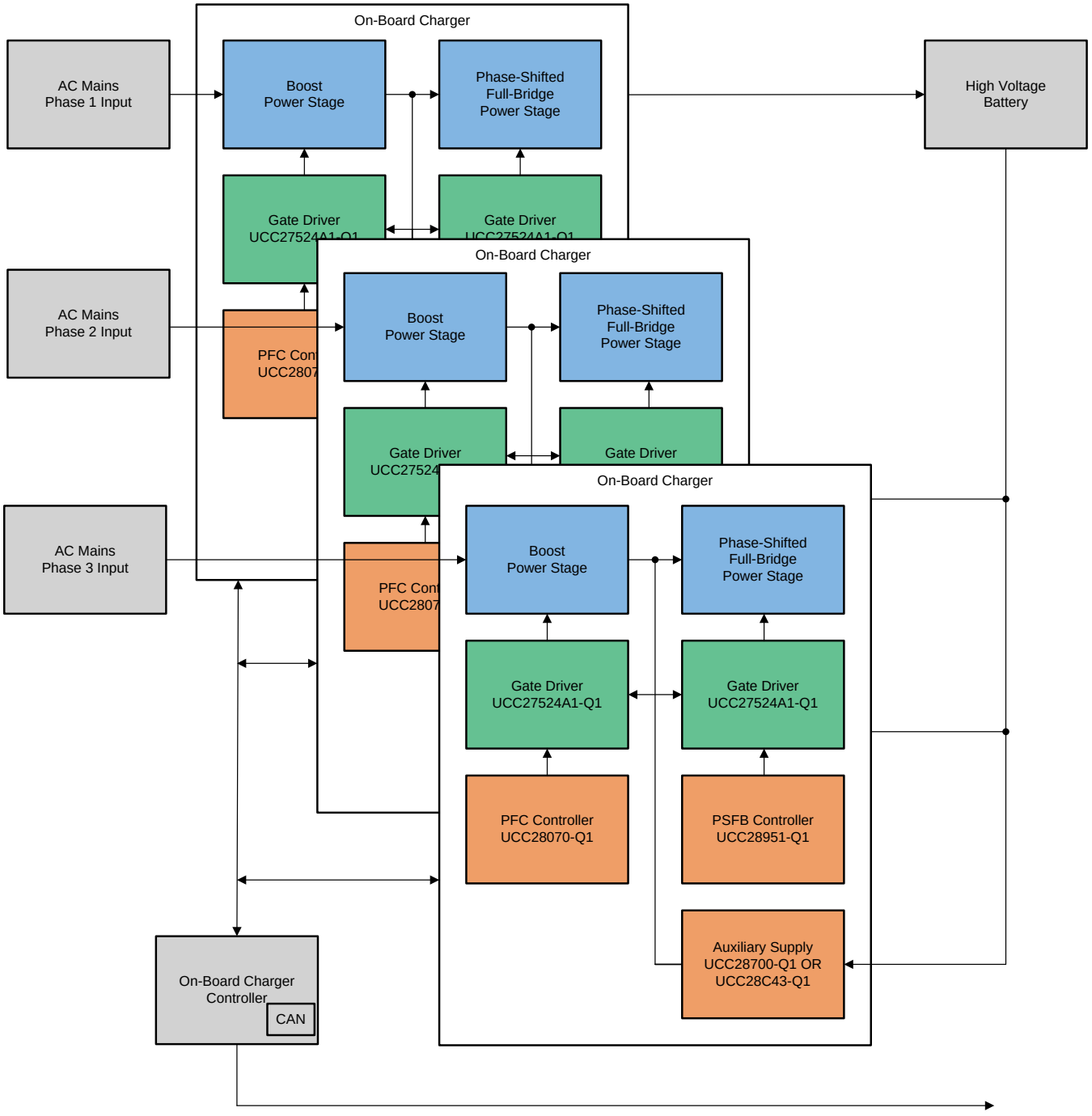

Figure 7. OBC Design Paralleling Designs from 3 AC-Input Phases

In this configuration, the OBC is designed to accommodate a single line phase input. This single line phase OBC system is paralleled with other OBC systems connected to different input line phase grid voltages to scale to the higher power level.

8 Summary

The differences between a single-phase versus a two-phase interleaved CCM PFC are key items to consider in deciding when to using the two-phase interleaved CCM PFC versus a single-phase CCM PFC design; the differences are the boost inductor size and printed circuit board area allocation, the reduction of input and output ripple current seen by the input and output capacitors, EMI filter design, and how the thermal power losses are distributed over the printed circuit board. For a given design, a calculation for single-phase versus two-phase interleaved CCM PFC should be conducted using the quick calculations outlined in this application note followed by a component optimization selection based on the component Figure-of-merits, i.e. capacitor ESR, MOSFET R_{DSON}, boost inductor sizing, etc. Once the critical power train components are selected, a cost estimate can be examined to determine the optimal PFC design.

Several reference designs are provided to see actual implementations of the single-phase versus two-phase interleaved CCM PFC as well as a few comments on a digitally based control design where the effort put into the firmware development is the significant consideration especially in short time-to-market schedules.

The OBC includes more than the PFC itself; it also includes the isolated DC-DC and auxiliary power to control the different electronics in the OBC. For additional information on a complete OBC design, the "Design review of a 2-kW parallelable power supply module" [24] and "Designing multi-kW power supply systems" [25] discuss the other key power subsystems in the OBC design.

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