The TPS370x Family

Application Report

November 1998 Mixed-Signal Products

SLVA045

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Contents

List of Figures

List of Tables

The TPS370x Family

ABSTRACT

This application report describes the TPS370x-xx Supply Voltage Supervisor (SVS) family of devices. The report includes a description of the circuit and a discussion of the differences between members of the TPS370x family. In addition, the report describes circuit features in detail and gives application examples. Layout and design issues are also discussed.

1 Introduction

After power-on, a digital system must be forced into a definite initial state. DSPs, microcomputers and microprocessors have a reset input for this purpose.

In the simple reset solution shown in Figure 1, the reset input is connected to an RC-network, which delivers the necessary reset pulse. After switching on the power supply, this circuit keeps the logic level at the reset input low for a time, determined by the capacitor and the resistor values. The system requires this delay time to complete the initialization and allow the power supply to stabilize.

However, this circuit has some disadvantages. In case of brief reductions in the supply voltage, it does not work correctly. It does not recognize spikes because, due to the capacitor, the voltage at the reset pin does not decrease as fast as the supply voltage. Malfunction is thus possible. If V_{DD} goes down more than 0.7 V, the capacitor discharges quickly through the diode. A small decrease in V_{DD} can destroy the contents of memory and internal registers without activating the reset circuit.

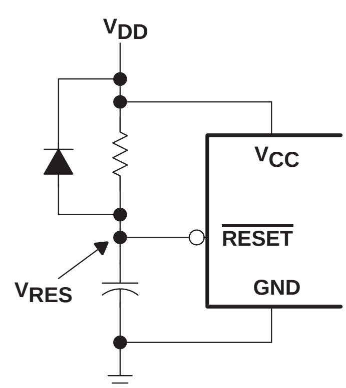

Figure 1. A Simple Reset Solution

If the reliability of a computer system is very important, more complex solutions are available to prevent such errors: when a power-fail interrupt signals dangerous conditions in time, the content of the memory is protected by a battery back-up and so on. In smaller systems, this elaborate protection is too expensive, and, in most applications, not required. It is usually sufficient that, after a serious voltage drop, the microcomputer is forced into a defined initial state.

To achieve this initial state, while preventing the above problems, the following circuit features are required:

- Accurate detection of a voltage drop below the critical voltage
- Generation of a reset signal when the supply voltage is not in the allowed range
- Keeping the reset signal active for a definite time after the supply voltage has returned to its nominal value to ensure proper initialization of the µP or DSP

The Texas Instruments TPS370x Supply Voltage Supervisor (SVS) family of devices fulfills these requirements and integrates other useful features without requiring external components.

2 Circuit Description

This section describes and discusses the circuits and features of the TPS370x SVS devices. Figure 2 shows a graphic overview of the device features.

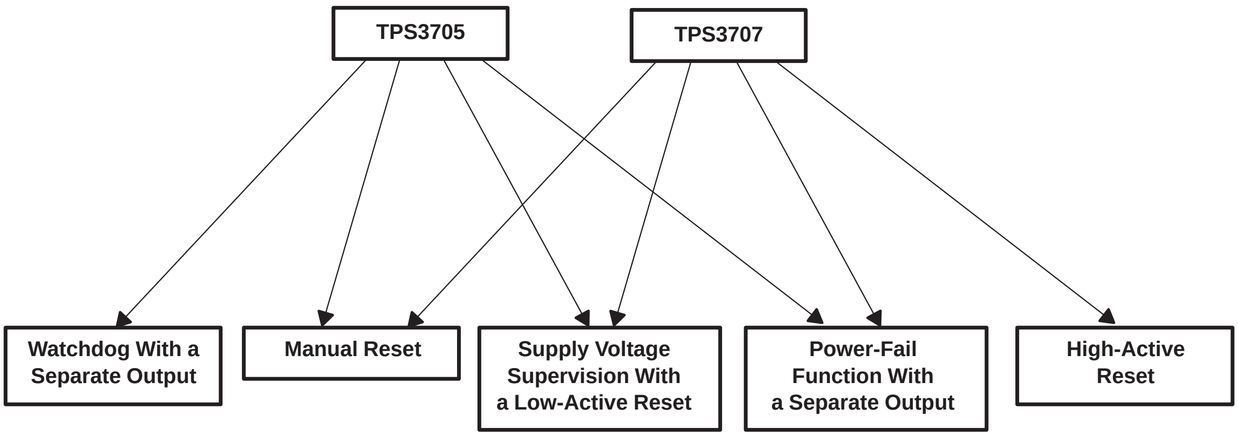

Figure 2. Features Overview

2.1 Supply Voltages Supported

Figure 3 shows the most popular supply voltages supported and supervised by the TPS3705 and TPS3707.

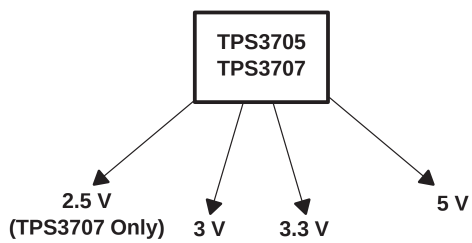

Figure 3. Supply Voltages Supported

2.2 Package Information

The TPS370x is available in the SO (small outline) and the MSOP (micro-small outline) packages. Figure 4 shows the pin assignments for the SO package, and Figure 5 shows the pin assignments for the MSOP package.

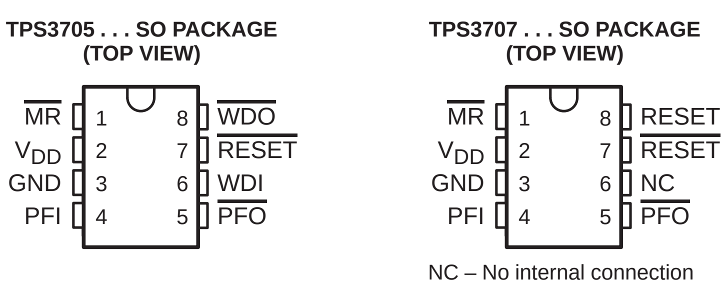

Figure 4. Pin Assignment of the TPS370x in SO Package

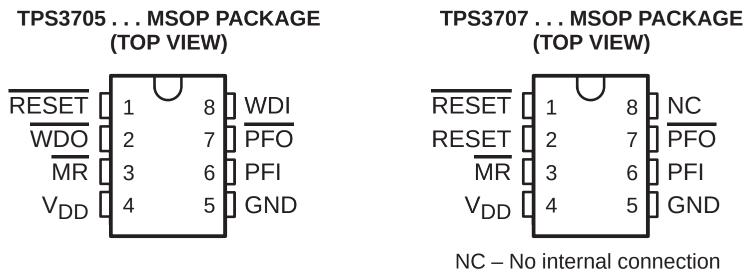

Figure 5. Pin Assignment of the TPS370x in MSOP Package

Table 1 lists the function of the pins.

Table 1. Pin Functions

NAME	STATUS	FUNCTION
V_{DD}	Positive power supply	Supplies the circuit with voltage and supervises the nominal voltage
GND	Negative power supply	Connects the circuit to ground, the zero volt reference for all signals
$\overline{RESET}$	Logic output, low-active	Triggers a low-active reset signal if the supply voltage decreases below the threshold voltage or manual reset is activated
RESET	Logic output, high-active	Triggers a high-active reset signal if the supply voltage decreases below the threshold voltage or manual reset is activated
$\overline{MR}$ manual reset	Logic input	Triggers a reset pulse by an external component. (e.g., a pushbutton can be connected to this terminal to reset the system manually)
PFI power-fail input	Analog input	Supervises a voltage of 1.25 V. It is easy to supervise any other voltage above 1.25 V, by using two external resistors.
$\overline{PFO}$ power-fail output	Logic output, low-active	Signals with logic low, that the voltage at the PFI is below 1.25 V
WDI watchdog input	Logic input	Watchdog input used to reset the internal timer by a positive or negative transition at the pin
$\overline{WDO}$ watchdog output	Logic output, low-active	Watchdog output delivers a logic low signal if the internal timer is not reset in time (after about 1.6 s).

2.3 Block Diagram

The main part of the SVS circuit is a reference voltage source consisting of a very stable temperature-compensated band gap reference. The voltage at the V_{DD} pin is divided by an internal resistor divider and compared with the reference voltage by a comparator. The value of the internal resistors between V_{DD}, the comparator input, and ground depends on the nominal voltage of the device. In sum, these two resistors have a value of 1.2 MΩ. Table 2 lists the nominal resistor values.

Table 2. The Resistor Values of the Internal Voltage Divider Between V_{DD} and Ground

CIRCUIT	R1 TYP	R2 TYP
TPS3707-25	533 kΩ	667 kΩ
TPS370x-30	630 kΩ	570 kΩ
TPS370x-33	688 kΩ	512 kΩ
TPS370x-50	870 kΩ	330 kΩ

The PFI pin compares a voltage with the voltage reference of 1.25 V. If the voltage at PFI is greater than 1.25 V, $\overline{PFO}$ is high, otherwise it is low.

A low signal at $\overline{MR}$ triggers the reset output. An internal 14-kΩ pull-up resistor connected between $\overline{MR}$ and V_{DD} pulls up the input, if it is unconnected.

A transition detector supervises the WDI to reset the watchdog timer at each positive or negative transition. If this input is not electrically connected, an internal driver with a 40-kΩ resistor delivers the necessary transitions in time, so that the $\overline{\text{WDO}}$ stays high.

The reset and watchdog timers are clocked with an internal oscillator. Figure 6 shows a block diagram of the TPS370x.

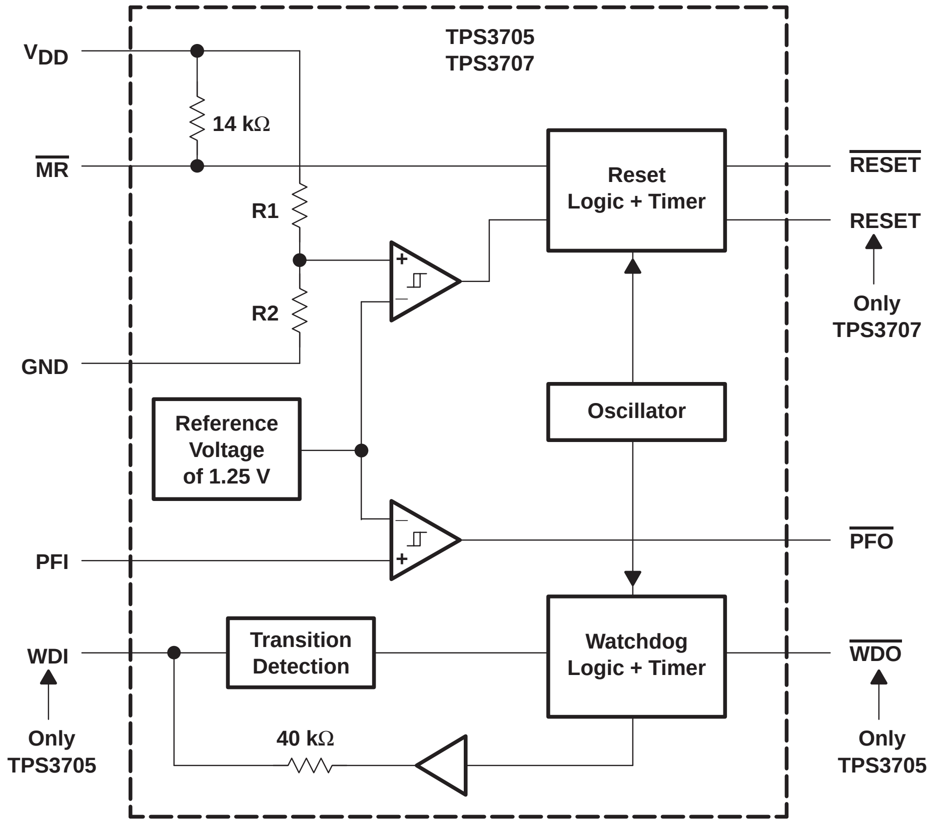

Figure 6. Block Diagram of the TPS370x

3 Supply Voltage Input V_{DD} and Reset Outputs

The following pinout refers to the SO package:

Pin 2: V_{DD}	Supply voltage input
Pin 3: GND	Ground
Pin 7: $\overline{\text{RESET}}$	Reset output – low-active
Pin 8: RESET	Reset output – high-active (only TPS3707)

3.1 Functional Description

An SVS controls the supply voltage and asserts a reset if the voltage at V_{DD} decreases below the negative-going threshold voltage, V_{IT-}. If the supply voltage increases above the positive-going threshold voltage, V_{IT+}, the reset output becomes inactive after about 200 ms. This delay time ensures that a reset sequence can be completed. All TPS370x devices have a low-active reset output. The TPS3707 also has a high-active reset.

The reset output(s) of the SVS start working properly at a voltage greater than 1.1 V and the recommended operating conditions of the power supply (between 2 V and 6 V). The typical supply current for a TPS3707 is about 20 µA, and for a TPS3705 about 30 µA, so that they are well-suited for battery operated systems. Figure 7 shows timing relationships for SVS circuits.

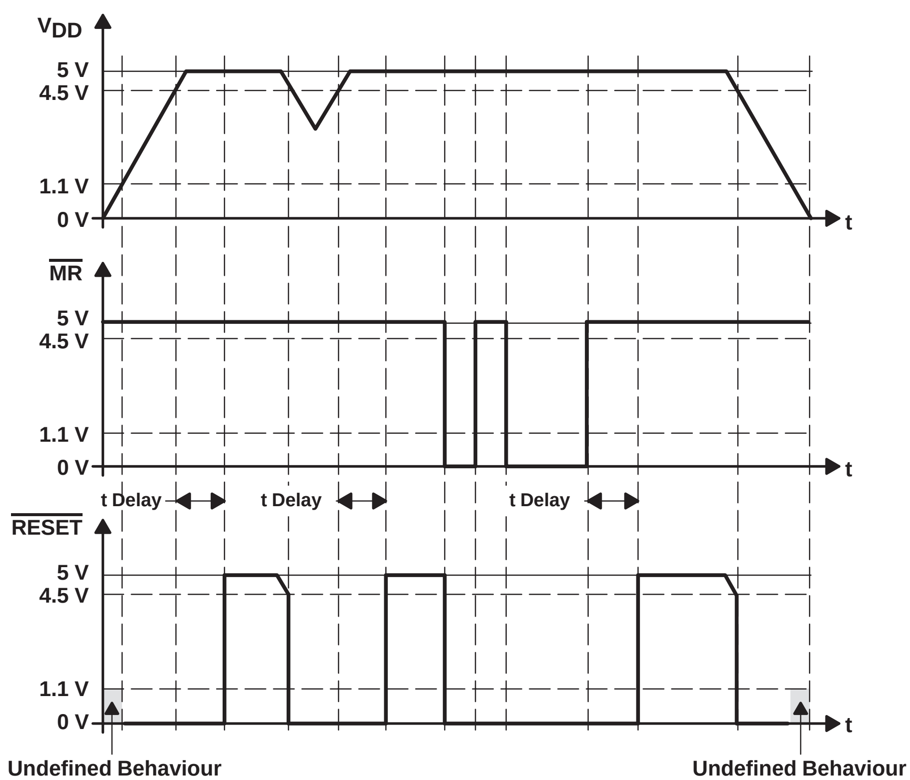

Figure 7. Timing Diagram of V_{DD}, $\overline{\text{MR}}$ and $\overline{\text{RESET}}$ Output (hysteresis neglected)

Hysteresis at the V_{DD} pin improves noise immunity and avoids oscillation at the reset outputs when the supply voltage falls slowly below the critical value. The data sheet specifies negative-going threshold voltage and hysteresis. The positive-going threshold voltage is calculated as $V_{IT+} = V_{IT-} + V_{hys}$. Figure 8 shows V_{DD} hysteresis curves for the TPS370x-50. Table 3 lists typical values of hysteresis at V_{DD}.

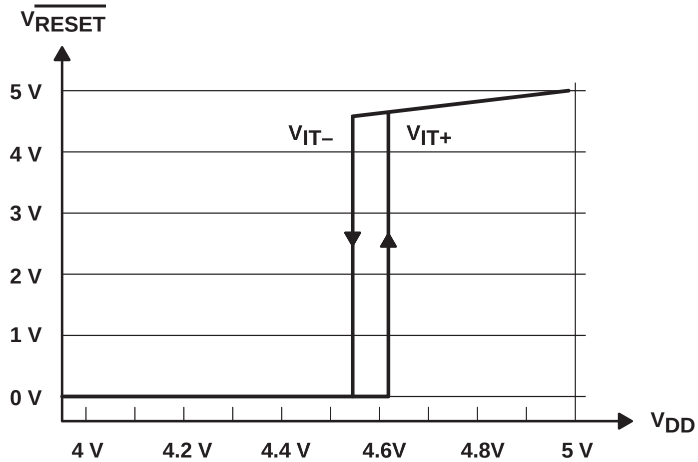

Figure 8. Hysteresis of V_{DD} of the TPS370x-50

Table 3. Typical Hysteresis of V_{DD}

CIRCUIT	TYPICAL HYSTERESIS AT V_{DD}
TPS3707-25	40 mV
TPS370x-30	50 mV
TPS370x-33	50 mV
TPS370x-50	70 mV

3.2 Overview of Reset Conditions

The truth table in Table 4 lists reset input conditions and typical delay times for reset to occur.

Table 4. Truth Table of Reset Influencing Inputs and Delay Times

V_{DD} > VIT	$\overline{MR}$	$\overline{RESET}$	RESET	DELAY TIME (TYPICAL)
1	H → L	H → L	L → H	30 ns
1	L → H	L → H	H → L	200 ms
1 → 0	H	H → L	L → H	3 µs
0 → 1	H	L → H	H → L	200 ms

3.3 Diagram of Breakdown Voltage with Pulsewidth

The supply voltage decreasing below the negative-going threshold voltage, V_{IT-}, asserts the low-active reset. This function operates if the supply voltage falls 200 mV below V_{IT-} for a duration of at least 6 µs. Figure 9 shows the relation between breakdown voltage and pulsewidth at V_{DD}. The SVS for this measurement, the TPS370x-33, was supplied with 3.3 V. The negative-going threshold voltage is approximately 2.93 V.

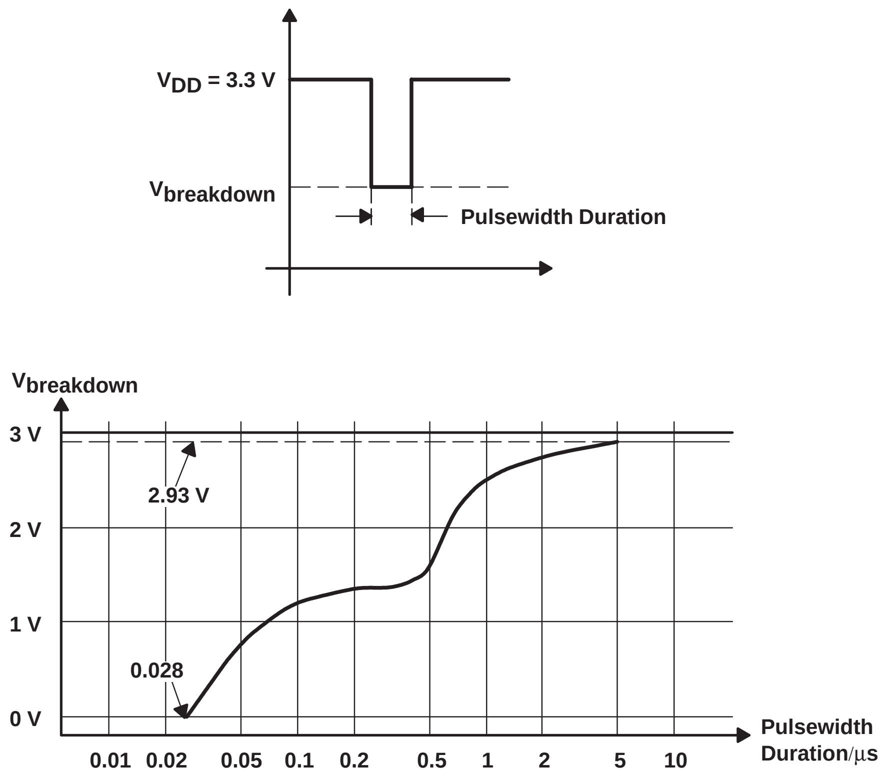

Figure 9. Typical Diagram of TPS370x-33 Breakdown Voltage with Pulsewidth

3.4 Threshold Voltages

Table 5 shows the minimum, typical, and maximum values of negative-going threshold voltages at V_{DD} over the temperature range from –40°C to 85°C. When this voltage is decreased, the $\overline{RESET}$ output goes active.

Table 5. The Negative-Going Threshold Voltages

CIRCUIT	MINIMUM	TYPICAL	MAXIMUM
TPS370x-25	2.20 V	2.25 V	2.30 V
TPS370x-30	2.57 V	2.63 V	2.69 V
TPS370x-33	2.87 V	2.93 V	3 V
TPS370x-50	4.45 V	4.55 V	4.65 V

3.5 Basic Application of the SVS

Figure 10 shows the basic application of the TPS370x. Only three pins are needed to supervise the supply voltage: V_{DD} and GND to supply the circuit and monitor the voltage, and RESET to assert a reset pulse if the conditions are fulfilled. If the supply voltage falls below the negative-going threshold voltage, V_{IT-} (at the TPS370x-50 this is typically 4.55 V), the $\overline{RESET}$ goes low and the DSP is reset. The reset returns to high about 200 ms after the supply voltage rises above V_{IT+} (at the TPS370x-50 this is about 4.62 V).

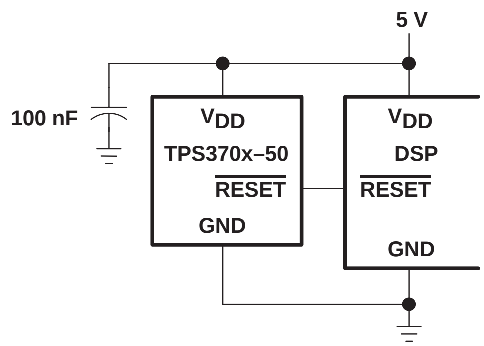

Figure 10. Basic Application Using a SVS to Reset a DSP

3.6 Application Example for the High-Active Reset (TPS3707-xx only)

In most cases, the low-active reset is needed to reset a microcomputer or DSP. An exception is the popular microcontroller family 80C51 as shown in Figure 11.

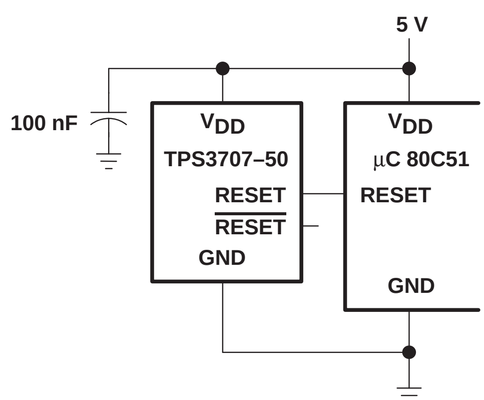

Figure 11. Resetting the 80C51 Controller using the High-Active Reset

4 Power-Fail Comparator

The following pinouts refer to the SO package:

Pin 4: PFI	Power-fail input
Pin 5: $\overline{\text{PFO}}$	Power-fail output – low-active

4.1 Functional Description

An additional comparator monitors voltages other than the nominal voltage. The power-fail input is compared with an internal voltage reference of 1.25 V. If the input voltage falls below 1.25 V, the power-fail output goes low; if it goes above 1.25 V plus approximately 0.01-V hysteresis, the output returns to high. Adding two external resistors allows the TPS370x to supervise any voltage above 1.25 V; the sum of both resistors should be about 1 MΩ to minimize power consumption and to ensure that the current in the PFI pin can be neglected compared with the current through the resistor network. The tolerance of the resistors should not exceed 1% to ensure that the sensed voltage does not vary too much.

Figure 12 shows the resistor network, and Table 6 lists resistor pairs that can be used for supervising voltages other than the nominal voltage. R2 is connected to the PFI and ground pin, R1 is connected with PFI and the supervised voltage. If the monitored voltage falls below the trip point, $\overline{\text{PFO}}$ is asserted.

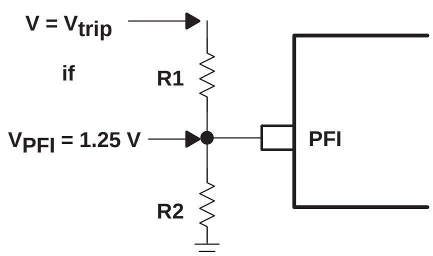

Figure 12. External Resistor Network

Table 6. Look-Up Table for Different Trip Points, Using E24 Resistors

R1/kΩ	R2/kΩ	V_{trip}/V	R1/kΩ	R2/kΩ	V_{trip}/V	R1/kΩ	R2/kΩ	V_{trip}/V
100	910	1.4	620	360	3.4	820	150	8.1
180	820	1.5	680	360	3.6	750	130	8.5
330	750	1.8	620	300	3.8	910	150	8.8
360	750	1.9	680	300	4.1	820	130	9.1
390	680	2.0	680	270	4.4	820	120	9.8
470	680	2.1	750	270	4.7	910	130	10.0
470	620	2.2	820	270	5.0	820	110	10.6
470	560	2.3	750	240	5.2	910	120	10.7
510	560	2.4	750	220	5.5	820	100	11.5
560	560	2.5	750	200	5.9	910	110	11.6
560	510	2.6	750	180	6.5	1000	120	11.7
560	470	2.7	820	180	6.9	820	91	12.5
620	470	2.9	750	150	7.5	910	100	12.6
680	470	3.1	910	180	7.6	1000	100	13.8
560	360	3.2	820	160	7.7	1100	100	15.0

4.2 Hysteresis of PFI

To ensure better noise immunity and to avoid oscillations at $\overline{\text{PFO}}$, hysteresis is used at PFI. As Figure 13 shows, all TPS370x devices have a hysteresis value of about 10 mV.

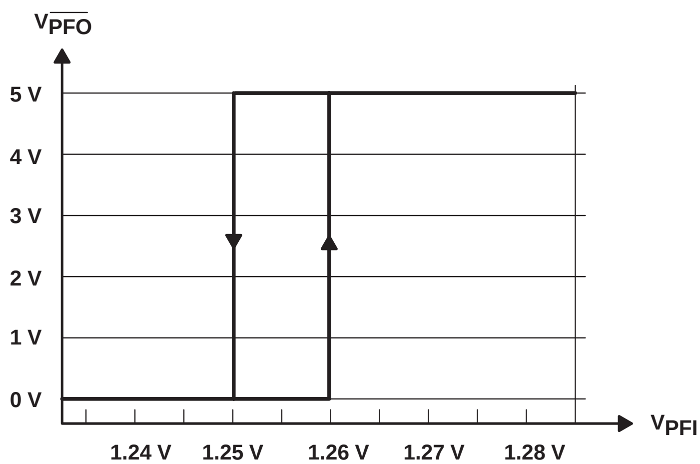

Figure 13. Hysteresis of Power-Fail Input

4.3 An Early Warning System of Power-Fail

Figure 14 shows an early warning system for power-fail. If the nominal voltage is 5 V, the threshold voltage is 4.55 V. For early recognition of supply voltage reduction, the supervising voltage could be adjusted to a threshold voltage of 4.7 V. If the $\overline{\text{PFO}}$ pin is connected to an interrupt input of a processor, data can be saved in time.

The formula to calculate the trip point voltage of PFI, which depends on R1 and R2 is:

$$V_{trip} \approx 1.25\ V \times \frac{R1 + R2}{R2}$$

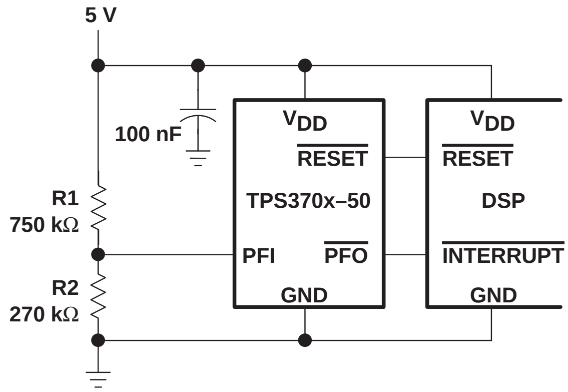

Figure 14. Sensing a Voltage of 4.7 V with the Power-Fail Function

The adjusted trip point at PFI is:

$$V_{trip} \approx 1.25\ V \times \frac{750\ k\Omega + 270\ k\Omega}{270\ k\Omega} \approx 4.7\ V$$

4.4 Under-Voltage and Over-Voltage Protection Example

With one inverter and two resistors, undervoltage and overvoltage protection can be realized. In Figure 15, the DSP is reset if the supply voltage decreases below 4.55 V or increases above 5.5 V. $\overline{\text{PFO}}$ is connected with an inverter to the $\overline{\text{MR}}$ pin because a reset should be asserted if the PFI trip point is increased and not if it is decreased. In other words, the PFI function is not normally used as an undervoltage protection, but as an overvoltage protection.

To calculate the trip point voltage for generating a reset because of overvoltage conditions:

$$V_1 \approx 1.26\ V \times \frac{R1 + R2}{R2}$$

The 1.26 V results from adding 10-mV hysteresis to the trip point voltage of PFI.

To calculate the trip point voltage where the low-active reset returns to high after delay time:

$$V_2 \approx 1.25\ V \times \frac{R1 + R2}{R2}$$

Because of tolerances of the resistors and the SVS, the formula delivers only an approximation. Resistors with the smallest possible tolerance should be used.

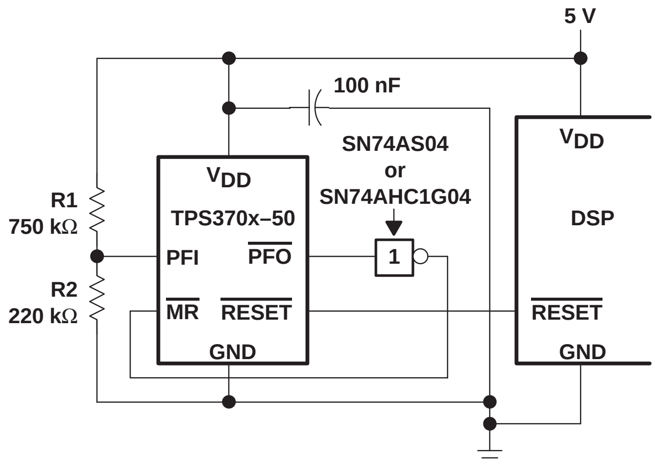

Figure 15. Under-Voltage and Over-Voltage Protection

To calculate the voltage for triggering a reset because of overvoltage conditions in the example:

$$V_1 \approx 1.26\ V \times \frac{750\ k\Omega + 220\ k\Omega}{220\ k\Omega} \approx 5.56\ V$$

To calculate the voltage, where the low-active reset returns to high after delay time in the example:

$$V_2 \approx 1.25\ V \times \frac{750\ k\Omega + 220\ k\Omega}{220\ k\Omega} \approx 5.51\ V$$

Table 7 shows the measurement results as the supply voltage increases from 5.50 V to 5.65 V and decreases to 5.50 V again.

Table 7. Measurement Results

Supply Voltage (V)	$\overline{\text{PFO}}$	$\overline{\text{MR}}$	$\overline{\text{RESET}}$
5.50	Low	High	High
5.59	Goes high	Goes low	Goes low
5.65	High	Low	Low
5.54	Goes Low	Goes high	Goes high
5.50	Low	High	High

Measurements have shown, that the capacitor between V_{DD} and ground is very important for proper operation. Measurements without the capacitor showed oscillations in the feedback loop and sometimes malfunctions occurred.

4.5 Signal Amplifier and Converter Example

Figure 16 shows another option to use the TPS370x as a signal converter and amplifier. The working point at PFI, adjusted by the two resistors, has to be near the trip point voltage of 1.25 V. Capacitor C1 couples in a small-amplitude signal. When the resulting signal at PFI increases above 1.26 V, $\overline{\text{PFO}}$ goes high and returns to low if the voltage decreases below 1.25 V.

Figure 17 and Figure18 show how to transform 0.1-V sine and triangular signals into 5-V rectanglular signals.

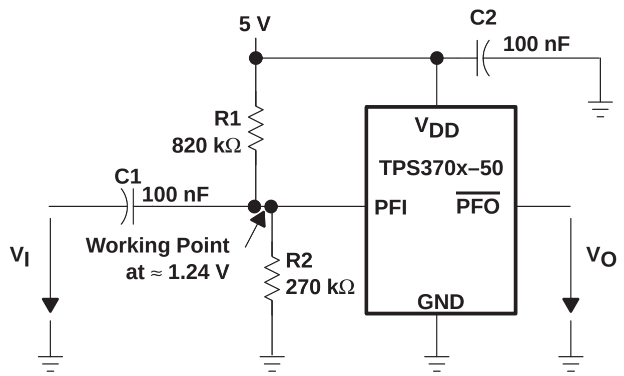

Figure 16. A Signal Amplifier and Transformer

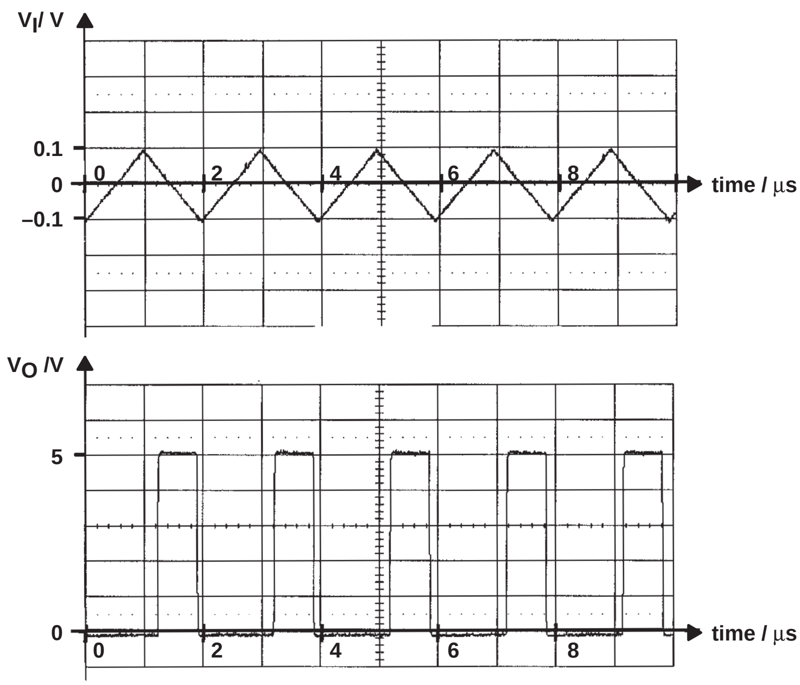

Figure 17. Transforming a 0.1-V Triangular Signal into a 5-V Rectangular Signal

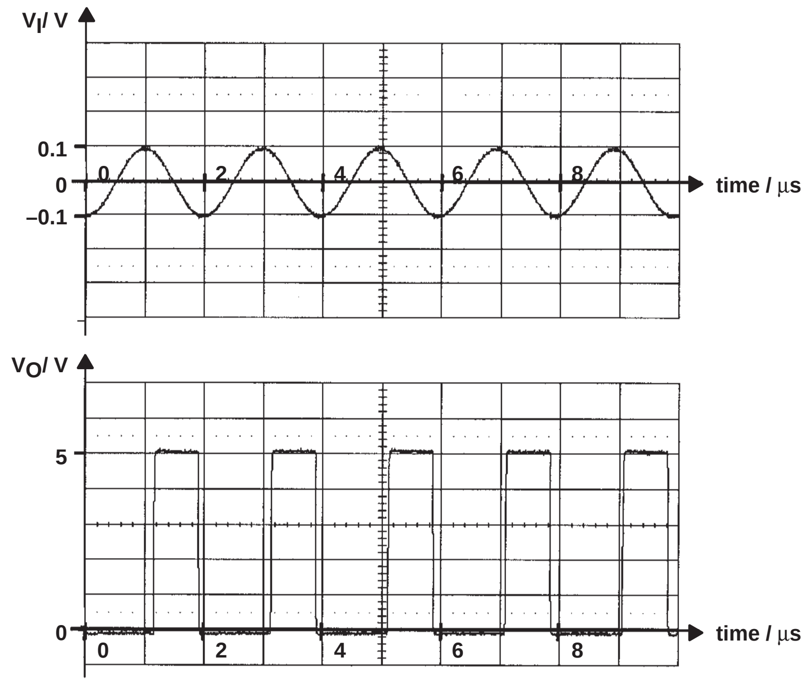

Figure 18. Transforming a 0.1-V Sine Signal into a 5-V Rectangular Signal

4.6 Supervising the Standard Industry Voltage of ±15 V

With five resistors, a voltage reference, and two TPS370x-50s, the popular industry voltages of ±15 V can be supervised. As shown in Figure 19, both $\overline{\text{PFO}}$ pins are connected to I/O-ports of the microcontroller to signal the status of the voltages.

If the 15-V line has more than about 14 V, the $\overline{\text{PFO}}$ of SVS1 is high; otherwise it is low. SVS2 operates oppositely. If the –15-V line has a voltage value in the recommended range (<–14 V), $\overline{\text{PFO}}$ is low, otherwise it is high. The signal logic can be adjusted by connecting $\overline{\text{PFO}}$ to the $\overline{\text{MR}}$ input of SVS2 and by connecting RESET (TPS3707 only) to the I/O-port of the microcontroller. In both cases a high level means correct voltages and a low level means incorrect voltages.

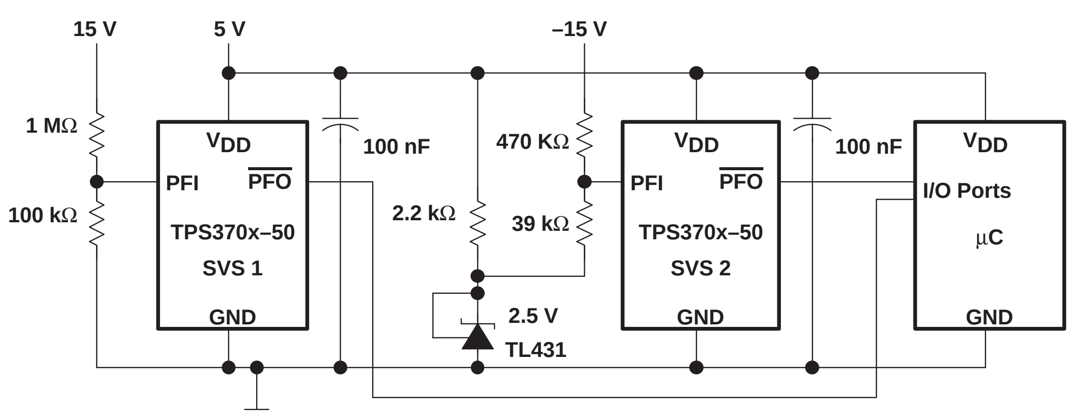

Figure 19. Application Example of Sensing ±15 V Supply Voltage

Measurement values:

SVS1: $\overline{\text{PFO}}$ goes low, if 13.98 V is decreased and returns to high, if 14.07 V is increased.

SVS2: $\overline{\text{PFO}}$ goes high, if –13.80 V is increased and returns to low, if –13.94 V is decreased.

Both supervising circuits work independently of each other. This means that if one voltage fails, the other can continue to operate. The assumption for proper operation of both circuits is that the 5-V supply line of the SVS units is within the recommended range.

5 Manual Reset

The following pinout refers to the SO package:

Pin 1: $\overline{\text{MR}}$	Manual reset input
Pin 7: $\overline{\text{RESET}}$	Reset output – low-active
Pin 8: RESET	Reset output – high-active (only TPS3707)

5.1 Function Description

The manual reset function allows reset of the system by a pushbutton or by a logic circuit output. Because of an internal pull-up resistor, no external component is required. The $\overline{\text{MR}}$-input can be left open or configured as a 3-state input without influencing the normal functionality. Figure 20 shows a typical manual reset arrangement.

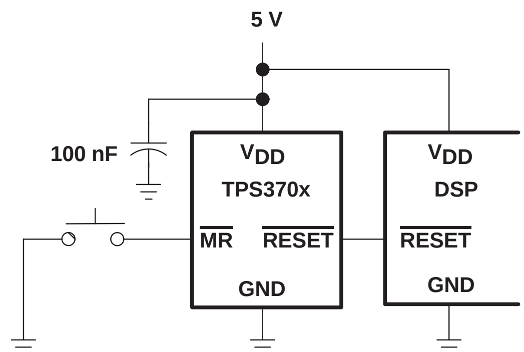

Figure 20. Manual Resetting of the DSP with a TPS370x

5.2 Sensing Two Voltages with One RESET-Output

Many electronic systems use more than one supply voltage. To control two voltages with the TPS370x-xx, refer to Figure 21 and choose the TPS370x device for one of the voltages to be supervised. For the other voltage, use the PFI terminal, which is adjustable by a resistor divider. Because there is only one reset pin for the voltage supervised by the V_{DD} pin, connect the $\overline{\text{PFO}}$ with the $\overline{\text{MR}}$ input. In this way, a reset is triggered, if either the voltage at V_{DD} or the voltage sensed by PFI decreases under the critical value.

$$V_{trip} \approx 1.25\ V \times \frac{910\ k\Omega + 120\ k\Omega}{120\ k\Omega} \approx 10.7\ V$$

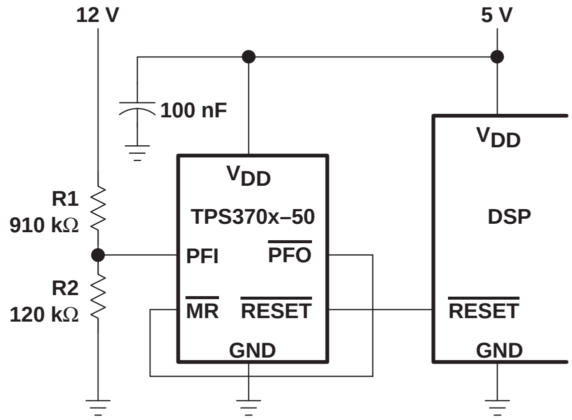

Figure 21. Sensing 12 V and 5 V Supply Voltages

5.3 Supervising Three Voltages

To supervise three voltages, two SVSs and two resistors are needed. Figure 22 shows that the devices are connected by the low-active reset output of the first SVS and the $\overline{MR}$ input of the second SVS. The assumption is that two voltages are nominal voltages of the TPS370x SVS family. The available nominal voltages are 5 V, 3.3 V, 3 V, and 2.5 V.

A trip point voltage example at the first device:

$$V_{trip} \approx 1.25\ V \times \frac{470\ k\Omega + 330\ k\Omega}{330\ k\Omega} \approx 3.03\ V$$

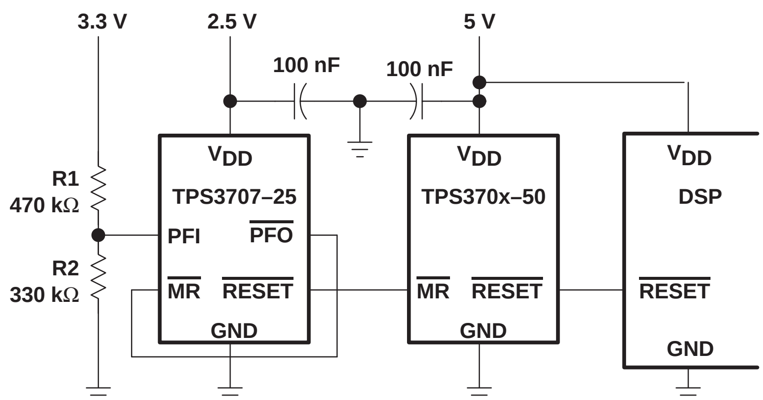

Figure 22. Supervising the Three Voltages 2.5 V, 3.3 V, and 5 V

5.4 Sensing a Positive and a Negative Voltage

Sensing a positive and a negative voltage requires two SVSs, two resistors, and one transistor, as shown in Figure 23. The output level of the SVS2 reset is adjusted to the input level of the SVS1 $\overline{\text{MR}}$ input by a transistor switch. If the transistor is switched off (reset output of SVS2 has a low signal), $\overline{\text{MR}}$ is pulled to 5 V through the internal 14-kΩ resistor. If it conducts (reset output of SVS2 has a high signal), the resistive divider consisting of the internal 14-kΩ resistor and the external 15-kΩ resistor between ±5 V make the low level at the $\overline{\text{MR}}$ input generate a reset.

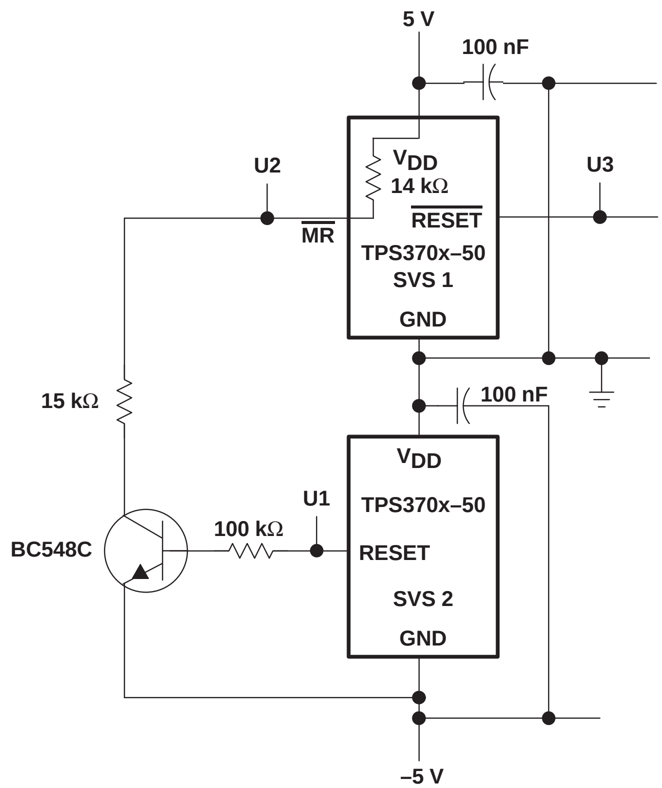

Figure 23. Supervising ±5 V with Two TPS370x-50

Measurement results:

The reset output of SVS1 is connected through a 1-MΩ resistor and a parallel 47-pF capacitor to ground (to simulate an electrical CMOS load). Figure 24 shows what happens if the negative voltage increases from –5 V to 0 V at a voltage level of –4.52 V.

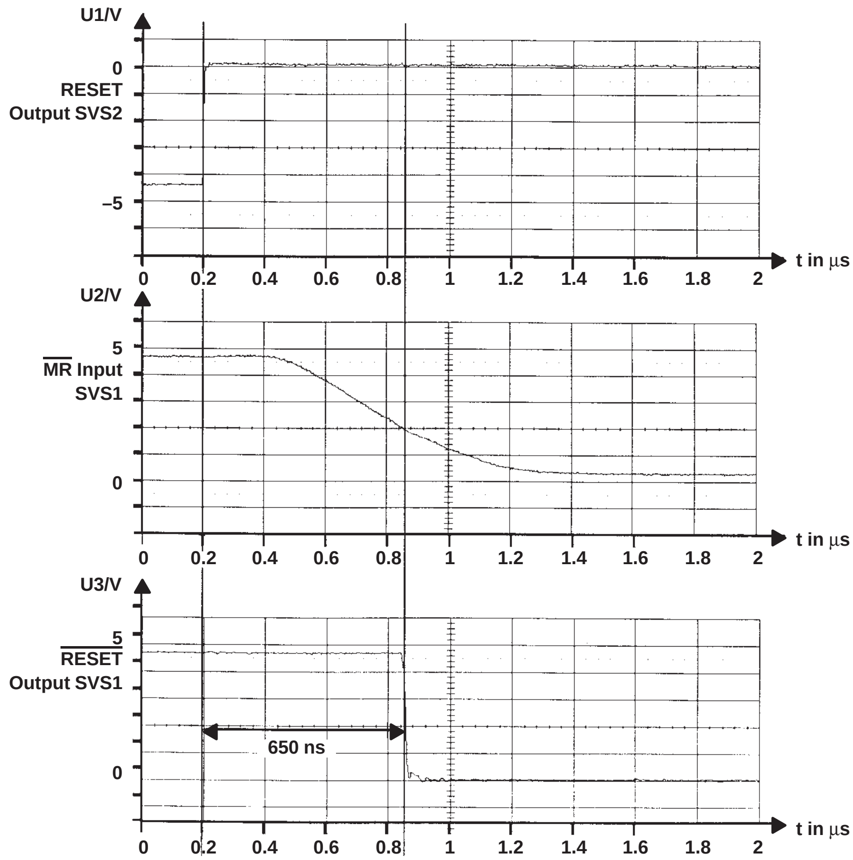

Figure 24. Timing Diagram for Sensing a Positive and a Negative Voltage

The reset output of SVS1 is correctly asserted with a low level from –4.52 V up to –0.62 V.

6 Watchdog (TPS3705 Only)

The following pinouts refer to the SO package.

Pin 6: WDI — Watchdog input

Pin 8: $\overline{WDO}$ — Watchdog output – low-active

6.1 Functional Description

In a microprocessor-based or DSP-based system, it is not only important to supervise the supply voltage, it is also important to ensure correct program execution. The task of a watchdog is to ensure that the program is not stalled in an indefinite loop. The microprocessor, the microcontroller, or the DSP typically have to toggle the watchdog input within 1.6 seconds to avoid a timeout occurring and the watchdog output ($\overline{WDO}$) going low. Either a low-to-high or a high-to-low transition resets the internal watchdog timer. If the input is unconnected or tied with a high impedance (e.g., a 3-state driver), the watchdog resets itself.

6.2 Timing Considerations

In Figure 25, the minimum, typical, and maximum values of timeout over the temperature range are shown. The time starts at the last transition of WDI.

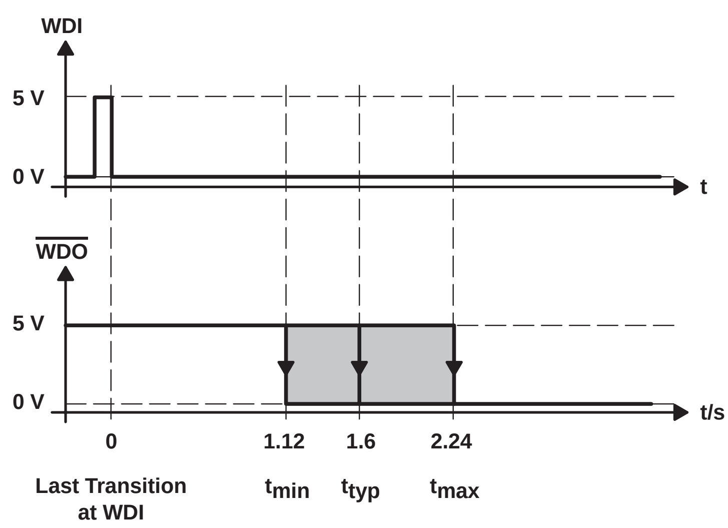

Figure 25. Timeout of the Watchdog Timer

6.3 The Watchdog Function in a μP-Application

In some applications $\overline{WDO}$ is connected to a non-maskable interrupt input of a processor or controller to generate an interrupt if timeout occurs. See Figure 26. The triggered interrupt service routine subsequently can remove the problem by software. In this way an indefinite loop does not mean loss of data. Figure 27 shows the measured results of this application.

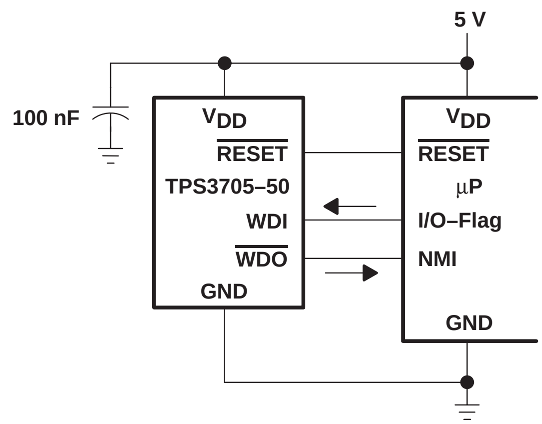

Figure 26. Application Example of Using the Watchdog with a Microprocessor

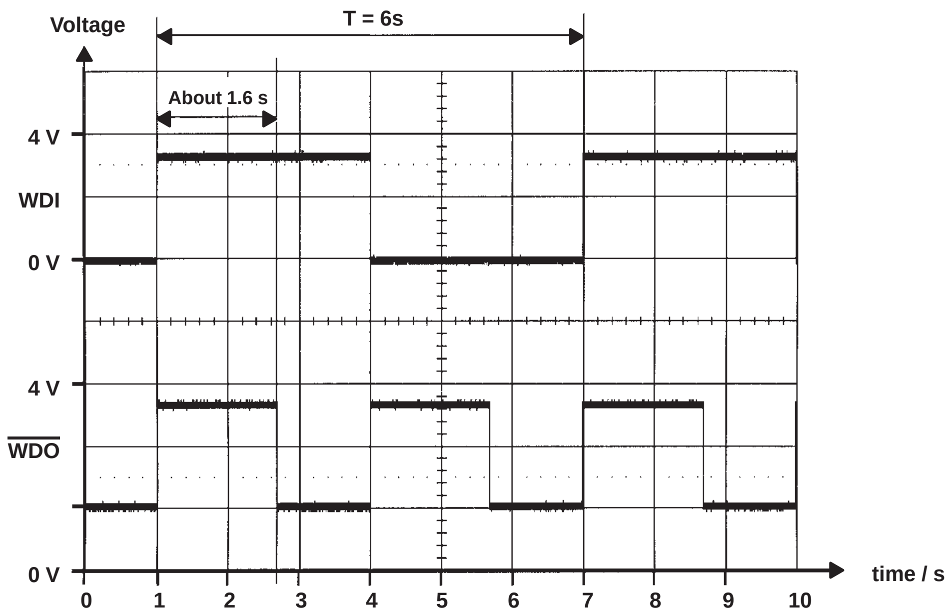

Figure 27. Measurement Results

The measurement shows that about 1.6 seconds after the last transition at WDI, the watchdog output $\overline{WDO}$ becomes active. $\overline{WDO}$ stays low until WDI sees another transition.

6.4 The Watchdog Function in a DSP-Application

In some applications, it is not possible to restore normal program execution with an interrupt. In this case, as shown in Figure 28, a reset must be generated. For this reason $\overline{WDO}$ and $\overline{MR}$ should be tied together.

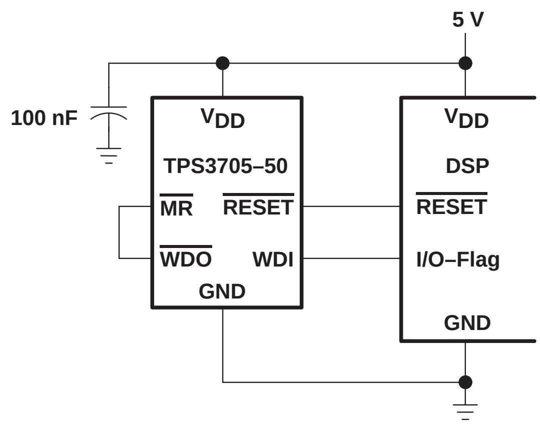

Figure 28. Application Example of Using the Watchdog with a DSP

The measurements in Figure 29 show that the $\overline{\text{WDO}}$ goes low only for some nanoseconds, if it is connected to $\overline{\text{MR}}$. The reason for this behavior is that some nanoseconds after $\overline{\text{RESET}}$ is asserted, the output-latch of $\overline{\text{WDO}}$ will be set again. $\overline{\text{WDO}}$ thus returns to a high level. If the $\overline{\text{RESET}}$ becomes inactive again after about 200 ms, the internal timeout counter is reset and starts counting again.

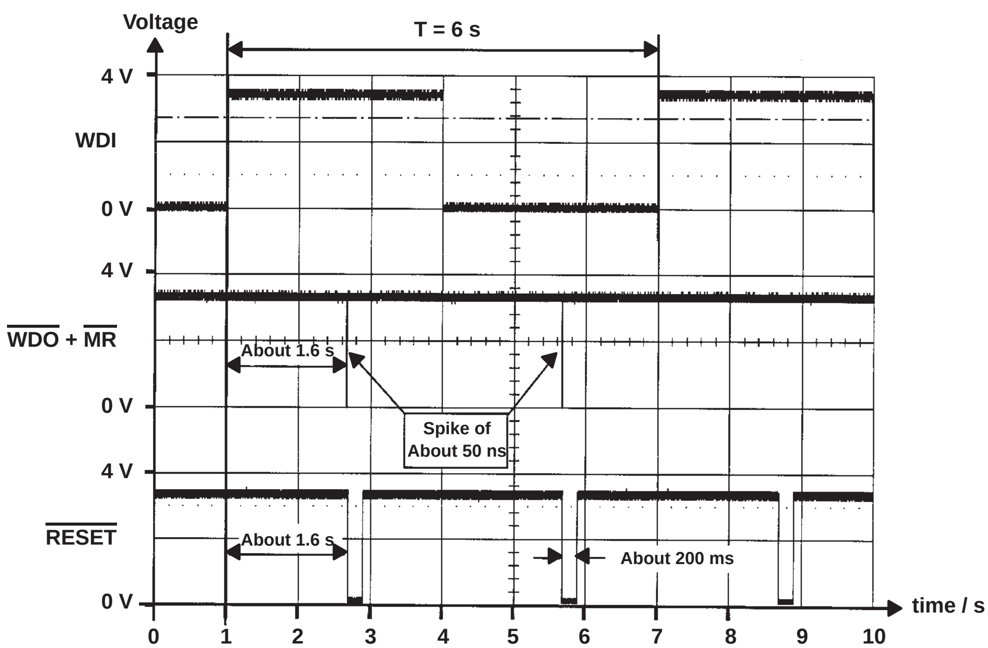

Figure 29. Measurement Results for Watchdog With DSP

7 Application Hints and Layout

This section discusses layout considerations.

7.1 Layout Considerations

Refer to Figure 30. The following three points should be considered in the layout to ensure proper operation:

- Connections to external components should be kept as short as possible.
- The supply voltage supervisor should be situated in an interference-free environment on the edge of the circuit.
- A 100-nF blocking capacitor between supply voltage and ground is needed to avoid disturbances on the supply line.

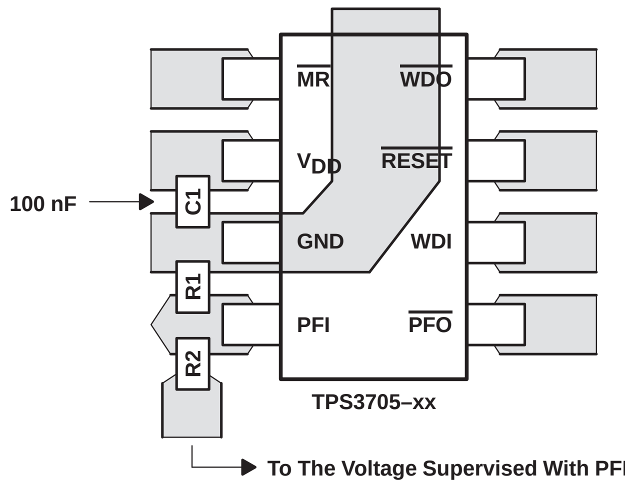

Figure 30. Suggested Layout for a Circuit with the TPS3705-xx in SOP

7.2 The Capacitor Between V_{DD} and GND

Figure 31 shows the behavior of V_{DD} and $\overline{RESET}$ at the moment of pushing a button to connect the $\overline{MR}$ input to ground with a 100-nF capacitor between V_{DD} and ground.

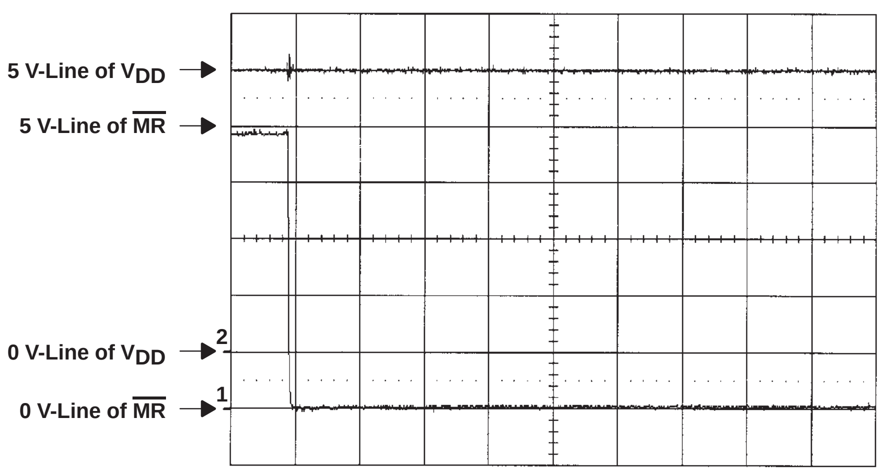

Figure 31. V_{DD}–Line with a Capacitor at the Moment of Switching Output

Figure 32 shows the behavior of V_{DD} and $\overline{\text{RESET}}$ at the moment of connecting the $\overline{\text{MR}}$ input to ground without a capacitor between V_{DD} and ground.

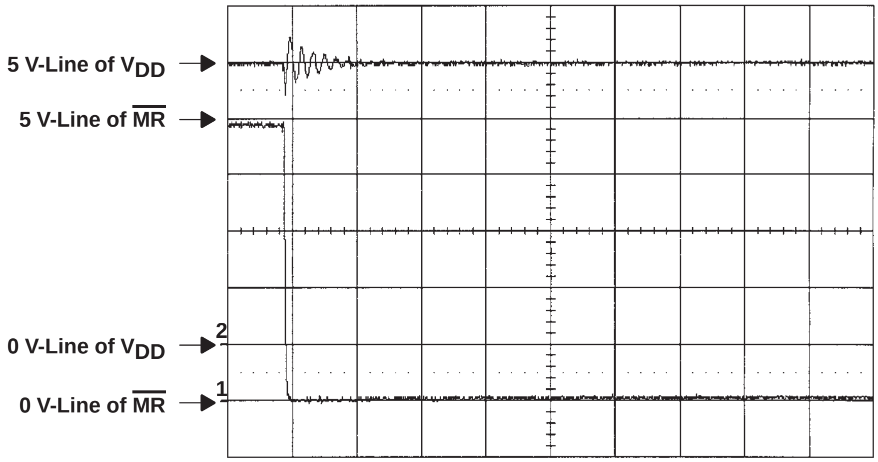

Figure 32. V_{DD}–Line without a Capacitor at the Moment of Switching Output

Comparing the two diagrams, it can be seen that the V_{DD}-line shows dangerous oscillations without the 100-nF capacitor if the outputs are switching. The oscillations have an amplitude of more than 0.5 V, lowering the threshold voltage of 4.55 V. An unwanted reset could be triggered if, for example, $\overline{\text{PFO}}$ goes low because of decreasing 1.25 V at PFI.

This behavior is caused by a current peak at the moment of switching outputs. Both transistors of the totem pole output stage (see Figure 33) are conducting momentarily, so that a current of up to 10 mA can flow between V_{DD} and ground. Because of this, the supply voltage starts to oscillate a certain time.

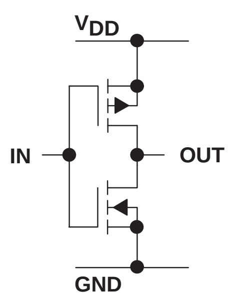

Figure 33. Totem Pole Output Stage

8 Summary

The Texas Instruments TPS370x family of devices supervises 5.0 V, 3.3 V, 3.0 V and 2.5 V. If the voltage falls below a specified value, a reset will be asserted. A second voltage can be supervised at PFI. This voltage can be customized with two resistors. This feature offers increased security for microcontroller- or DSP-based systems. Another possibility to trigger a reset is a low pulse at manual reset input $\overline{MR}$. External ICs or a pushbutton can be connected with this input. The TPS 3705 family includes a watchdog function for more reliable program execution. The TPS3707 family integrates a high-active reset output to support different kinds of processors or controllers like the popular 8051 family.

9 References

1. *Designer's Guide and Data Book* – InfoNavigator CD-ROM, SLYC005A
2. Data sheet of TPS370x
3. *TLC77xx Series of BiCMOS Supply Voltage Supervisors*, SLVAE03
4. *Supply Voltage Supervisor TL77xx Series*, SLVAE04
5. *TPS382x Microprocessor Supervisory Circuits with Watchdog Function*, SLVA039
6. *Power Supply Circuits Data Book*, SLVD002
7. *Linear Design Seminar*, SLYDE05
8. Internet: http://www.ti.com/sc/docs/psheets/pids1.htm

Please select MICROPROCESSOR SUPERVISORY CIRCUITS