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Powering OMAP™3 With TPS6235x: Design-In Guide

Andy Dykstra and James Doublesin — *PMP - Catalog Power Mgmt Units*

ABSTRACT

This document details the design considerations of a power management unit solution for the OMAP™3 processor using the TPS6235x device.

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1 Introduction

The OMAP35xx Applications Processors have a diverse set of power management features which potentially enable lower cost power solutions based on your application. This design-in guide describes a power solution based on the TPS6235x device. This guide can be used to evaluate this solution for your design, or help you make decisions when designing in this solution.

2 Power Requirements and Features of OMAP35xx

Because of the maximum supply current of 800 mA on the TPS6235x devices, a TPS6235x-based power solution is only applicable for OMAP3503- and OMAP3515-based designs. The following section describes the specifications and power management features of these devices.

2.1 Power Specifications

The following tables detail the power requirements for each OMAP35xx device that is supported by a TPS6235x-based power solution. Note that the only difference in power lies in the amount of current required by the VDD_CORE voltage rail. Otherwise, the specifications are identical.

Table 1. OMAP3503 Power Specifications

	POWER RAIL	VOLTAGE	TOLERANCE	Imax (mA)	SEQUENCING ORDER
Core	VDD_MPU	0.95 V, 1 V, 1.2 V, 1.27 V, 1.35 V (1)	±5%	680	4
Core	VDD_CORE	0.95 V, 1 V, 1.15 V (1)	±5%	320	3
I/O	VDDS, VDDS_WKUP_BG, VDDS_MEM, VDDS_SRAM	1.8 V	±5%	147	1
I/O	VDDS_DPLL_PER, VDDS_DPLL_DLL	1.8 V	±5%	40	2
I/O	VDDA_DAC	1.8 V	±5%	65	After reset
I/O	VDDS_MMC1, VDDS_MMC1A	1.8 V	±5%	22	After reset(see MMC Boot for more information)
		3 V	±10%		
The preceding power values assume that SmartReflex™ AVS is implemented.					

(1) See the latest OMAP35xx Operating Condition Addendum for the most current voltage values.

Table 2. OMAP3515 Power Specifications

	POWER RAIL	VOLTAGE	TOLERANCE	Imax (mA)	SEQUENCING ORDER
Core	VDD_MPU	0.95 V, 1 V, 1.2 V, 1.27 V, 1.35 V (1)	±5%	680	4
Core	VDD_CORE	0.95 V, 1 V, 1.15 V (1)	±5%	430	3
I/O	VDDS, VDDS_WKUP_BG, VDDS_MEM, VDDS_SRAM	1.8 V	±5%	147	1
I/O	VDDS_DPLL_PER, VDDS_DPLL_DLL	1.8 V	±5%	40	2
I/O	VDDA_DAC	1.8 V	±5%	65	After reset
I/O	VDDS_MMC1, VDDS_MMC1A	1.8 V	±5%	22	After reset(see MMC Boot for more information)
		3 V	±10%		
The preceding power values assume that SmartReflex™ AVS is implemented.					

(1) See the latest OMAP35xx Operating Condition Addendum for the most current voltage values.

2.2 Power-Up Sequencing

Figure 1 shows the power-up sequencing requirements of OMAP35xx. The description of the power-up sequence follows.

1. VDDS_WKUP_BG, VDDS_MEM, VDDS, and VDDS_SRAM are all 1.8-V rails and are tied to the same power supply. These are ramped first, ensuring a valid level on the I/O domain. In the example block diagram (Figure 3), these rails are powered by the TPS77418 LDO.
2. During the entire power-up sequence, the power-on-reset signal SYS_NRESPWRON must be held low until all rails and clocks are stable. This is accomplished using the TPS3808G18 supervisor circuit. See SYS_nRESPWRON Timing for more information.
3. Both the 32-kHz and the high-frequency clock need to start oscillating and be stable.
4. After 1.8 V is stabilized, VDD_CORE can start ramping.
5. After VDD_CORE is stabilized, VDD_MPU can start ramping.
6. After 1.8 V is stabilized, VDDS_DPLL_DLL and VDDS_DPLL_PER (rails are tied to the same power supply) can ramp during or after VDD_CORE and VDD_MPU ramp.
7. Once all of the preceding power rails have stabilized, and the 32-kHz and the high-frequency clock have stabilized, then SYS_NRESPWRON can be released.
8. Other power supplies, such as VDDS_MMC1, VDDS_MMC1A, VDDS_DAC, etc., can be turned on or off depending on the application.

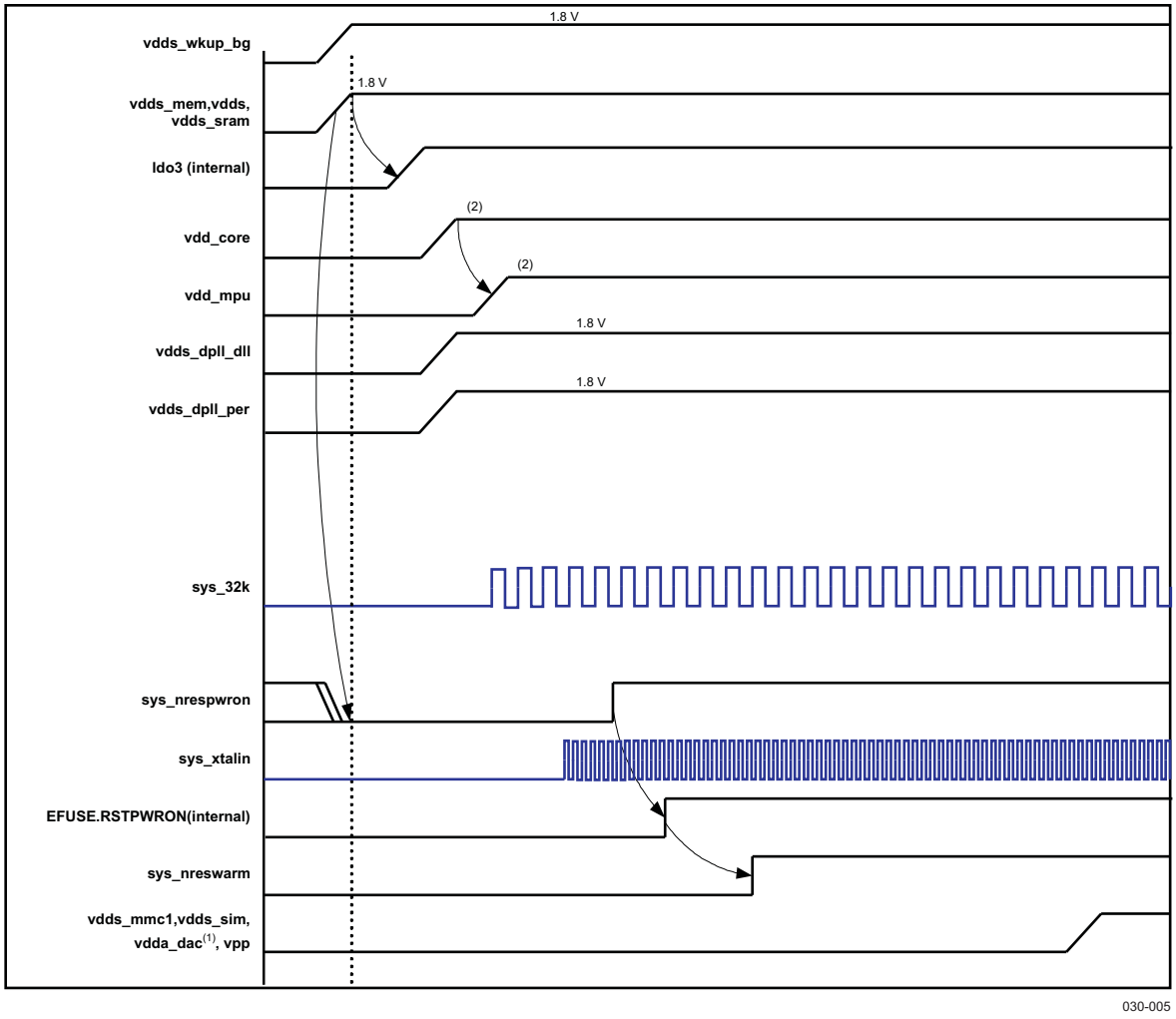


Figure 1. OMAP35x Power-Up Sequencing Requirements

2.3 Power-Down Sequencing

When using the TPS6235x power solution, power down is achieved by removing the input voltage from each of the power integrated circuits (IC). When this occurs, all voltages ramp down at the same time, and the ramp rate of each voltage is generally determined by the load on that voltage.

During power down, all signals driving OMAP™3 must have a voltage level equal to or less than the I/O voltage of OMAP™3 to avoid driving pins that are unpowered. For example, the schematic example of Figure 2 shows that the 32-kHz clock gated by a 1.8-V Power Good signal. This ensures that this clock circuit does not drive the OMAP™3 input clock pins when the 1.8 V is removed from OMAP™3.

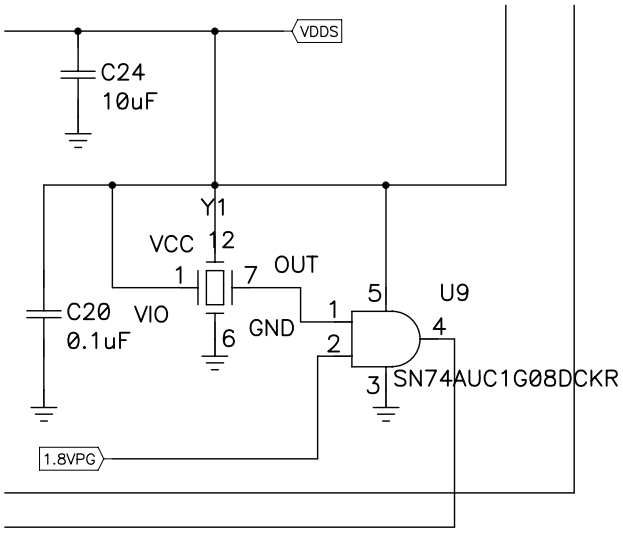


Figure 2. 32-kHz Clock Circuitry

2.4 OMAP35xx Power Management Features

The OMAP35xx Applications Processors have a rich set of features that make aggressive power optimizations feasible in a user application. These features include DVFS (dynamic voltage frequency scaling) and SmartReflex™ AVS (adaptive voltage scaling). Both of these features allow for the lowest power operation depending on the OMAP35xx processing requirements. In short, DVFS allows the user to change between the OMAP35xx's operating points (voltages) depending on the device's operating frequency. Depending on your application, you may want to be able to move among these voltage levels during operation to reduce power consumption. SmartReflex™ AVS optimizes each of these operating points based on wafer process differences, temperature, and silicon degradation.

2.4.1 Dynamic Voltage and Frequency Scaling

DVFS is a power management technique used while active processing is going on in the system-on-chip (SoC). The technique matches the operating frequency of the hardware to the performance requirement of the active application scenario. Whenever clock frequencies are lowered, operating voltages can be lowered as well to achieve power savings. OMAP35xx supports this technique on VDD_MPU and VDD_CORE power rails by defining discrete voltage values for these power rails and the accompanying maximum clock frequencies allowed for the modules supplied by those power rails. Each operating voltage and accompanying maximum clock frequency specification is called an operating performance point (OPP). The following tables show the OPP definitions for VDD_MPU and VDD_CORE.

Table 3. VDD_MPU Operating Points

PROCESSOR OPP	VDD_MPU	ARM Max MHz
5	1.35	600
4	1.27	550
3	1.20	500
2	1	250
1	0.95	125

Table 4. VDD_CORE Operating Points

INTERCONNECT/ PERIPHERALS OPP	VDD_CORE	L3 Max MHz
3	1.15	166
2	1	100
1	0.95	41.5
See the latest OMAP™3 Operating Condition Addendum for the most current voltage values.		

A TPS6235x power solution supports DVFS for OMAP35xx by meeting the requirements shown in the Table 5.

Table 5. TPS6235x Power Solution Support for DVFS

Power IC Requirement for DVFS	Does TPS6235x based power solution implement the requirement?	How TPS6235x power module for the OMAP3EVM implements this DVFS requirement
Support all five DVFS voltage values (0.95 V, 1 V, 1.2 V, 1.27 V, and 1.35 V) defined for VDD_MPU	**Yes.** The TPS62353 supports full voltage range and can adjust in 12.5-mV increments.	Uses TPS62353 to power VDD_MPU rail
Support all three DVFS voltage values (0.95 V, 1 V, and 1.15 V) defined for VDD_CORE	**Yes.** The TPS62352 supports full voltage range and can adjust in 12.5-mV increments.	TPS62352 used to power VDD_CORE rail
I2C™ interface for setting output voltage to any of the values defined for DVFS	**Yes.** TPS6235x supports high-speed I2C bus available for controlling voltage output.	I2C buses of TPS62352 and TPS62353 connected to OMAP35xx I2C bus

2.4.2 SmartReflex™ Adaptive Voltage Scaling

AVS is a power management technique that can be used to refine system power consumption at a given OPP. The DVFS technique defines safe voltages for the OPPs so that all manufactured devices can meet the maximum frequency specifications for the OPPs. However, the silicon manufacturing process yields a distribution of devices, some (called strong or hot devices) of which can meet the frequency specifications at lower operating voltages than the conservative values defined by DVFS. SmartReflex™ AVS has been implemented by Texas Instruments to continuously adapt the operating voltage to the process properties of individual devices in order to maximize power savings for active scenarios. The OMAP35xx integrates specialized hardware to enable SmartReflex™ AVS on VDD_MPU and VDD_CORE. The special hardware can be used to implement Class-2 or Class-3 SmartReflex™.

- **Class-2 SmartReflex™:** The special hardware monitors real-time performance; small software loop runs on ARM processor to change voltage whenever necessary.
- **Class-3 SmartReflex™:** The special hardware has a dedicated hardware loop to dynamically monitor performance and adjust voltage without ARM processor intervention.

Equivalent power savings can be achieved with either implementation.

A TPS6235x power solution supports SmartReflex™ for OMAP35xx by meeting the requirements shown in Table 6. See Enabling Class 2 SmartReflex for more implementation details.

Table 6. TPS6235x Power Solution Support for SmartReflex™

Power IC Requirement for SmartReflex™	Does TPS6235x-based power solution implement the requirement?	How TPS6235x power module for the OMAP3EVM enables SmartReflex™
High-speed (or full-speed) I2C bus for setting output voltage	**Yes.** HS I2C bus available.	I2C connections present between power ICs and OMAP35xx I2C bus
Voltage programmability in steps over the range 0.8 V to 1.35 V	**Yes.** Can scale the output voltage between 0.75 V to 1.5375 V with voltage steps down to 12.5 mV on both VDD_MPU and VDD_CORE	Makes use of this property of TPS62353 and TPS62352 used to power VDD_MPU and VDD_CORE rails
(For Class-3 ™) Ability to affect voltage change with a single I2C register write	**Yes.** Requires just one register write using VSEL1 register	Connects TPS6235x I2C bus with OMAP™3 I2C4 bus which is directly used by SmartReflex™ hardware.
(For Class-2 SmartReflex™) Ability to affect voltage change with a sequence of one or more I2C register writes	**Yes.** Requires just one register write using VSEL1 register	Power ICs' I2C buses connected to OMAP™3 general-purpose I2C2 bus
Slew rate between 4 mV/µs and 16 mV/µs	**Yes.** TPS6235x supports multiple slew rates, including 4.8 mV/us and 9.6 mV/us selectable in CONTROL2 register bits [2:0].	Makes use of this property of TPS62353 and TPS62352 used to power VDD_MPU and VDD_CORE rails, respectively

2.4.3 Static/Standby Leakage Management

Static/Standby Leakage Management (SLM) is the combination of techniques used to achieve lowest power consumption during system idle time, when a system-on-chip (SoC) performs no useful processing. The OMAP35xx supports various options for low-power standby states that trade-off level of power savings with speed of wakeup latency. The level of power savings during standby is determined by whether internal memories and logic are retained or powered down, whether clocks are on or off, and whether external voltage regulators are kept on or off.

Several SLM features are built into the OMAP35xx architecture to enable low-power standby modes. In addition, OMAP35xx supports features for achieving further standby power savings by putting system components external to the OMAP SoC into lower power states. Notable among these are control signals for gating external clock and power sources.

- SYS_CLKREQ is a signal used to gate the high-frequency clock when it is not needed. The OMAP35xx can be set up to automatically deassert the sys_clkreq in full-chip retention and/or off modes.
- SYS_OFF_MODE is a signal used to indicate to external voltage regulators when they can be shut down.

OMAP35xx supports a standby mode called off-mode, which is the lowest power state from which the device can wake up autonomously. In OMAP35xx off-mode, system state is saved in external memory that can be put into self-refresh mode, most of the SoC is off, but a small wakeup domain stays powered on and operational at 32 kHz to monitor for wakeup events. The sys_clkreq is used to sequence an external clock source, while the sys_off_mode signal is used to sequence power during transitions into and out of the off-mode. The ability to shut off most of the external voltage supplies in this off-mode saves additional power dissipation in the voltage regulators. Alternatively to using the sys_off_mode pin, OMAP35xx supports I2C commands for VDD_MPU and VDD_CORE sequencing during off-mode transitions.

A TPS6235x power solution supports OMAP35xx SLM by meeting the requirements shown in Table 7.

Table 7. TPS6235x Power Solution Support for SLM

Power IC Requirement for SLM	Does TPS6235x-based power solution implement the requirement?	How TPS6235x power module for the OMAP3EVM enables SLM
Ability to gate high-frequency clock source with I/O signal for standby power savings	**Yes.** Can be taken care of in hardware with SYS_CLKREQ. See High Frequency Clock Circuit	Not supported on power module
(For SLEEP mode) Ability to lower voltage on VDD_MPU_IVA power source to lowest OPP via I2C	**Yes.** Supports I2C register write to VSEL1 register	Use I2C writes to set TPS6235x to its lowest voltage level for VDD_MPU
(For SLEEP mode) Ability to lower voltage on VDD_CORE power source to lowest OPP via I2C	**Yes.** Supports I2C register write to VSEL1 register	Use I2C writes to set TPS6235x to its lowest voltage level for VDD_CORE
(For OFF mode) Ability to turn off/on VDD_MPU power source with SYS_OFF_MODE signal or a single register write to the power IC over I2C	**No.** Use I2C writes to set TPS62353 to lowest voltage setting for VDD_MPU (0.95V). Does not support completely shutting down TPS6235x	Use I2C writes to set TPS6235x to its lowest voltage level for VDD_MPU
(For OFF mode) Ability to turn off/on VDD_CORE power source with SYS_OFF_MODE signal or a single register write to the power IC over I2C	**No.** Use I2C writes to set TPS62352 to lowest voltage setting for VDD_CORE (0.95V). Does not support completely shutting down TPS6235x	Use I2C writes to set TPS6235x to its lowest voltage level for VDD_CORE

3 TPS6235x Design-In Considerations

Figure 3 is a block diagram of one example of a complete power solution using the TPS6235x devices to power OMAP™3. The rest of the section details each design consideration to tailor the power solution to your needs.

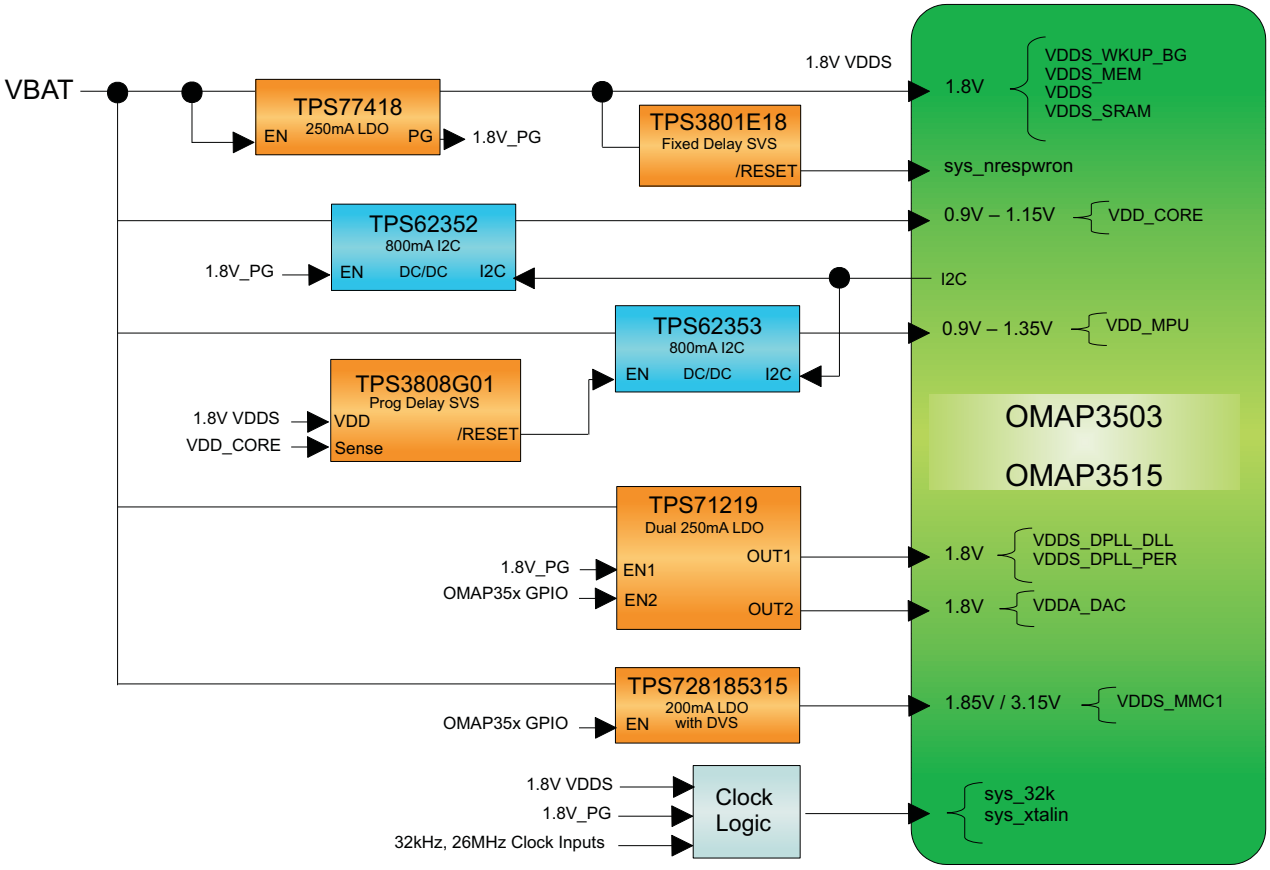


Figure 3. TPS6235x Power Solution Block Diagram

3.1 Reset

3.1.1 SYS_nRESPWRON Rise Time

The OMAP35xx data sheet states that the maximum rise/fall time for SYS_nRESPWRON is 10 ns (see the following highlighted sections extracted from data sheet tables)

BALL BOTTOM [1]	BALL TOP [2]	PIN NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULL U/D TYPE [12]	IO CELL [13]
AH25	NA	sys_nrespwron0	0	I	Z	I	NA	vdds	Yes	NA	NA	LVCMOS

PARAMETER			MIN	NOM	MAX	UNIT
STANDARD LVCMOS						
V_{IH}(6)	High-level input voltage		0.65 × vdds(5)		vdds ÷ 0.3	V
V_{IL}(6)	Low-level input voltage		–0.3		0.33 × vdds(5)	V
V_{HYS}	Hysteresis voltage at an input(1)			0.1		V
V_{OH}	High-level output voltage, driver enabled, pullup or pulldown disabled	$I_O = I_{OH}$ or I_O = –2 mA	vddsy(5) – 0.45			V
		$I_O = I_{OH} < \|–2\|$ mA	vddsy(5) – 0.40			
V_{OL}	Low-level output voltage with driver enabled, pullup or pulldown disabled	$I_O = I_{OL}$ or I_O = 2 mA			0.45	V
		$I_O = I_{OL}$ < 2 mA			0.40	
t_T	Input transition time (rise time, t_R or fall time, tF evaluated between 10% and 90% at PAD)		0		10(2)	ns
I_I	Input current with $V_I = V_I$ max		–1		1	µA
I_{OZ}	Off-state output current for output in high impedance with driver only, driver disabled		–20		20	µA

In order to meet this requirement, a push-pull output buffer is required, with rise/fall time of <10 ns.

Sometimes a push button reset is required to be shared with the SYS_nRESPWRON signal, thus implying an open-drain requirement. However, to meet the rise time requirement, such a solution consume\s too much power for certain power-sensitive applications.

If multiple reset sources are needed, you can use a TPS3808 as shown in Figure 4 (the TPS3808 has an open-drain output). Other reset sources can be combined with this, and then use an AND gate or other buffer to achieve the required rise time for SYS_nRESPWRON.

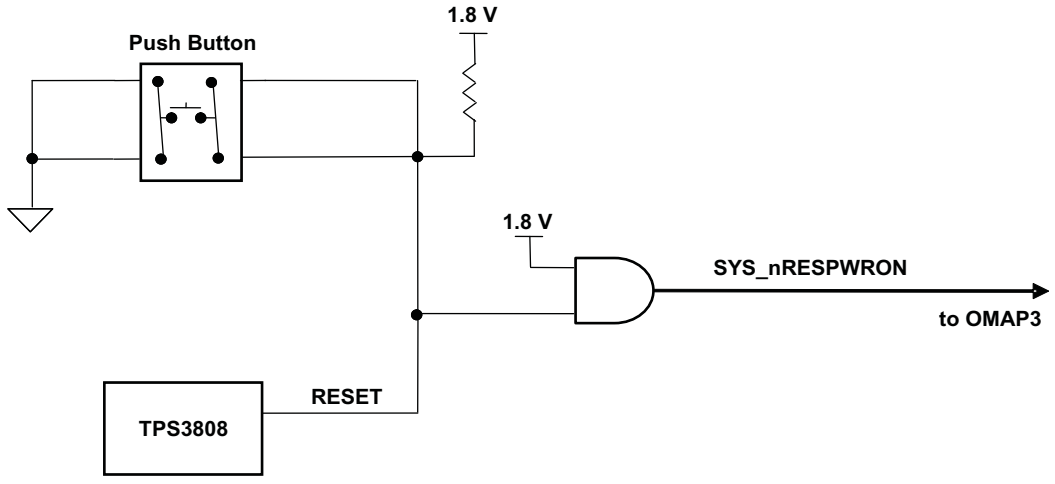
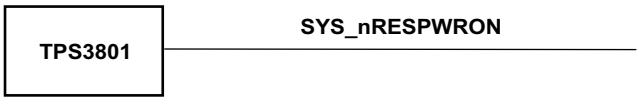


Figure 4. Circuitry to Combine Multiple Reset Sources

If multiple reset sources are not needed, a TPS3801 (with push-pull output buffer) can be used and directly connected to the OMAP™3 SYS_nRESPWRON signal.



3.1.2 SYS_nRESPWRON Timing

Typical 32-kHz oscillators on the market can have up to a 1-second maximum to stabilize. This poses a challenge in the power-up sequencing in that the reset signal must be maintained low throughout this stabilization time in order to properly reset OMAP™3. You can achieve this lengthy reset time using devices such as TPS3808 supervisory circuit. The schematic in Figure 5 is just one example of how to achieve this. You may need to adjust your reset time depending on the specifications of the oscillator you choose. See the TPS3808 data sheet (SBVS050) for more detailed information.

1. SYS_nRESPWRON is first delayed by U4 (TPS3808). The timing of the RST output of this device depends on the SNS signal plus the amount of delay as determined by the CT input. In this case, the SNS signal is determined by VDD_CORE, which is the second supply to ramp in the sequence. Once that voltage is reached, the delay is determined by:

$$\text{Delay} = \frac{C_T\,(\text{nF})}{175} = +\,0.5 \times 10^{-3}\,(\text{s})$$

$$\text{Delay} = \frac{220(\text{nF})}{175} = +\,0.5 \times 10^{-3}\,(\text{s})$$

$$\text{Delay} = 1.26\ \text{s}$$

2. The output of the TPS3808 is fed into the TPS3801, which ultimately controls the SYS_nRESPWRON signal. This device has a fixed 200-ms delay from the rising edge of MR.

   Thus, the total delay (from 1.8 V valid to rising edge of SYS_nRESPWRON) is:

   1.26 s + 0.2 s = 1.46 s

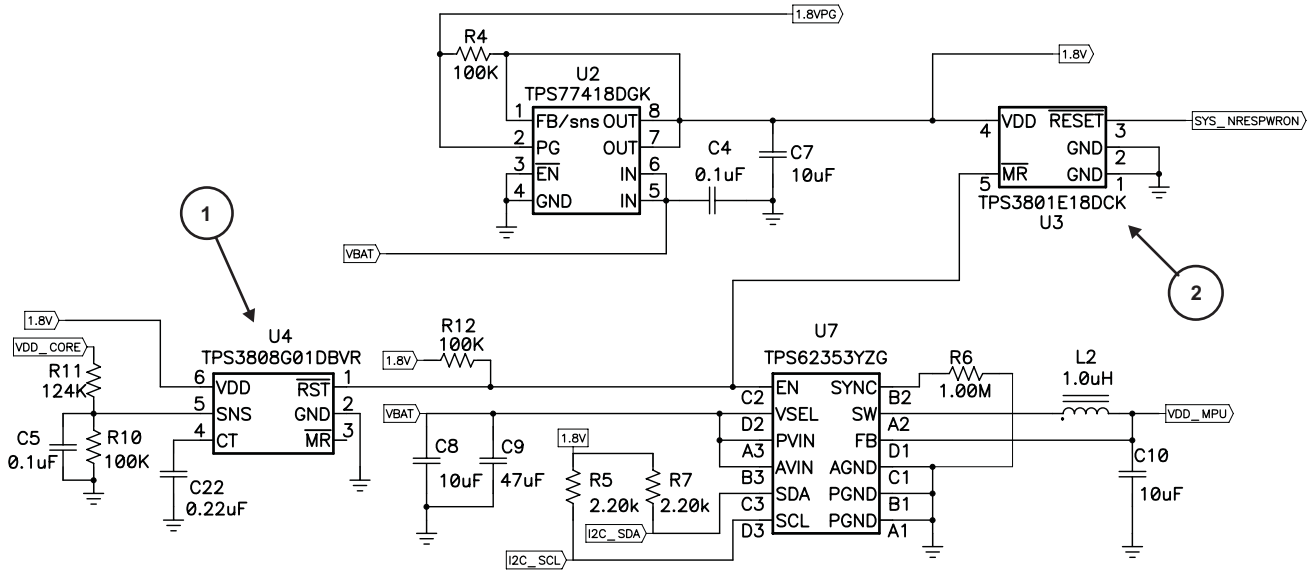


Figure 5. SYS_nRESPWRON Circuitry

3.2 Clocks

3.2.1 Clock Rise/Fall Time

OMAP™3 clocks (both 32-kHz and high-frequency clocks) also have strict rise/fall requirements. Note the excerpts from the data manual shown in Table 8.

Table 8. Clock Source Requirements

PAD	CLOCK FREQUENCY		STABILITY	DUTY CYCLE	JITTER	TRANSITION
sys_32k	32.768 kHz		±200 ppm	—	—	<20 ns
sys_xtalout sys_xtalin	12, 13, 16.8 or 19.2 MHz	Crystal	±25 ppm	NA	NA	NA
	12, 13, 16.8, 19.2, 26 or 38.4 MHz	Square	±50 ppm	45% to 55%	<1%	<2.5 ns
sys_altclk	48, 54, or up to 59 MHz		±50 ppm	40% to 60%	<1%	<10 ns

In order to meet these rise/fall times, a push-pull buffer is required to provide a faster edge on both clocks. See Figure 7 and Figure 8.

3.2.2 Clock Gating

When using an external oscillator for the high-frequency clock, the OMAP™3 SYS_CLKREQ signal is used to request the high-frequency clock. This signal can be used to gate the clock on power up while OMAP™3 is going through its power-up sequence.

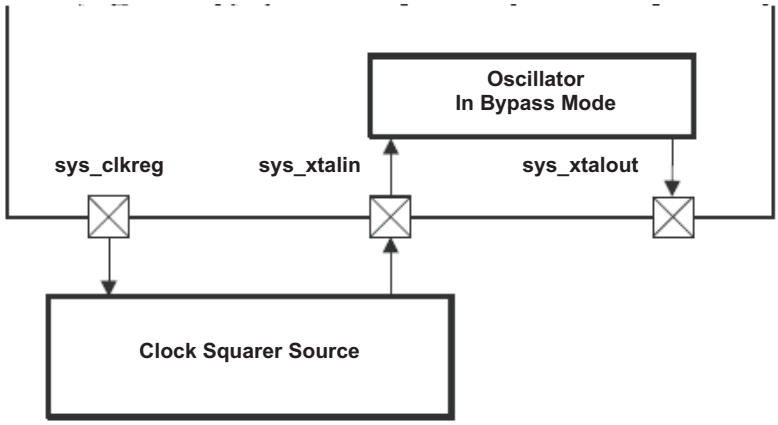


Figure 6. Clock Squarer Source Connection

Generally, the 32-kHz oscillator is powered off the 1.8-V supply. Use this as a condition before applying the 32 kHz to the I/Os of OMAP™3.

3.2.3 32-kHz Clock Circuit

If the 32-kHz oscillator you choose exceeds the rise/fall time limit, a push-pull output buffer must be used to create a faster edge. Generally, the 32-kHz oscillator is powered off the 1.8-V supply. Use this as a gating condition before applying the 32 kHz to the I/Os of OMAP™3.

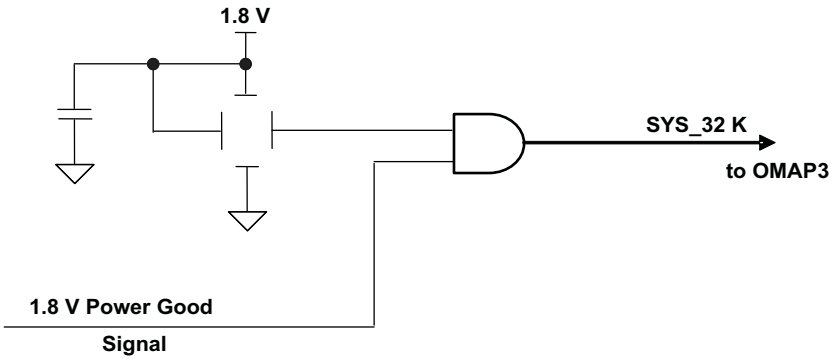


Figure 7. Push-Pull Buffer Circuitry on 32-kHz Clock

3.2.4 High-Frequency Clock Circuit

OMAP™3 requires a high-frequency clock for normal operation. OMAP™3 accepts two different types of input clock sources:

- A crystal can be used in combination with the internal OMAP™3 oscillator for frequencies 12, 13, 16.8, or 19.2 MHz.
- A square oscillator can be used with the OMAP™3 oscillator in bypass mode for frequencies 12, 13, 16.8, 19.2, 26, or 38.4 MHz

When an external oscillator is used, it has strict rise/fall time restrictions of less than 2.5 ns.

Table 9. Clock Source Requirements With External Oscillator

PAD	CLOCK FREQUENCY		STABILITY	DUTY CYCLE	JITTER	TRANSITION
sys_32k	32.768 kHz		±200 ppm	—	—	<20 ns
sys_xtalout sys_xtalin	12, 13, 16.8 or 19.2 MHz	Crystal	±25 ppm	NA	NA	NA
	12, 13, 16.8, 19.2, 26 or 38.4 MHz	Square	±50 ppm	45% to 55%	<1%	<2.5 ns
sys_altclk	48, 54, or up to 59 MHz		±50 ppm	40% to 60%	<1%	<10 ns

In order to meet these requirements, a push-pull buffer is required before the clock input of OMAP™3.

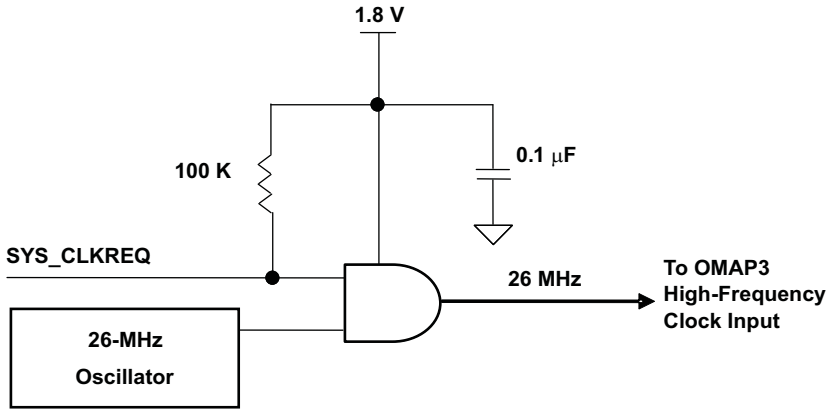


Figure 8. Push-Pull Buffer Circuitry on 26-MHz Clock

3.3 Power Devices

A TPS6235x-based power solution for OMAP™3 involves several different discrete power devices.

A 1.8-V supply is needed for OMAP™3 I/O. The block diagram in Figure 3 shows that a TPS77418 fixed-voltage LDO was used. When choosing this device, the following considerations were made:

- Provided enough supply current (250 mA) for OMAP™3 and other device I/Os
- Provided a Power Good signal to facilitate OMAP™3 power sequencing

Separate 1.8-V supplies are needed for PLLs and DAC voltage rails. The PLL voltage rails is involved in the power-up sequencing of OMAP™3, while the DAC voltage rails are turned on/off based on application needs. The TPS71219 dual output was chosen for the following reasons:

- Provided enough supply current (250 mA) for both voltages
- Provided independent enable signals for each voltage to facilitate OMAP™3 power sequencing and application control.
- Provided ultralow noise and high power-supply rejection ratio for PLL supply.
- Provided 1.8 V EN to connect directly to OMAP™3 GPIO

If you are not using the video DAC on OMAP™3, this dual LDO is unnecessary, and only one LDO is required for the PLL supply.

A separate voltage also is needed to support a MMC interface. Like the DAC, this voltage is enabled/disabled based on application need. The TPS728185315 was chosen for the following reasons:

- Dual voltage capable (1.85 V and 3.15 V) based on GPIO input. Note these voltages are within the specified tolerances for OMAP™3 MMC voltage.
- EN and VSET inputs compatible with OMAP™3 1.8-V GPIO
- Provided enough supply current (200 mA) for MMC applications

Figure 9 is an example schematic of the two TPS6235x devices used to power OMAP™3.

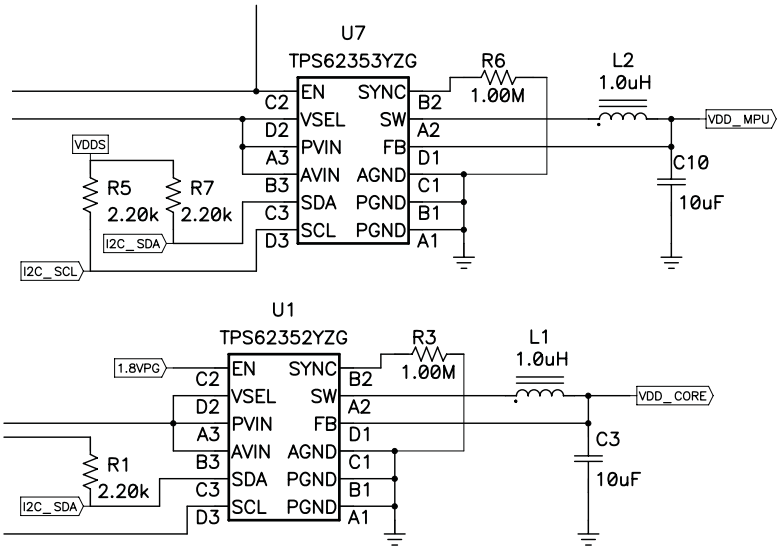


Figure 9. TPS6235x Circuitry to Power OMAP35x Core Voltages

For OMAP™3, the suggested implementation is to use the TPS62353 for VDD_MPU, and the TPS62352 for VDD_CORE. These devices were chosen for the following reasons:

- Each device has its own I2C address so OMAP™3 can distinguish them.
- The TPS62353 and TPS62352 allow for control over the full range of voltages for both VDD_MPU and VDD_CORE, respectively.
- The EN pin of each device allows for proper OMAP™3 power-up sequencing.
- By pulling VSEL high, the VSEL1 register in each device can be exclusively used to adjust voltage levels.

- Only one I2C write is needed to change voltage levels. This allows support up to Class-3 SmartReflex™.
- Provided enough supply current (800 mA) for an OMAP3503 or OMAP3515 design. *Note that this power supply solution is unsuitable for the high-current requirements of OMAP3525 and OMAP3530.*
- Optimized power-save modes at light load currents and can maintain high efficiency over the entire load current range
- Provided proper voltage ranges for both supply voltages.
- Provided high granularity (12.5 mV) for voltage scaling

3.4 Sleep/Standby Modes

As described in Power Requirements and Features of OMAP35x, the OMAP35xx has many power management features that make it attractive in power-sensitive applications. One aspect of this is the sleep/standby modes of OMAP™3, which allow the device to enter very low power states while maintaining certain levels of functionality. The OMAP35xx also has the ability to go into a deep sleep mode and still recognize wakeup events when needed.

With a TPS6235x power solution, you can implement a majority of these sleep/standby modes which allow you to take advantage of the power savings of an OMAP35xx solution. Many different sleep/standby modes exist, depending on which portions of OMAP™3 need to be active for your application. With the TPS6235x solution, you have control over PLL, video DAC, and MMC voltage, allowing you to completely shut off these supplies if needed. You can also bring OMAP™3 into some sleep modes by reducing voltage on VDD_MPU and VDD_CORE to the lowest retention voltage (0.95 V). By implementing SmartReflex™, these voltages can potentially be lower, thus enabling further power savings. Using the PRCM in OMAP™3, you also can cut the power going to different domains on the device, including the domains for VDD_MPU and VDD_CORE. This brings you to near OFF mode power levels by reducing leakage power of OMAP™3.

The last step in OFF mode sequencing involves shutting down the power IC. This step is not supported by the TPS6235x power solution if your application requires wakeup from sleep mode. It is recommended to keep VDD_MPU and VDD_CORE at the lowest retention voltage (0.95 V) for the lowest possible sleep mode. Although you cannot achieve complete OFF mode power levels, you can still obtain very low sleep power scenarios with a TPS6235x solution.

Wakeup then can be achieved using I2C commands from the PRCM on OMAP™3. See the OMAP™3 Technical Reference Manual for more information on Sleep and Wakeup sequencing.

3.5 Enabling Class-2 or Class-3 SmartReflex™ Implementations

Implementing either Class-2 or Class-3 SmartReflex™ with TPS6235x devices requires some hardware and configuration setup. The following table outlines a comparison of the implementation

	Class 2	Class 3
I2C functionality	I2C read/writes with I2C1/I2C2/I2C3 allowed to/from TPS6235x	Only I2C writes with I2C4 allowed
ARM activity	Requires more ARM code overhead to interpret voltage change and send/receive command via I2C	No ARM overhead required. Once SmartReflex™ subchip is configured for a certain OPP, it autonomously adjusts voltage via I2C4.

Class-2 SmartReflex™ Implementation

With a Class-2 SmartReflex™ implementation, the ARM processor in OMAP™3 controls all of the functions of the TPS devices. You can use either OMAP™3 I2C1, I2C2, or I2C3 to connect to the I2C port of the TPS6235x. If possible, use a dedicated I2C bus between OMAP™3 and TPS6235x. If you must share the bus with other peripherals, group the TPS6235x devices with peripherals, which require only infrequent I2C activity. This avoids long latencies during voltage changes.

To configure the TPS6235x devices for Class-2 SmartReflex™ operation, initialize them as follows:

- Ensure HW_nSW = 1.
- Set slew rate to 9.6 mV/µs (for OMAP™, slew rate must be between 4-16 mV/µs)

With the VSEL signal pulled high, all voltage control is achieved through VSEL1 register. VSEL0 register is not used. Also, with HW_nSW = 1, the GO bit is not used. A direct write to VSEL1 register changes the voltage with the specified slew rate.

Class-3 SmartReflex™ Implementation

With a Class-3 SmartReflex™ implementation, less burden is on the ARM processor because the SmartReflex™ subchip in OMAP™3 handles the voltage control and I2C commands to the TPS6235x. In this case, only I2C4 can be used, as this is the I2C port that the SmartReflex™ subchip uses to connect to external power supply devices.

One restriction you have when using I2C4 is that it is a write-only port. You cannot read TPS6235x registers to gather status or confirm transactions. You must keep track of the register settings by keeping a local copy of the values.

Also, in order to initialize the TPS6235x devices, put I2C4 in a bypass mode to use it as a generic I2C port for sending commands. Once the TPS6235x is set up properly, I2C4 can be switched over and controlled by the SmartReflex™ subchip. See the OMAP™3 Technical Reference Manual for more information about these registers in the PRCM:

PRM_VC_BYPASS_VAL – used to specify address, subaddress, and data, to write through I2C4 to power IC device.

Several registers in OMAP™3 must be initialized so that the SmartReflex™ subchip uses the proper I2C device and register addresses associated with each external power IC. See the OMAP™3 Technical Reference Manual for more information about these registers:

PRM_VC_SMPS_SA – used to set the I2C address of power IC devices on VDD_MPU and VDD_CORE

PRM_VC_SMPS_VOL_RA – used to set the subaddress of the register in the power IC, which controls the voltage on VDD_MPU or VDD_CORE.

PRM_VC_SMPS_CMD_RA – used to set the subaddress of the register in the power IC, which controls the enable/disable of the voltage on VDD_MPU or VDD_CORE

PRM_VC_CMD_VAL_0/1 – used to set I2C data values for different voltage levels

PRM_VC_CH_CONF – used to setup which address is used for each power IC

3.6 MMC Boot

The OMAP™3 processor has the ability to boot from many different sources. One possible boot configuration is to boot from MMC. This configuration requires that the MMC memory card is properly powered before ROM code executes (i.e., on power on reset).

If MMC boot is a requirement in your application, you must ensure that VDDS_MMC1 (and VDDS_MMC1A if using 8-bit MMC data) is set for 3-V operation at power up. It can later be turned off if necessary by your application.

In the following example schematic of Figure 10, MMC1_EN and MMC1_VSET are connected directly to OMAP™3 GPIOs. To ensure this power device is enabled and supplying 3.15 V at OMAP™3 power on reset, both MMC1_EN and MMC1_VSET must be high by default. To achieve this, choose OMAP™3 GPIOs which default high at power up, or use an inverter where necessary.

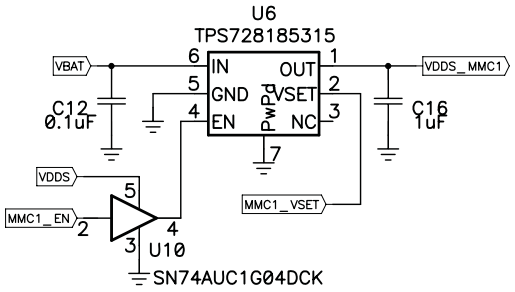


Figure 10. LDO Circuitry to Provide MMC1 Voltage

Some applications may require MMC voltage sequencing to ensure that 3.3 V is valid before 1.8 V. For this case, use two LDOs for each voltage to ensure proper sequencing, then enable/disable them using OMAP™3 GPIOs.

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