

# Designing With TPS7H3301-SP Double Data Rate (DDR) Termination

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## ABSTRACT

This application note provides the basics of DDR memory. It is mainly intended as a guide for the designer designing with TPS7H3301-SP for space system applications. Application note highlights critical rails of DDR memory, discusses comparison of linear versus switcher approach and finally the design criteria's that are critical to ensure proper design performance with TPS7H3301-SP DDR termination regulator.

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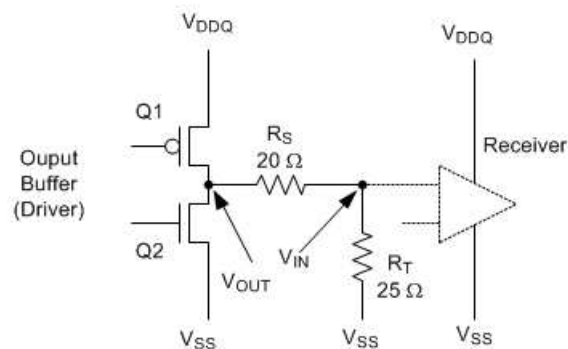
## 1 DDR Memory and SSTL Basics

In commercial applications, there are two forms of memory that are commonly used in computer systems non-Volatile memory and volatile memory. Whereas non-volatile memory is memory that can retain the stored information even when not powered. Example of non-volatile memory includes flash memory, ferroelectric RAM (F-RAM), magneto resistive RAM (MRAM). Whereas contrary to non-volatile memory, volatile memory is memory that requires power to maintain the stored information which can be static RAM (SRAM) or dynamic RAM (DRAM). The two types differ in the technology they use to hold data. Though SRAM is faster as it does not need to be refreshed, whereas DRAM needs to be refreshed thousands of times per second. DRAM is more popular as it is lower cost and the most popular type of DRAM is DDR SDRAM (DDR-Synchronous DRAM).

However for the space market where the memory is only now migrating from SDRAM to DDR-SDRAM, thus allowing higher bus speeds, and higher data transfer rates are attainable. DDR memory is called double data rate because it clocks the data into the memory device on both rising and falling edge of the clock. Because the DDR operates at very high switching speed thus bus termination resistors are needed to control the impedance of the clock lines.

Traditionally, logic systems were designed to clock on only one edge of the clock namely rising edge of the clock to transfer data, while in DDR memory clocks on both the leading and falling edge of clock. For example, in a DDR200 device the data transfer frequency is 200 MHz, but the bus speed is 100 MHz.

There are various approaches that can be used to terminate a transmission line into its characteristic impedance. Bus termination resistor connected at the end of distribution network and connected to ground is shown below in [Figure 1](#). If bus driver is in low state, resistors have zero power dissipation, whereas when the bus driver is in high state resistors dissipate  $V_{DD}$  squared divided by the bus resistance ( $R_S + R_T$ ). Where bus resistance is the series combination of source resistance ( $R_S$ ) and common bus termination ( $R_T$ ) resistance.



**Figure 1** Grounded Termination Resistor

Alternately the series stub termination logic (SSTL) used in DDR design, involves using one series resistor attached from the controller to the memory and one termination resistor attached to the termination rail ( $V_{TT}$ ). When the Common bus termination resistor is tied to  $V_{TT}$  ( $V_{DDQ} / 2$ ), this results in power savings as power dissipation will be  $V_{TT}$  squared divided by termination resistance. We have equal power dissipation when the driver is high or low.

As in any power systems, the motivation in going to DDR memory from SDRAM memory is due to higher performance as a result of DDR and improved power management as less heat is dissipated since DDR memory operates at lower voltage.

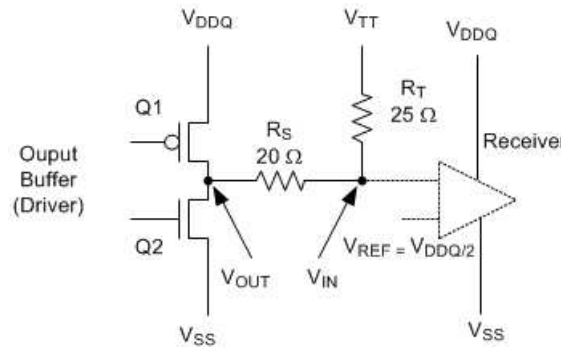


Figure 2. Termination Resistor Connected to  $V_{TT} = V_{DDQ} / 2$

When the driver outputs are high, termination voltage  $V_{TT}$  will have current flowing into it. When the bus driver output is low then you will have current flowing from the  $V_{TT}$  power supply thru the resistors ( $R_T + R_S$ ) into output buffer. Thus current is a function of driver stage, whether you are sourcing or sinking current.

## 2 Critical Rails for DDR Memory

Most DDR memory devices use a common supply for core, I/O and logic voltages; these terms are commonly combined and referred to simply as drain-to-drain core voltage ( $V_{DDQ}$ ).

$V_{TTREF}$  (termination-tracking reference voltage) is a low current precision reference voltage.  $V_{TTREF}$  tracks 1/2 of  $V_{DDQSNS}$  and is capable of sourcing and sinking a load up to 10 mA. Typical specification of  $V_{TTREF}$  is  $0.49$  to  $0.51 \times V_{DDQSNS}$ .

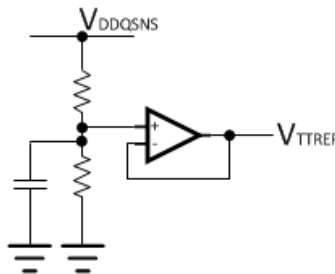


Figure 3.  $V_{TTREF}$  Buffered Output

$V_{TT}$  (terminator tracking voltage) is high current capable midrail. Current requirements of  $V_{TT}$  are dependent upon total lines in the memory system. This includes address and data lines. The total peak current would be number of lines multiplied by current consumed by each line. For DDR, each line can consume as much as 20 mA/data/address channel whereas for DDR3 it can be as high as 15 mA/line.

$$I_{TT\_max} = \left( \frac{V_{TT}}{R_{Term}} \right) \times \text{Number\_Lines} \quad (1)$$

The midrail  $V_{TT}$  in SSTL and DDR-memory devices is different. When the SSTL circuit generates a zero, an active pulldown device sinks current from the termination rail, and the termination supply acts as a conventional supply voltage, sourcing the required current to maintain the desired termination voltage. However, when the logic circuit generates a one, a pullup device sources current into the termination rail, and the termination supply must suddenly become a load, sinking current from the memory output. This sink-and-source requirement significantly increases the complexity of the  $V_{TT}$  design but provides a valuable feature to the memory device. Because standard LDOs cannot sink current, source/sink LDO is needed to meet the challenge. Alternately, a tracking switcher can also meet the challenge.

$V_{in} / V_{DD}$  bias supply for the TPS7H3301-SP this is nominally 2.5-V or 3.3-V rails provides bias to the internal logic including drive circuitry for the LDOs.

### 3 Switcher versus Linear for $V_{TT}$ Termination

There are a number of options, whether one uses a linear or a switcher solution for the DDR termination. Switcher will give you high peak power with high efficiency, however it will have higher component count, lower bandwidth, and higher output noise. A linear solution provides less output noise, higher bandwidth, and lower cost.

With randomness of the driver stages, actual measured current may be significantly less than the worst case calculated current, thus the lower efficiency due to linear DDR may not pose a thermal concern at system level.

Even though the worst case load calculations may indicate the system load transitioning from  $-3$  A to  $+3$  A when going from sinking to sourcing the load, this can only occur if we go from all 0s to all 1s, and this condition stays for longer than the inverse of converter bandwidth. For a linear converter with a bandwidth of 80 kHz, this implies about 12.5  $\mu$ s, and for the switcher with its bandwidth in the range of 20 kHz, this implies about 50  $\mu$ s. With the memory bus operating at hundreds of MHz, then the bus needs to stay at all 0s or all 1s for 1250 to 5000 cycles. Probability of having all 1's or all 0's for such a long time is very low.

Because a single capacitor may not be sufficient to ensure that the impedance is low over various frequency ranges of interest, it becomes important to connect various output capacitors in parallel to extend the bandwidth.

To meet the output impedance requirements, one can connect various capacitors in parallel using both tantalum and ceramic capacitors. However, caution must be taken when connecting different values of capacitors in parallel. When capacitors of different values of capacitors are placed in parallel, they can produce an unwanted effect referred to as anti-resonance. An anti-resonance peak is generated when one capacitor has gone inductive while the other capacitor of a different value is capacitive.

One can use a tool such as K-Sim, a Pspice simulator from Kemet, to assess the output impedance of a capacitor network. Adding various capacitor values allows one to extend the impedance bandwidth.

[Figure 4](#) shows an example of various values of ceramic capacitors in parallel with tantalum capacitors, resulting in anti-resonance.

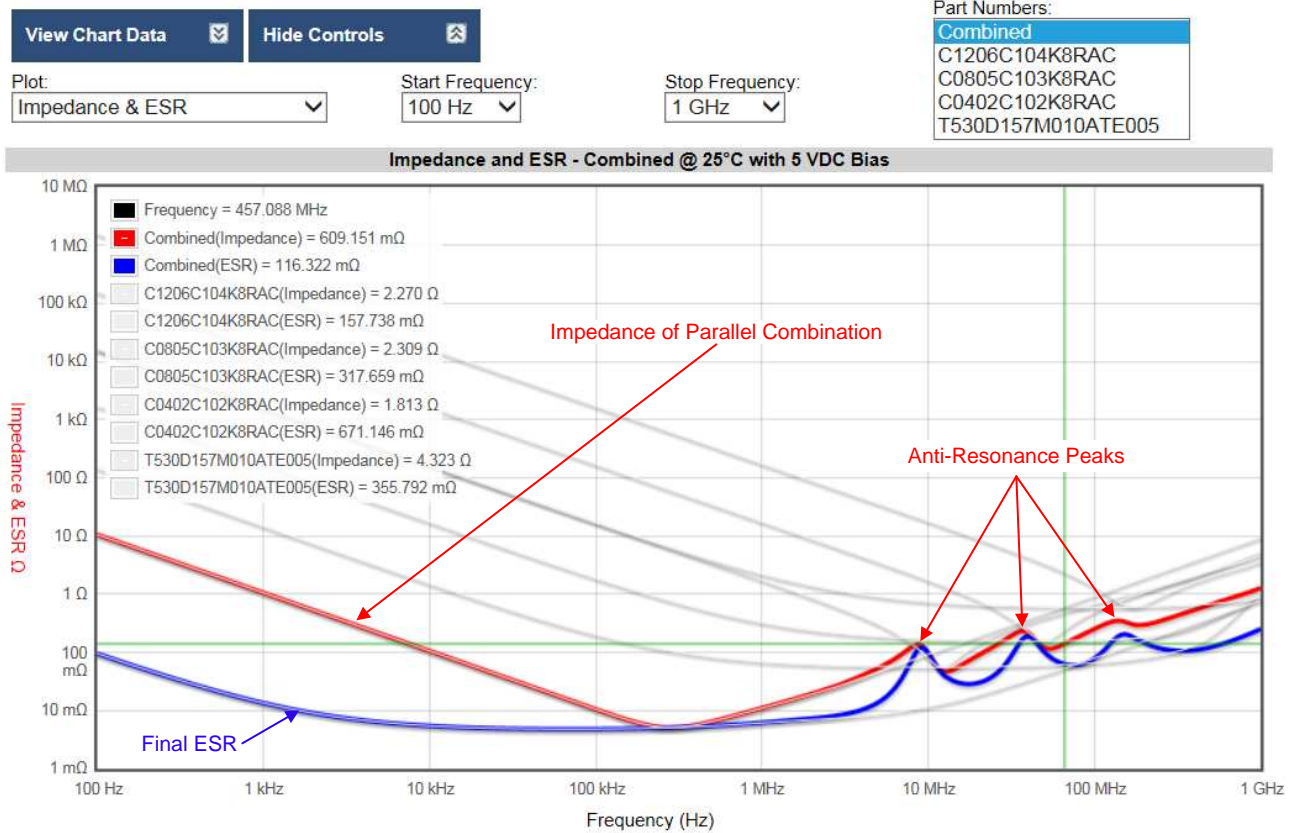


Figure 4. Paralleling Various Tantalum and Ceramics Capacitors Using KSIIM from Kemet

#### 4 Using the TPS7H3301-SP: Design Guidelines

The typical application schematic shown in Figure 5 highlights the DDR application. The schematic highlights various pinouts and their associated functions.

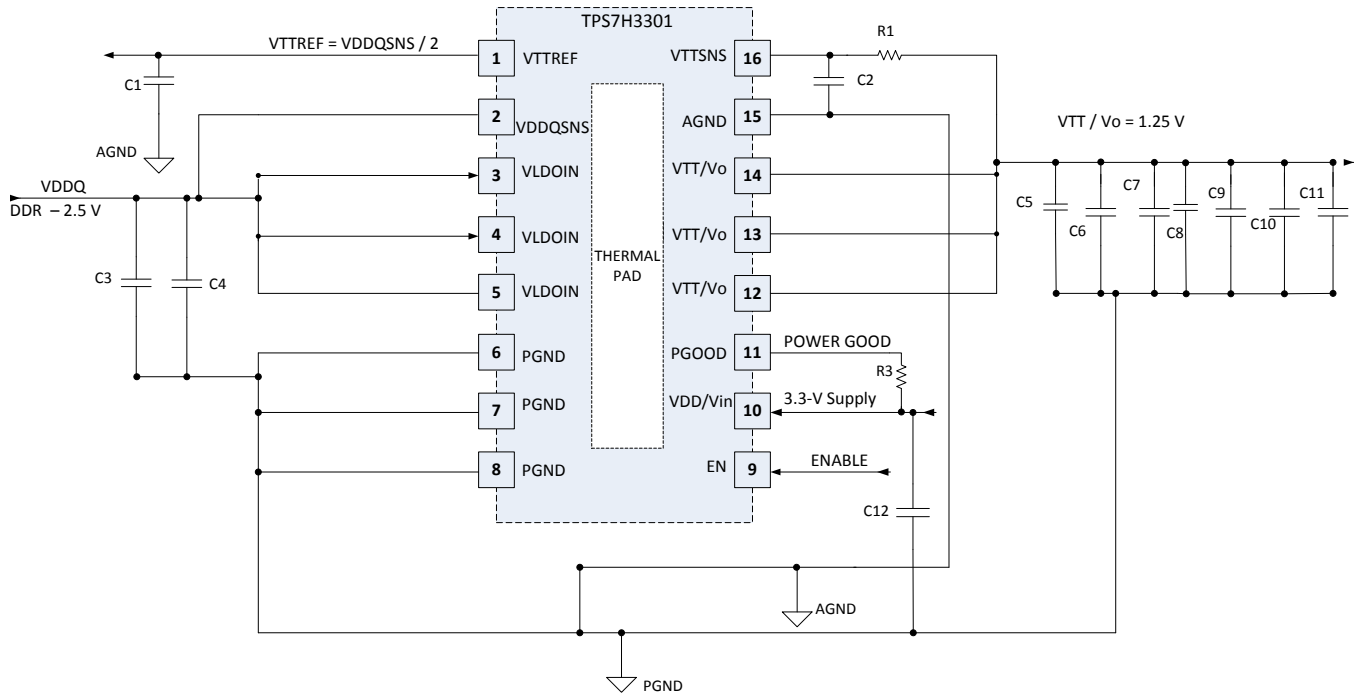


Figure 5. Typical Application Schematic of DDR Termination

#### 5 $V_{LDOIN}$ Considerations

TPS7H3301-SP incorporates a dedicated pin  $V_{LDOIN}$ . This can help improve efficiency by minimizing LDO power dissipation in user application. One must ensure that minimum  $V_{LDOIN}$  voltage meets the dropout requirements as highlighted in the data sheet. For example for the DDR application where  $V_{TT} = 1.25\text{ V}$ ,  $V_{LDOIN\_min} \geq V_{TT} + V_{dropout}$  threshold per system application. Thus having a separate voltage source for  $V_{LDOIN}$  and  $V_{DDQSNS}$  will help improve system efficiency.

TI recommends that  $V_{LDOIN}$  be isolated from  $V_{DDQSNS}$  and if this is not possible then an RC filter as shown in Figure 6 be used to isolate  $V_{DDQSNS}$  from  $V_{LDOIN}$ .

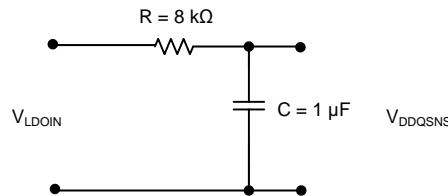


Figure 6. RC Filter to Isolate  $V_{LDOIN}$  to  $V_{DDQSNS}$

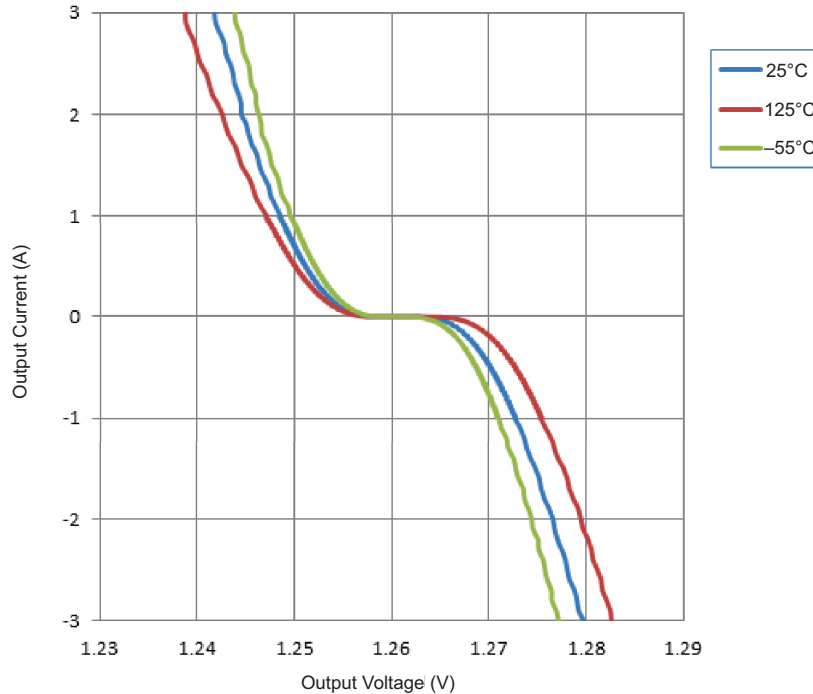
Adding RC filter to isolate  $V_{LDOIN}$  to  $V_{DDQSNS}$  will result in loss of dynamic tracking of  $V_{TT}$  to  $V_{TTREF}$ . For additional details see user's guide [SLVUAK2](#).

As  $V_{LDOIN}$  is a high current input that supports the output load requirements, thus it is important from system level that the input source ( $V_{LDOIN}$ ) must be able to supply DDR current limit set point as well as current necessary to charge the output capacitor bank, irrespective of output load current.

## 6 TPS7H3301-SP $G_m$ Driven LDO

TPS7H3301-SP is a  $G_m$  driven source – sink LDO. Transconductance ( $G_m$ ) is a measure of output current vs  $V_{TT}$  voltage, which is shown in Figure 7. By taking the tangent to the curve at the load point of interest, one can calculate  $G_m$ . As highlighted in Figure 7,  $G_m$  varies with output load current and  $G_m$  plot highlights dc load regulation of the design. For a typical  $G_m$  of 294 S at 3 A load current, load regulation of 3.4 mV/A and as the load reduces  $G_m$  of the converter will also reduce to the point that the feedback is practically operating in open loop. The  $G_m$  source/sink LDO is a single pole system, and its unity gain bandwidth for the voltage loop is only determined by the output capacitance.

Table 1 shows typical  $G_m$  for various load conditions.



$$V_{VIN} = 2.95 \text{ V}$$

$$V_{DDQSNS} = 2.5 \text{ V}$$

DDR1

Figure 7.  $G_m$  Curve (Output Current vs Output Voltage)

Table 1.  $I_{out}$  vs  $G_m$  for Various Load Conditions

$I_{out}$	$G_m$
0.15 A	82 A/V
1.25 A	230 A/V
2.0 A	270 A/V
3.0 A	294 A/V

By knowing the  $G_m$  at the desired load current and desired crossover frequency, the output capacitance can be calculated using Equation 2.

$G_m = 230 \text{ A/V}$  measured using the  $G_m$  curve at 1.25 A load current.

$f_c = 81 \text{ kHz}$  is the desired crossover frequency.

$$C_{out} = \frac{G_m}{2\pi f_c} \tag{2}$$

The minimum output capacitance calculated as  $C_{out} = 450 \mu\text{F}$ .

Select output capacitors to ensure that the capacitor esr is low, thus the zero introduced by  $C_{out}$  and its esr is at high frequency above the internal parasitic pole that is approximately 200 kHz.

Selection of lower  $f_c$  crossover frequency is dictated by fact that we want to ensure that we have acceptable phase margin. Though there are options such as adding a lead network in the output feedback to boost the phase margin, it has implications on the output load regulation.

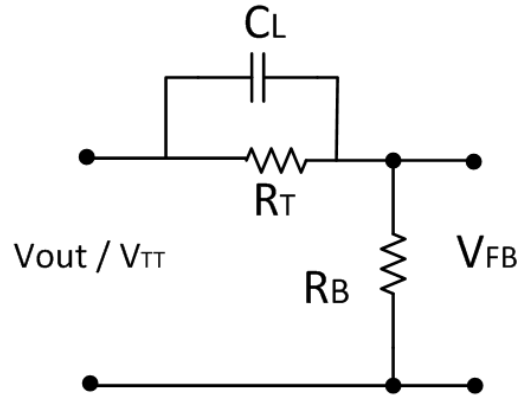


Figure 8. Lead Network to Boost Phase Margin

## 7 Droop Compensation

TPS7H3301-SP DDR termination incorporates droop compensation. Transconductance  $G_m$  of the device and output load determines the droop between the reference input  $V_{TTREF}$  and the output regulator  $V_{TT}$ .

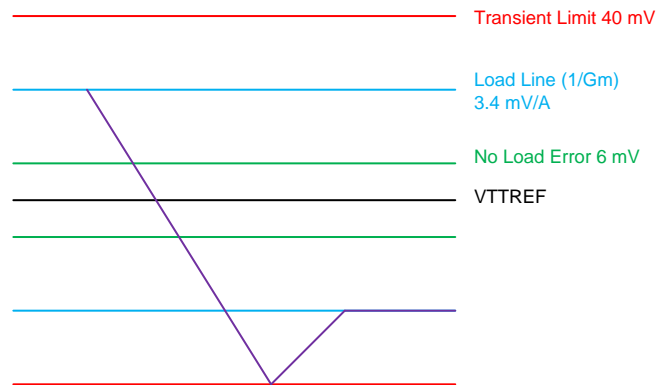


Figure 9. Transient With Load Line Droop

As can be seen from Figure 9, if the output load is at  $-3$  A, the output voltage  $V_{TT}$  will be at a higher dc level due to the load line. If we have a transient condition step load from  $-3$  A to  $+3$  A from sinking to sourcing, this provides a wider working voltage window for the transient as a result of droop compensation.

$$\text{Impedance} = \text{Voltage window} / \text{Load step.}$$

## 8 Design Considerations

An important fact that drives the selection of output impedance is to ensure that an esr of zero is introduced by output capacitance is at high frequency.

Using multiple Kemet T530D series capacitors in parallel  $150 \mu\text{F}/10$  V with esr =  $5 \text{ m}\Omega$  or the commercial off-the-shelf (COTS) for high reliability applications such as T540, T541 and T543 polymer tantalum capacitors can be used to meet the output impedance requirements.



$$C_{esr} = \frac{5 \text{ m}\Omega}{3} \tag{3}$$

$$C_{esr} = 1.66 \text{ m}\Omega$$

Modulator gain can be calculated as

$$\text{Mod\_Gain} = G_m R_L \tag{4}$$

$$\text{Mod\_gain\_db} = 20\log(\text{Mod\_gain}) \tag{5}$$

$R_L = 1 \Omega$  output load for DDR configuration where  $V_{TT} = 1.25 \text{ V}$ , thus  $I_{out} = 1.25 \text{ A}$ .

$$\text{Mod\_gain\_db} = 20\log(G_m R_L)$$

$$\text{Mod\_gain\_db} = 47.235 \tag{6}$$

$$\text{Mod\_Pole} = \frac{1}{2\pi R_L C_{out}}$$

$$\text{Mod\_Pole} = 352.174 \text{ Hz} \tag{7}$$

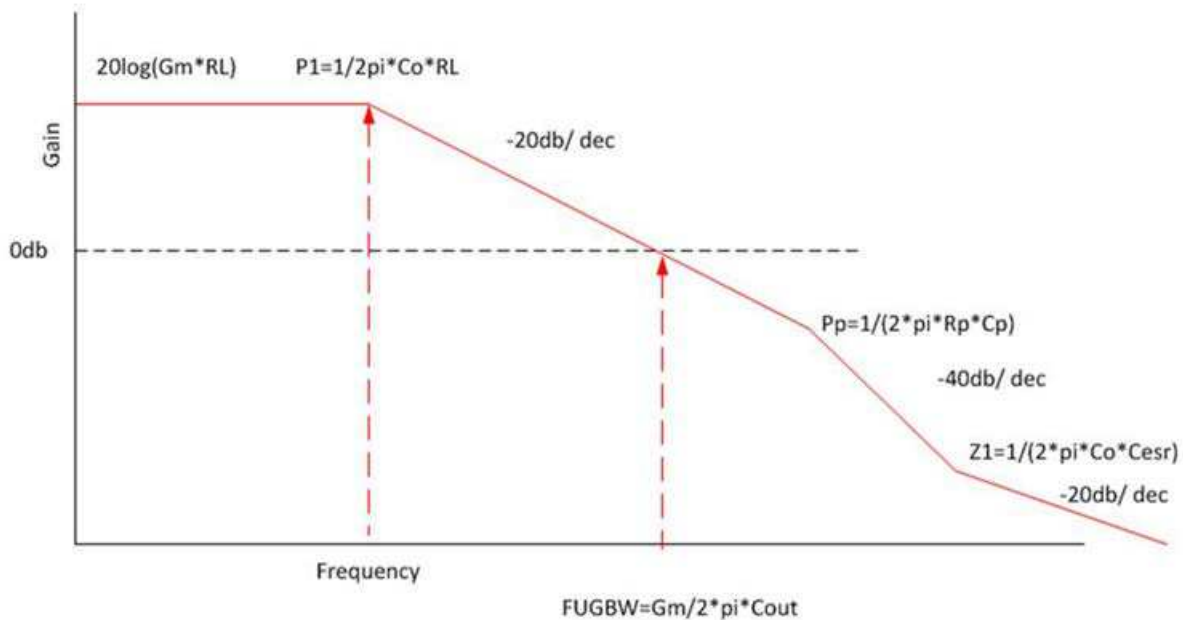
$$\text{Mod\_Zero} = \frac{1}{2\pi C_{esr} C_{out}}$$

$$\text{Mod\_Zero} = 211 \text{ kHz} \tag{8}$$

$$F_{UGBW} = \frac{G_m}{2\pi C_{out}}$$

where  $F_{UGBW}$  = Unity gain bandwidth

$$F_{UGBW} = 81 \text{ kHz} \tag{9}$$



**Figure 10. Plot Highlighting DDR Gain and Pole-Zero Locations**

Another design criteria that must be observed is that for frequency above the unity gain cross over frequency one should ensure that  $G_{m(f)} \times Z_{out(f)}$  must be less than 1 or 0 dB to ensure stable design.

It is important to understand and it must be highlighted that the output impedance of the capacitor network when multiplied by  $G_m$  should be less than 1 or 0 db in order to ensure we do not have multiple zero crossings and thus resulting in oscillation. Knowing the frequency response of  $G_m$  amplifiers becomes an important aspect of design in order to analyze the loop response above the crossover frequency. Thus, the designer can assess the frequency range over which the output impedance must be kept low.

At high frequency the capacitor banks ESL increases above the self-resonance frequency of capacitor as highlighted in Figure 14.

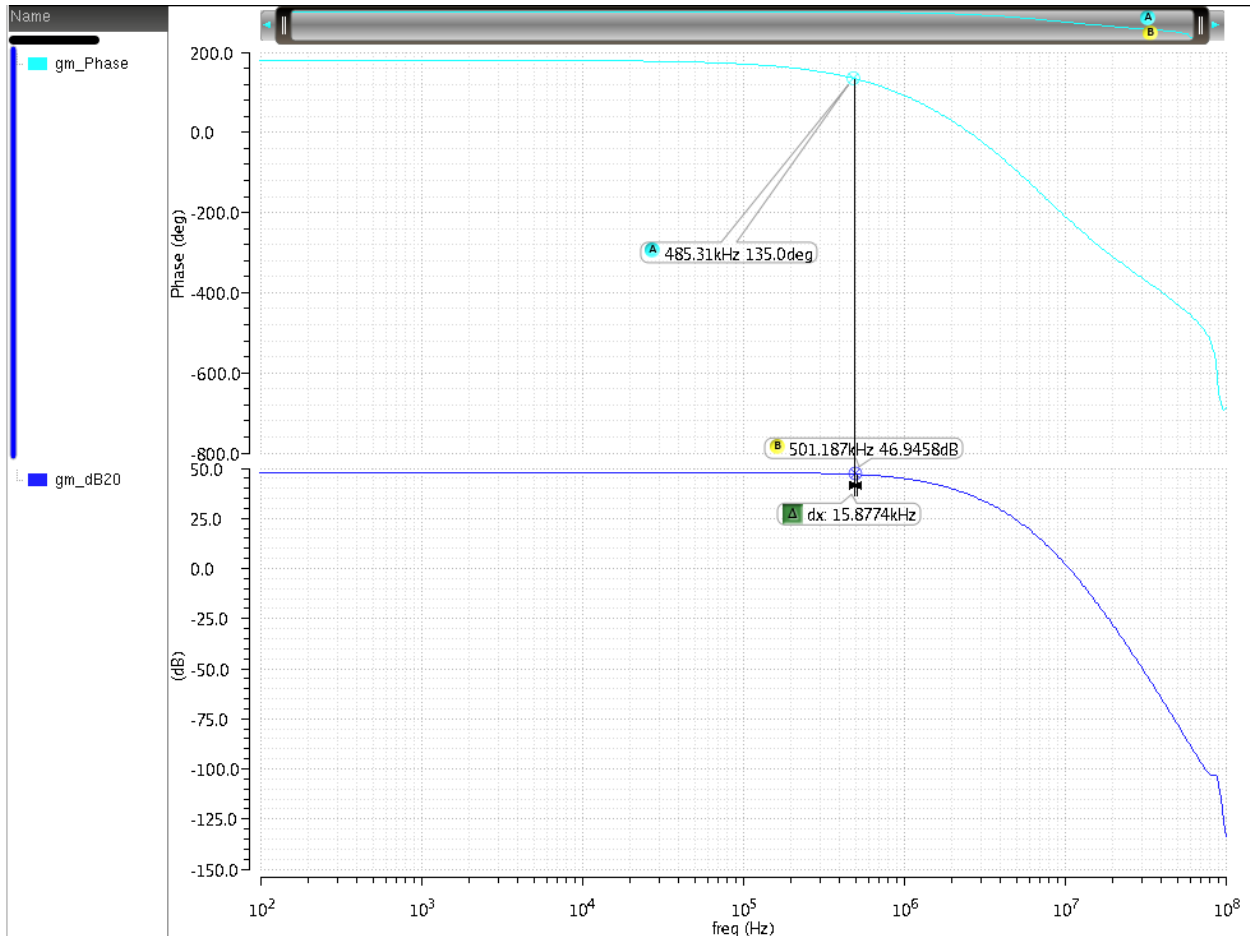


Figure 11.  $G_m$  vs Frequency

It is critical that one measure the output impedance of the capacitor network in design. Bode 100 from [www.picotest.com](http://www.picotest.com) was used in measuring the output impedance. As a first step proper calibration of equipment is critical. Thus a calibration board as shown below with 1  $\Omega$  shunt-thru is used to null out the effect of the leads connected from the source equipment to the DUT. Figure 12 shows the calibration board along with its schematic that has one ohm precision resistor used for calibration (see [1]).

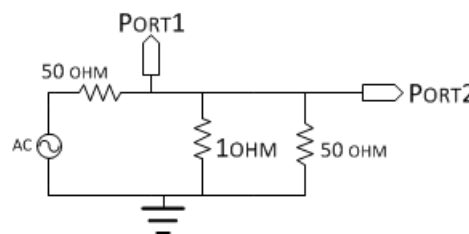
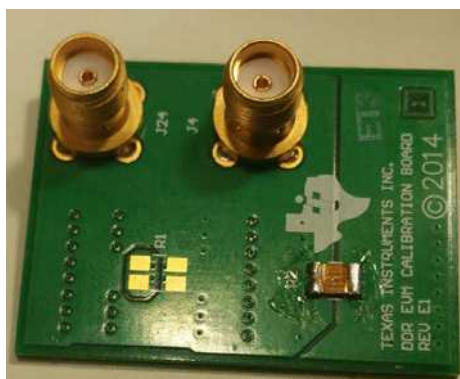


Figure 12. Two Port Shunt-Thru Impedance Measurement

After the equipment is properly calibrated, then one can use a capacitor test board in place of a calibration board and measure the output impedance of the capacitor bank. The example below highlights a ceramic and tantalum capacitor combination, though individual capacitors can also be measured similarly.

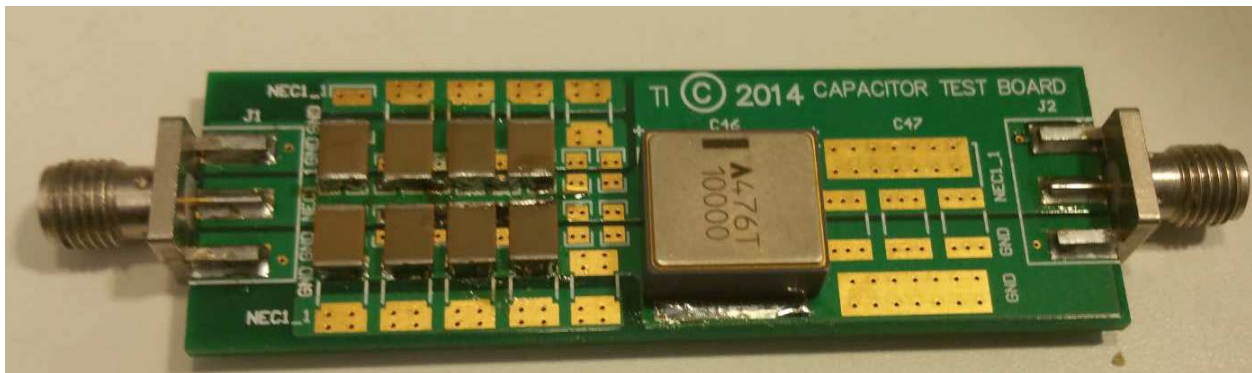
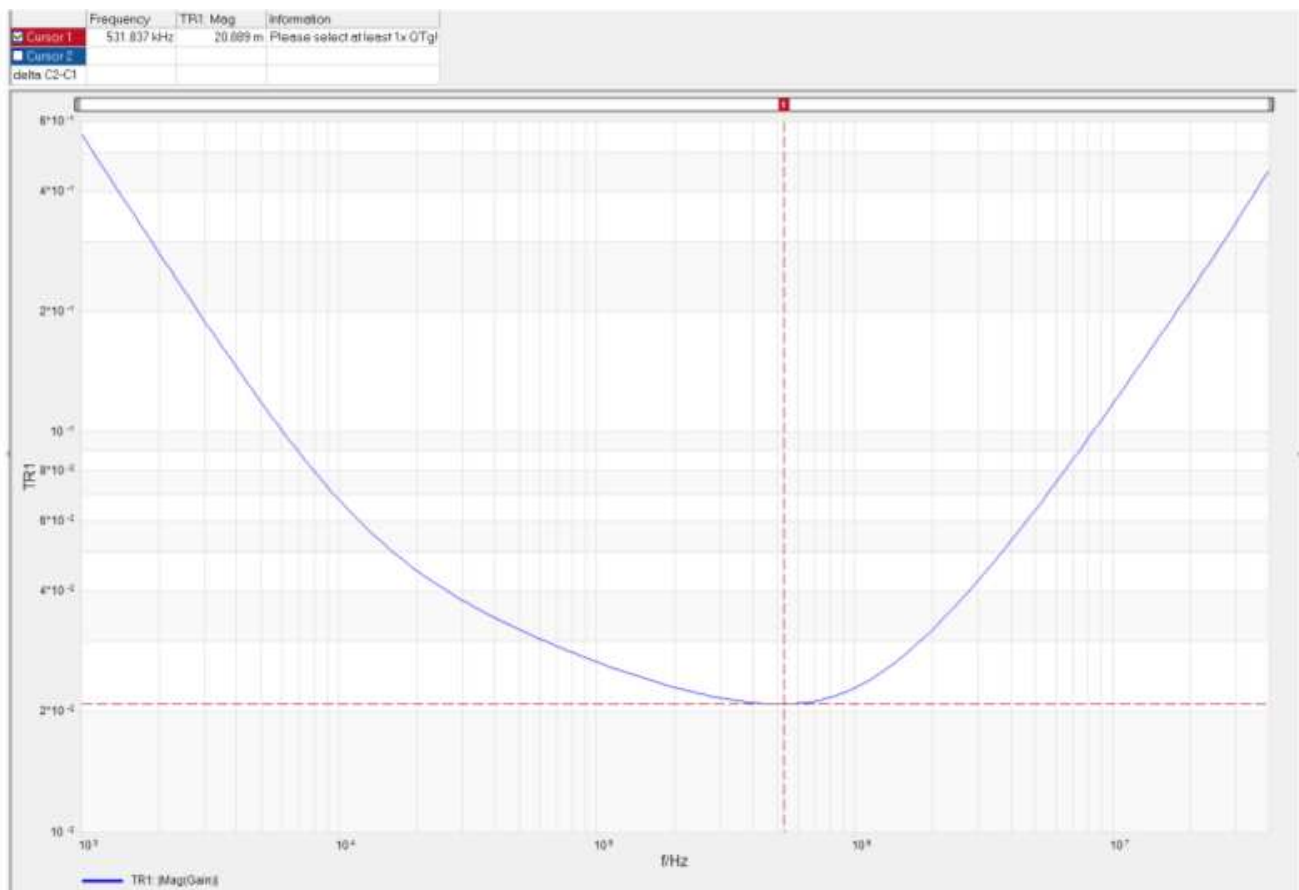


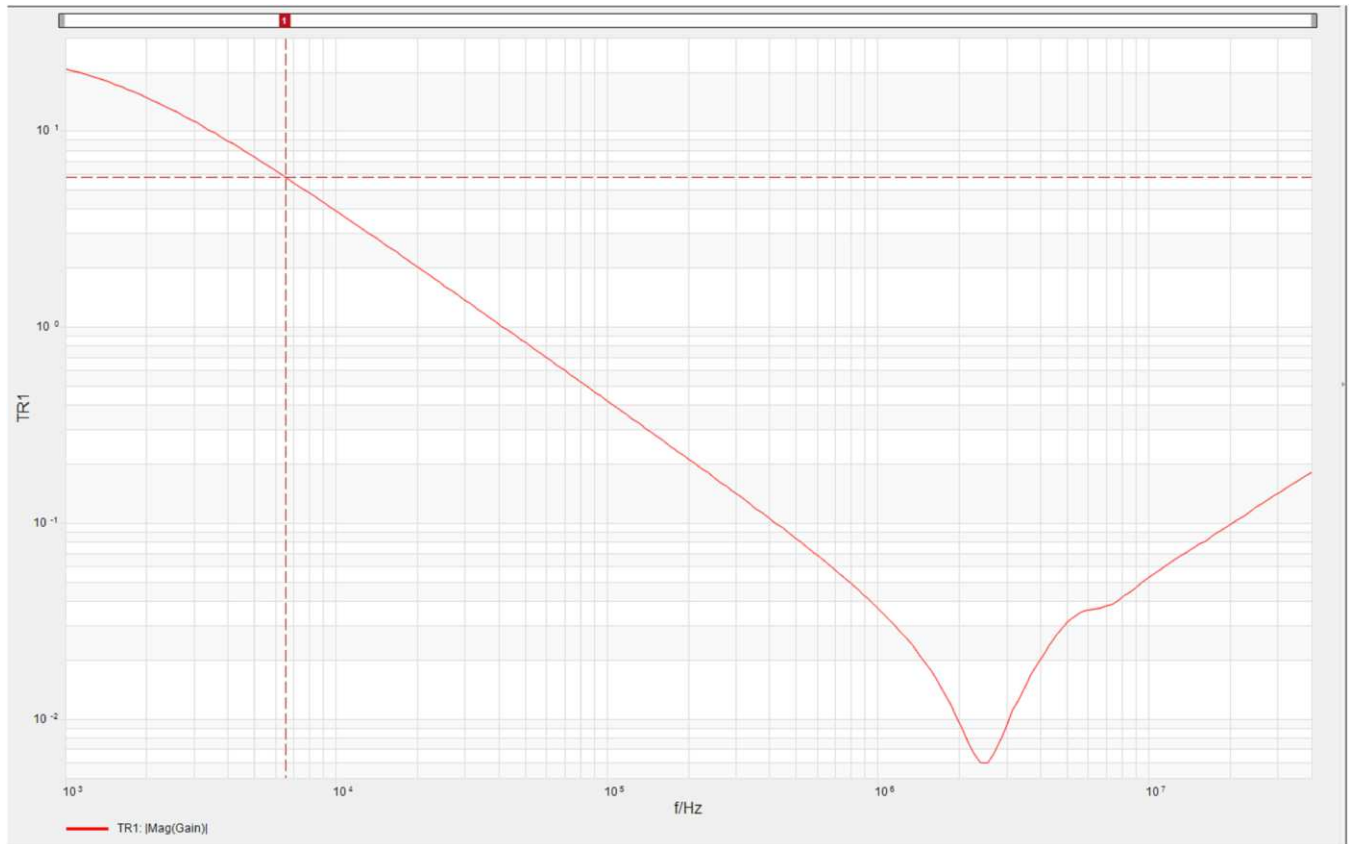
Figure 13. Capacitor Board to Measure Output Impedance of Capacitor Bank



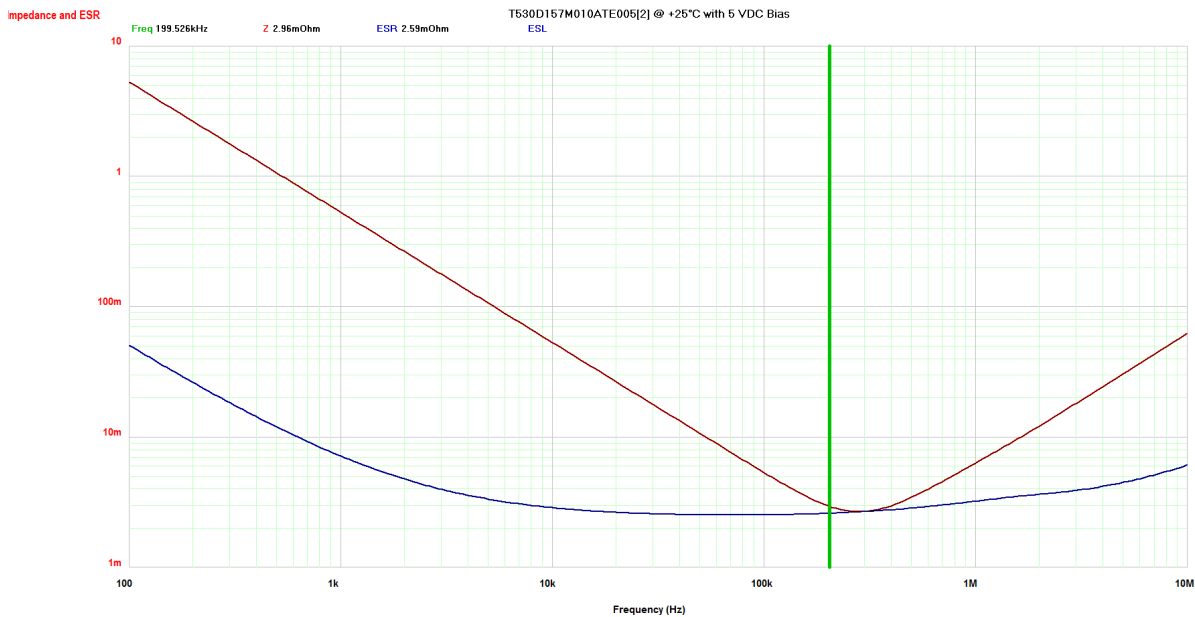
Output impedance for  $3 \times 100 \mu\text{F}$  TAZH107K010 (CWR29) only without the ceramic capacitors  
 Resonant frequency = 530 kHz  
 esr = 20 m $\Omega$  with three capacitors in parallel

Figure 14. Output Impedance Measurements of 3 Tantalum Capacitors TAZH107K010 in Parallel

Figure 14 highlights output impedance measurement of three TAZH107010 100uf/ 10V tantalum capacitors in parallel using Bode 100. Tantalum capacitor esr will increase with temperature, thus at low temperature its impedance can be as high as 3 times that at room temperature. This must be taken into consideration when determining the output impedance to meet system needs. Similarly we can measure the output impedance of Ceramic capacitors as shown in Figure 15. Ceramic capacitor highlights higher resonant frequency as expected. Thus a combination of both Tantalum and ceramic capacitors will provide optimum solution.



**Figure 15. Ceramic Capacitor 4.7  $\mu$ F / 10 V 1812 Package 1812X7R475\_10V Presidio Electronics Measured Data**



**Figure 16. Output Impedance of 3 × T530D157M010 Series Tantalum Capacitors**

From Figure 16, one can see that at a higher frequency above the resonance frequency of the capacitor bank, output impedance increases.

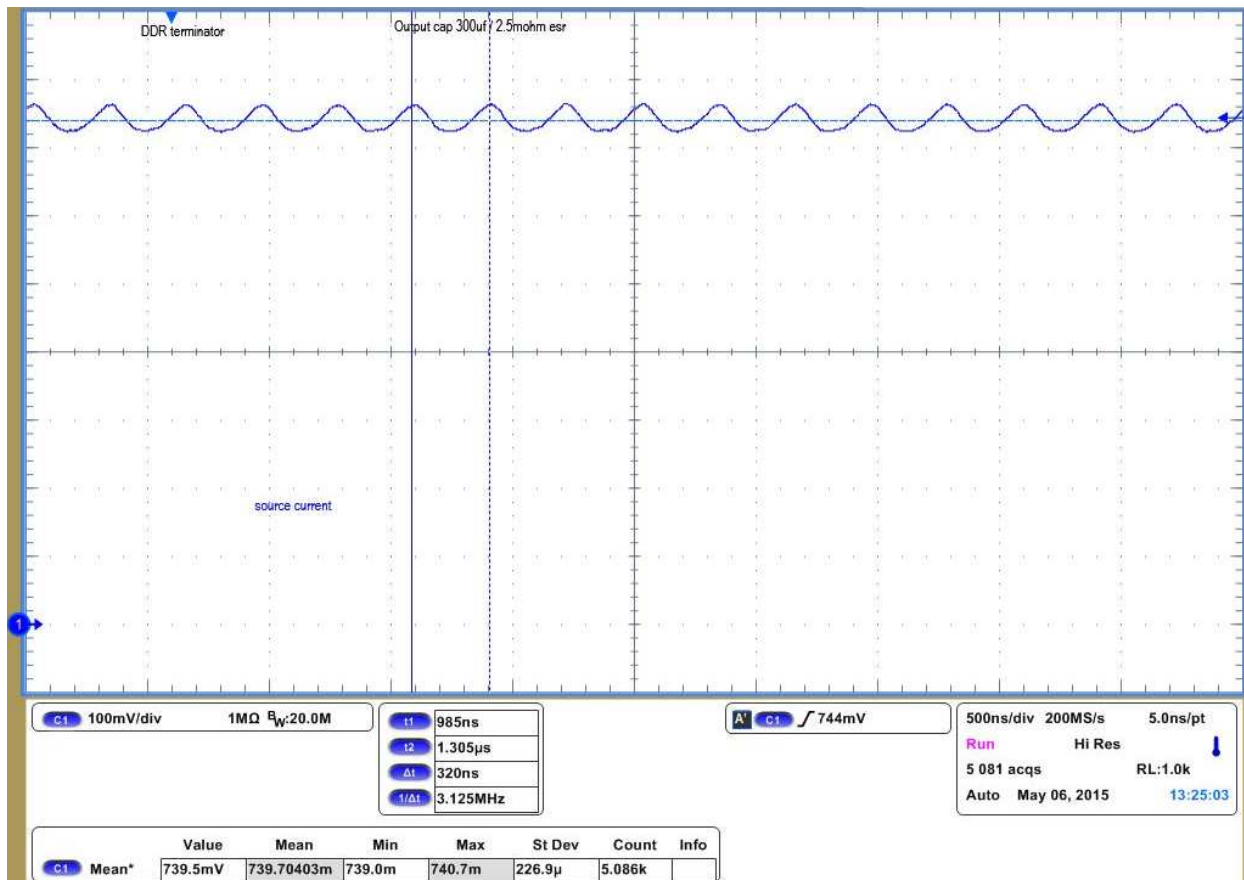
Figure 11 ( $G_m$  vs frequency) shows that the  $G_m = 35 \text{ db} = 56 \text{ A/V}$  at 3 MHz.

Figure 16 shows measured output impedance to be 18 mΩ at 3 MHz.

If  $G_{m(f)} \times Z_{out(f)}$  function of frequency becomes higher than 1 (0 dB) the it will introduce multiple unit gain crossings, leading to loop instability and oscillation will be observed on the output, as highlighted in Figure 17.

Thus use of design tool like Ksim from Kemet [www.ksim.kemet.com](http://www.ksim.kemet.com) one can estimate the output impedance of output capacitor bank. An alternate approach is to measure the output impedance of the capacitor bank in the system.

A simple way is to measure output impedance is to use tools like Bode 100 from [www.picotest.com](http://www.picotest.com). As highlighted earlier, in any measurement, Initial calibration of equipment is critical to ensure that a proper measurement is taken.

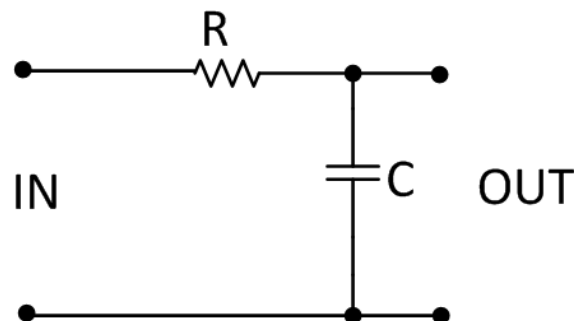


**Figure 17. Output Oscillation as a Result of Higher Output Impedance at 3 MHz**

We must ensure that the output impedance at a higher bandwidth is low, such that when  $G_{m(f)} \times Z_{out(f)}$  is less than 1 or (0 db).

One solution to address this concern is to introduce a pole in the feedback network and thus output impedance at reduced at higher frequency.

Adding a pole will ensure that we have an adequate gain margin.



**Figure 18. Output Pole**

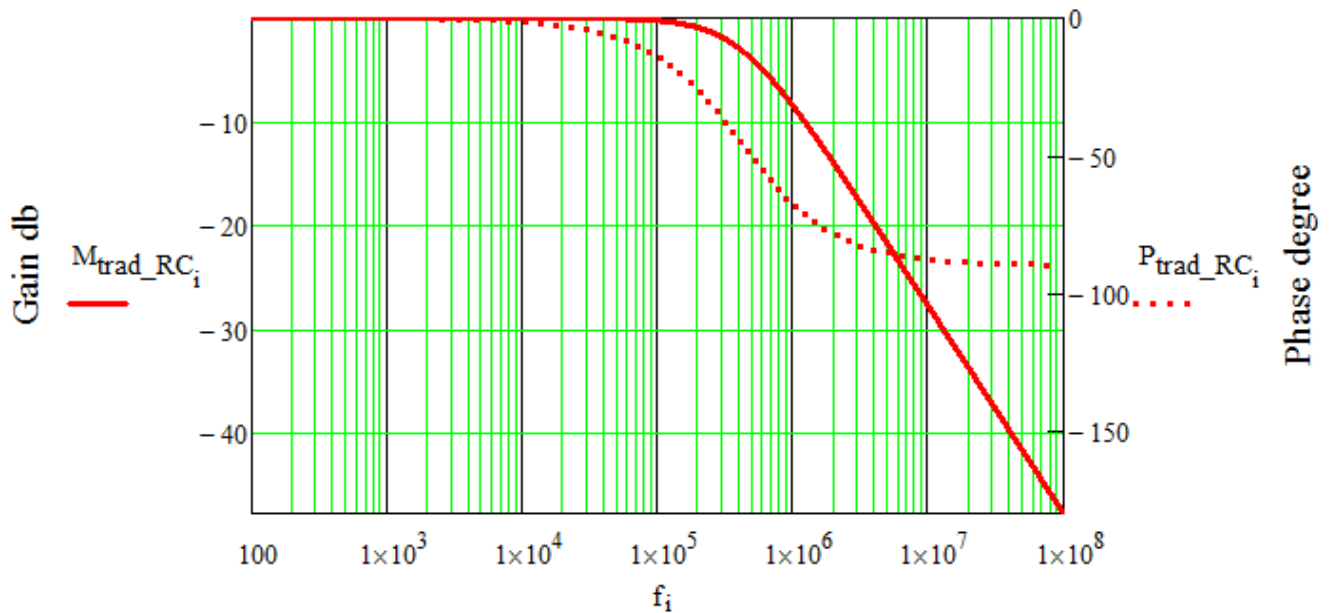


Figure 19. DC Gain vs Frequency Plot RC Filter

$$f = \frac{1}{2\pi R_1 C_1}$$

where

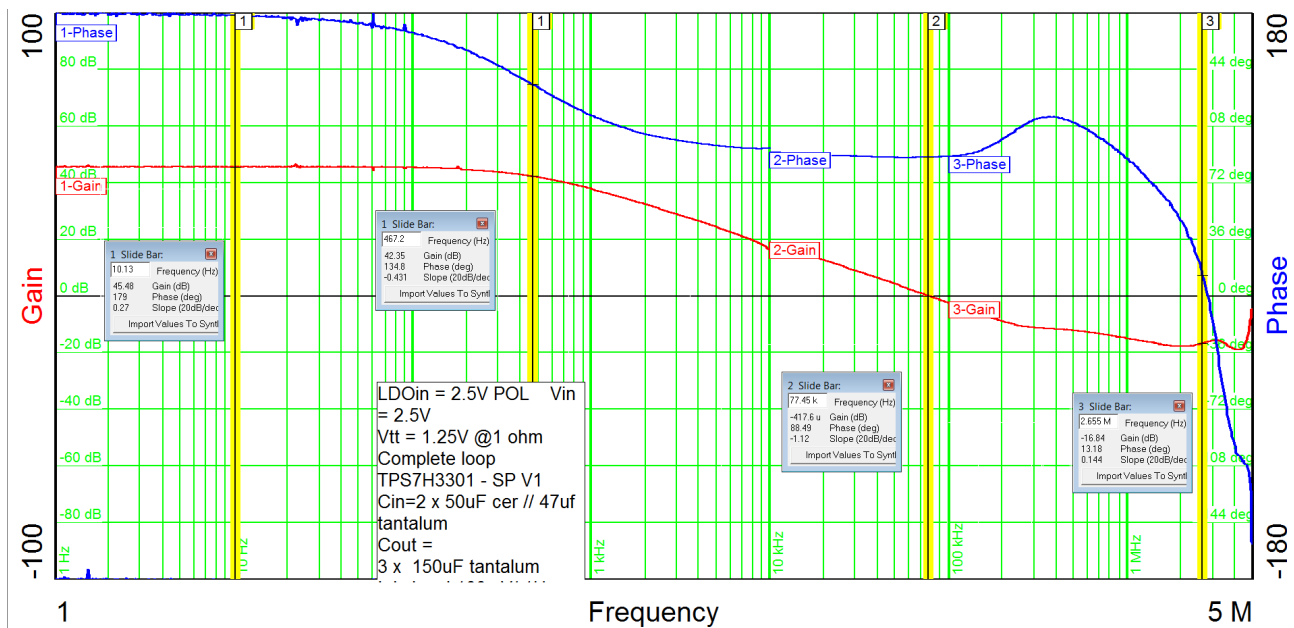
- $R_1 = 392 \Omega$
- $C_1 = 1000 \text{ pF}$

(10)

$$f = 406.008 \text{ kHz}$$

With introduction of added pole one can see a stable design with acceptable phase and gain margin, as shown in Figure 20.

DC gain = 45.48 dB,  $f_c = 77.45 \text{ kHz}$ , phase margin = 88.49°, Gain margin = 16.84 dB.



TPS7H3301-SP with transient board isolated / V2 isolated  
 $V_{DDQ} = 2.5\text{ V}$ ,  $R_L = 1\ \Omega$ , (1.25 A),  $V_{TT} = 1.25\text{ V}$   
 $V_{DDQSNS}$  isolated from  $V_{LDOIN}$

**Figure 20. Bode Plot of DDR Termination With Added Feedback Pole**

In summary, TPS7H3301-SP is a  $G_m$  driven source and sink DDR termination regulator. With thermally enhanced package that integrates low dropout (LDO) regulator that is capable of both sourcing and sinking current. Due to the simplicity of its design,  $G_m$  driven LDO is a single pole system and the output capacitance determines the unity gain bandwidth of the voltage loop. Thus, proper selection of output capacitors and its impedance is critical to ensure proper design performance.

## 9 References

- (1) Power Integrity – Steven M. Sandler pg. 123
- (2) DDR Memories Require Efficient Power Management Nazzareno Rossetti and Ron Lenk
- (3) Power supply solution for DDR bus termination by Robert Kollman, John Betten and Bang S. Lee
- (4) Powering DDR memory and SSTL – Peter James Miller, Texas Instruments [www.eetimes.com](http://www.eetimes.com) 05/24/2011



## Revision History

Changes from Original (December 2015) to A Revision	Page
• Corrected parameter symbol, $V_{DDQ}$ .....	2
• Removed duplicate paragraph .....	4
• Corrected the DDR application .....	6
• Corrected $V_{TT}$ value to match example and application name to DDR.....	6
• Corrected no load error to 6 mV .....	8

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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