Application Report
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TPS25831-Q1 Support Type-C VCONN Power Without Using LDO

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ABSTRACT

The USB Type-C™ receptacle, plug, and cable provide a smaller, thinner, and more robust solution to existing Standard and Micro USB cables and connectors, so it is widely used in the consumer and automotive markets today. The USB Type-C receptacle contains the VCONN pin. Once the connection between host and device is established, the CC pin (CC1 or CC2) in the receptacle that is not connected via the CC wire through the standard cable is repurposed to source VCONN to power circuits in the plug needed to implement Electronically Marked Cables. The TPS2583x-Q1 is a Type-C controller that supports all Type-C functions in a downstream facing port. It is also used to manage current advertisement and protection to a connected UFP and active cable. It can power the active cable through VCONN with the internal LDO, but the limitation is the current capability is only 5 mA, while the Type-C spec requires minimum 1 W power for sources with superspeed signals. Usually, one can use an external LDO to support the 1-W power (as described in TPS2583x-Q1 datasheet), but this method increases the solution cost. This report give a solution that shows how to support such an application without using the external LDO.

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1 Introduction

1.1 Limitations of Internal VCONN Power

The TPS2583x-Q1 integrates an internal LDO to generate VCC for control circuitry and MOSFET drivers. The nominal voltage for VCC is 5 V. VCONN is provided by the source to power cables through electronics in the plug. VCONN is provided over the CC pin that is not connected to the CC wire of the cable. If Ra is detected on the other CC pin (not connected to UFP), VCONN is applied to allow current to flow from the VCC to the CC pin connected to Ra. Figure 1 shows the internal structure of the VCONN power from the VCC. The bottleneck is that the VCC can provide just max 5 mA current to the VCONN. Under overload conditions, a precision current-limit circuit limits the VCONN output current. When a VCONN overload condition is present, the TPS2583x-Q1 maintains a constant output current, with the output voltage determined by (iOS_CCn x RLOAD). VCONN functionality is supported only with an external 5-V supply connected to the VCC. Failure to connect an external supply may cause the TPS2583x-Q1 VCC to reset. The device turns off when the junction temperature exceeds the thermal shutdown threshold (TSD) and remains off until the junction temperature cools approximately 20°C before restarting.

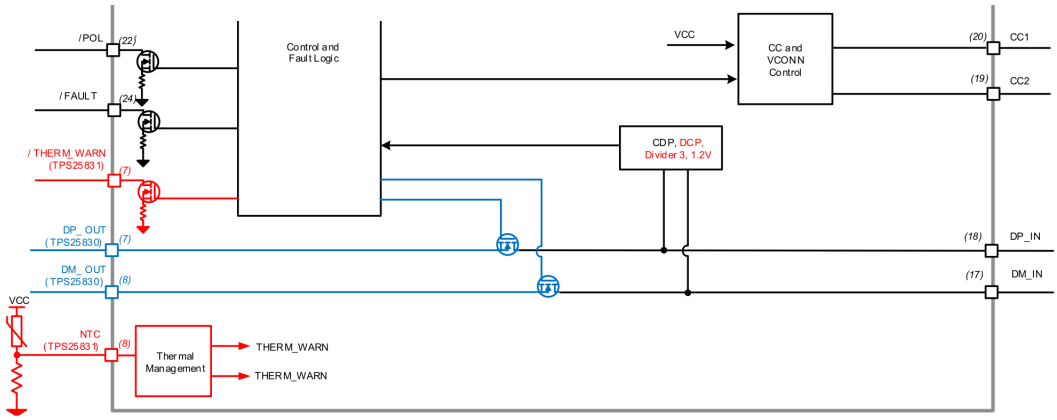

Figure 1. TPS2583x-Q1 VCONN Functional Block

1.2 Source VCONN Using External LDO

To solve the power limitation problem of the internal VCONN, the VCC pin can be over-driven with an external 5-V LDO capable of sourcing at least 300 mA in applications where higher VCONN power support is required. Figure 2 shows the typical application block for the external LDO power the VCONN. In this operating mode, the external LDO is the source for the buck low-side switch gate drive, as well as power to the internal VCONN mux. Note that, if using an external 5-V LDO for VCONN power, the following timing sequence is required. External VCONN power cannot be enabled before the TPS2583x-Q1 is enabled, so the external VCONN must be disabled before the TPS2583x-Q1 is disabled. In real applications, the customer can tie the EN of the external, 5 V LDO and EN of the TPS2583x-Q1 together to meet the timing requirement.

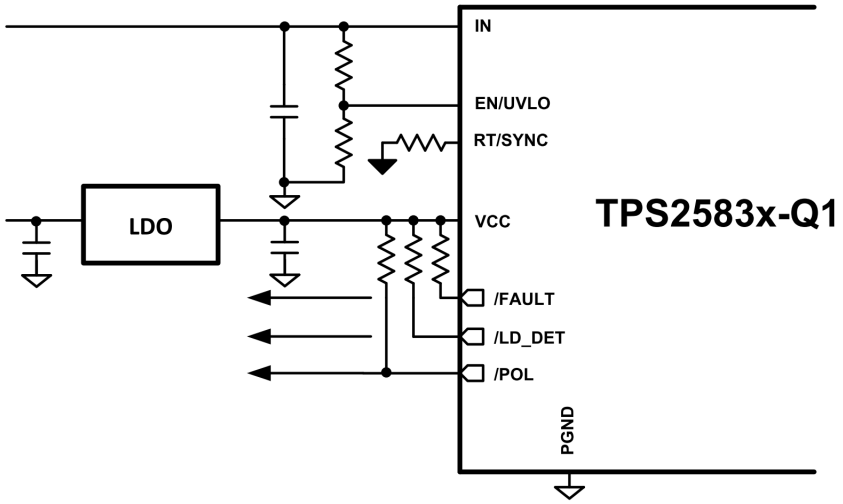

Figure 2. VCONN Source Using an External LDO

This solution can solve this problem, but it needs an external LDO and some capacitors. The following paragraph introduces a new solution that powers the VCONN through the TPS2583x-Q1 DC/DC converter output to save the BOM cost and minimize the solution size. This method needs an external P-FET, and uses the /LD_DET pin to control the ON/OFF of the device.

2 Power VCONN through TPS2583x-Q1 DC-DC output

2.1 Solution Overview

This solution uses the TPS2583x-Q1 DC/DC output to provide the power for VCONN. If no UFP connects to the Type-C port, the DC/DC output does not start up, so no VCONN power is needed. If the UFP connects to the Type-C port, since Rd is attached, the TPS25830-Q1 DC/DC converter starts up and provides 5.1 V default voltage at the OUT pin. This voltage can be used to source the VCONN if the UFP has a larger VCONN power requirement. Figure 3 shows the typical application block.

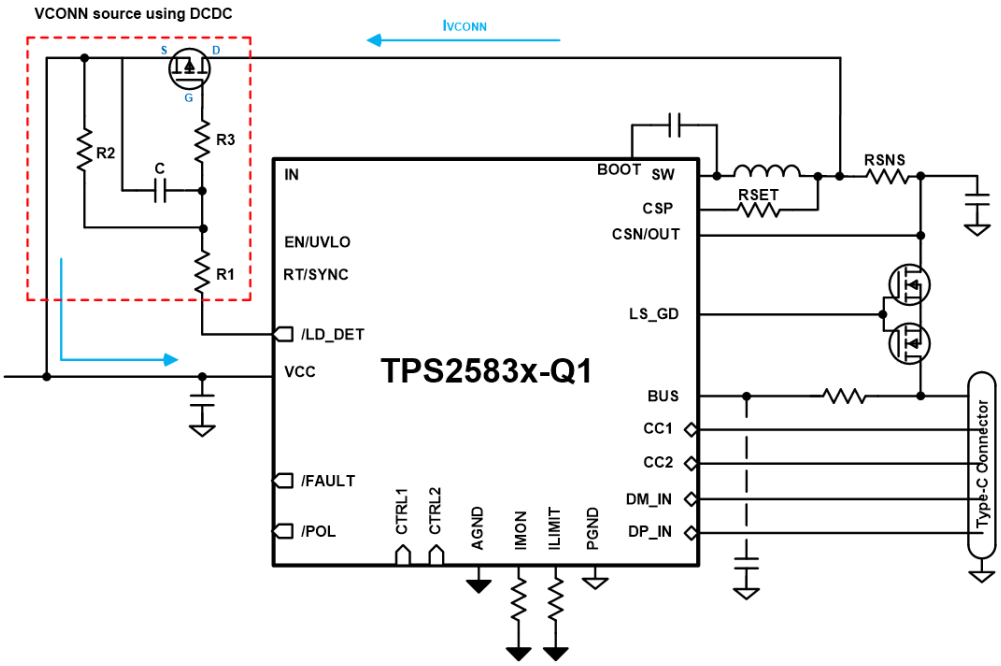

Figure 3. VCONN Sourcing Using the TPS2583x-Q1 DC/DC

2.2 Design Consideration

In this solution, the resistor R2 is used to guarantee the P-FET VGS = 0 V when the /LD_DET pin is not asserted. Make sure the P-FET is turned off, because if the PFET is not off before the DC/DC is working, the VCC charges the large caps on the TPS2583x-Q1 CSN/OUT pin. Since the VCC has very limited power capability, the VCC voltage is pulled below the UVLO threshold, and the TPS2583x-Q1 gets stuck in reset cycling. R3 can set what? as 0 Ω, but this resistor is optional and can be removed from the real design. R1 and C are very important for this solution, as they compose the RC delay circuit when the P-FET is intended to be turned on by /LD_DET.

If the R1 is too small, then when Rd is attached and after the deglitch time is asserted, the /LD_DET is asserted and pulled the P-FET gate to ground too early. The worst case is R1 = 0 Ω. Table 1 shows the /LD_DET assert timing the from TPS2583x-Q1 datasheet. The /LD_DET pin is pulled low within a max of 220 ms once Rd is attached.

Table 1. TPS2583x-Q1 /LD_DET Timing

PARAMETER		MIN	TYP	MAX	UNIT
tDEGLA	Asserting deglitch time	88	150	220	ms
tDEGLD	De-asserting deglitch time	7.0	12.7	19.4	ms

After this deglitch time, the /LD_DET is asserted, and the TPS2583x-Q1 DCDC starts up. The problem is after /LD_DET is asserted and the DC/DC start up, the CSN/OUT voltage needs time to ramp up to 5.1 V. So if the P-FET is turned on during that time, VCC voltage is higher than the CSN/OUT voltage (because the VCC voltage is at 5 V already, but the DCDC OUT is not ramped up to 5 V yet), so the VCC LDO charges the DC/DC output caps. This results in the VCC entering hiccup mode due to the large charging current, and TPS2583x-Q1 cannot start up normally. Figure 4 shows the VCC hiccup and reset under the condition R1 = R3 = 0 Ω, R2 = 100 KΩ, C = 470 nF.

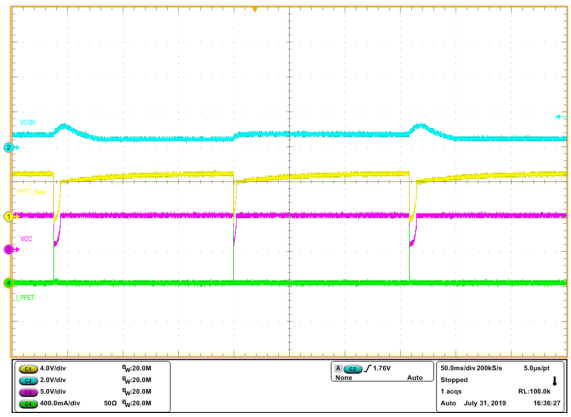

Figure 4. VCC Hiccup, CH1 = V_GATE, CH3 =VCC

Note that, in this application, the P-FET must be connected before the RSNS resistor. If connecting P-FET to the CSN/OUT pin (after the RSNS resistor), then the VCONN current is accounted for in the current limit calculation.

Another thing to pay attention to is the Type-C timing for VCONN power. Table 2 provides the timing values that are met when delivering power over VBUS and VCONN.

Table 2. VBUS and VCONN Timing Parameters

	Minimum	Maximum	Description
tVBUSON	0 ms	275 ms	From entry to the attached.SRC until the VBUS reaches the minimum vSafe 5 V threshold as measured at the receptacle of the source.
tVBUSOFF	0 ms	650 ms	From the time the sink is detached until the source removes VBUS and reaches vSafe 0 V
tVCONNON	Note 1	2 ms	From the time the source supplies the VBUS in the attached.SRC state. Measured from vSafe 5 V to the minimum VCONN voltage
tVCONNOFF	0 ms	35 ms	From the time that a sink is detached, or as directed, until the VCONN supply is disconnected

Note 1. VCONN may be applied prior to the application of VBUS

According to Table 2, the VCONN needs to be present within a maximum of 2 ms after the TPS2583x-Q1 VBUS is valid. So the P-FET turn-on time needs to be designed carefully.

A good design decision is to enable the P-FET quickly, once theTPS2583x-Q1 DC/DC output voltage is ramped up to the nominal value. As seen in Table 3, this DC/DC ramp-up time can refers to the internal soft-start time from the TPS2583x-Q1 datasheet:

Table 3. TPS2583x-Q1 Buck Regulator Soft-Start Timing

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TSS	Internal soft-start time	Internal reference time increases from 0 V to 1.0 V	3	5	7	ms

So the P-FET must be turned on with a T_{SS} delay time after the /LD_DET is asserted, since the MOSFET turn-on speed is very fast. Therefore, it can guarantee the VCONN turn on synchronizes with the DC/DC output (VBUS) voltage. With this special PFET turn-on timing design, this solution can prevent the VCC from charging the TPS2583x-Q1 output capacitor. It also does not delay VCONN power too much when the VBUS is valid in order to meet the maximum 2 ms VCONN delay timing restriction from the USB Type-C specification.

3 R, C Selection

3.1 R, C calculation

For this solution, R3 does not affect the P-FET turn on time, and only the R1 and C value need to be determined. The R1 and C can be determined by following the guidelines from the analysis discussed in the previous paragraphs:

- P-FET must be turned on after T_{SS}
- P-FET V_{GS} needs to ramp up to the P-FET V_{TH} threshold at T_{SS}

Here, T_{SS} is the TPS2583x-Q1 BUCK regulator typical soft-start timing; V_{GS} is the voltage across the P-FET GATE and SOURCE; V_{TH} is the P-FET Gate-Source typical threshold voltage.

For the application block in Figure 3, the GATE voltage of the P-FET can be deduced with the following formulas (assume R3 = 0 Ω):

(1) $U_C + U_{R1} = VCC$;

(2) $U_{R2} = U_C$;

(3) $I_C = C * (dU_c / dt)$;

(4) $I_{R2} = U_{R2} / R2$;

(5) $I_{R1} = I_C + I_{R2}$;

(6) $V_{GATE} = R1 * I_{R1}$;

Above are the linear, first-order, inhomogeneous differential equations, and the solution for V_{GATE} is:

$$V_{GATE} = \frac{R1}{R1 + R2} * VCC + \frac{R2}{R1 + R2} * VCC * e^{-\frac{(R1+R2)*t}{R1*R2*C}}$$

For this equation, t is the TPS2583x-Q1 soft-start time, and V_{GATE} is the P-FET GATE voltage during the DC/DC soft start. As previously described, it needs P-FET V_{GS} (V_{GATE} -VCC) voltage to achieve the V_{TH} when TPS2583x-Q1 finishes the soft-start. If choosing the C and R2 value first, then with these conditions, R1 can be deduced with the previously discussed equation.

3.2 Design Example

In this solution, assume the R2 is 100 KΩ, and choose C as 470 nF, the R1 value can be determined based on the given R2 and C value.

The VCC is the TPS2583x-Q1 VCC output voltage, the typical value is 5 V; t is the soft-start time, and the typical value is 5 ms. Take the Si2309CDS, for example. Table 4 shows the V_{TH} characteristic for this P-FET:

Table 4. Si2309CDS VGS(th) Spec

PARAMETER		Test Condition	MIN	MAX	UNIT
Gate-Source Threshold Voltage	VGS(th)	VDS = VGS, ID =-250 uA	-1	-3	V

It does not give the Gate-Source typical value, while it can measured by deducing it. According to the Figure 5, the P-FET is turned on when gate voltage (V_{GATE}) is 3.54 V (as long as the source voltage V_S (VCC) is 5 V). Therefore, the typical V_{TH} value is -1.46V.

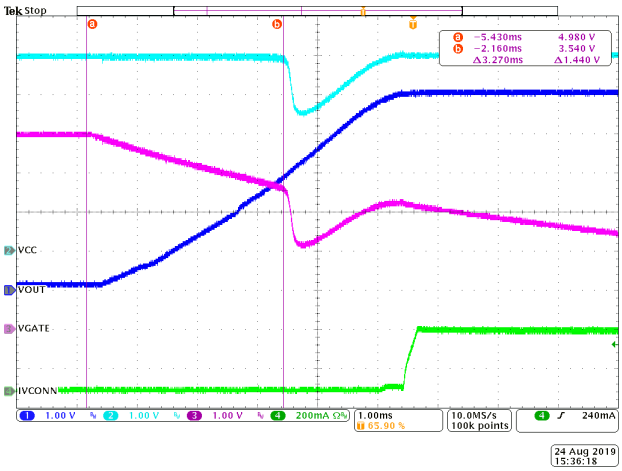

Figure 5. PFET Si2309CDS V_{GS}

The conditions are summarized as follows:

R2 = 100 KΩ, C = 470 nF, VCC = 5 V, V_{GATE}= 3.54 V, t = 5 ms.

The resistor R1 value can be calculated with above equation, resulting in an R1 approximate value of 30 KΩ.

4 The Performance of VCONN Sourcing by the P-FET

The following testing is based on the R and C parameters calculated previously. This testing uses an E-Load to simulate the 300 mA VCONN sink. Figure 6 shows that the TPS2583x-Q1 can start up normally, the VCC is flat with no voltage drop, and the CCx can source a 300 mA current. Figure 7 shows the VCC voltage is 5 V during the start up, and soft-start time is 5 ms.

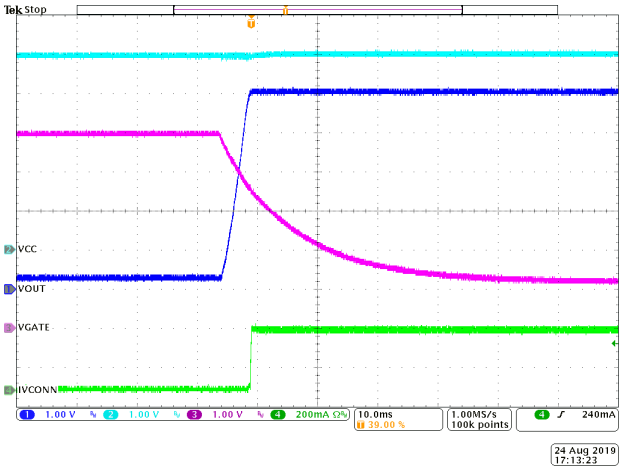

Figure 6. VCONN Sourcing Through an External P-FET

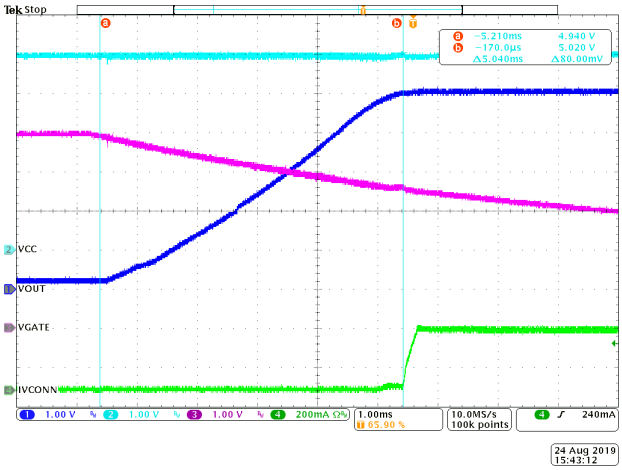

Figure 7. VCONN Sourcing Through an External P-FET

5 Limitations of the Solution

In this solution, the VCC connects to the TPS2583x-Q1 DC/DC output through the external P-FET. Since the TPS2583x-Q1 has the cable compensation function, the DC/DC output voltage rises along with the increased loading at the USB port. The maximum cable compensation voltage is 1.8 V per the TPS2583x-Q1 datasheet, so the VCC pin faces high-voltage when the cable compensation function is enabled. The risk is that the CSN voltage may be compensated too high, and beyond the VCC voltage rating shown in Table 5:

Table 5. TPS2583x-Q1 VCC Absolute Maximum Rating

PARAMETER		MIN	MAX	UNIT
Output Voltage	VCC to AGND	-0.3	6	V

So, the TPS2583x-Q1 cable compensation voltage must be designed below 0.9 V at the maximum load to guarantee the applied voltage on the VCC pin is limited below the VCC safety voltage range.

Another limitation is the short-to-battery protection function. If the VBUS shorts to battery, the TPS2583x-Q1 OUT/CSN voltage can be as high as 18 V, so the VCC faces this high voltage because it connects to the TPS2583x-Q1 output. Therefore, this solution cannot support BUS short-to-battery protection.

6 Conclusions

VCONN sourcing using the TPS2583x-Q1 DC/DC is good solution if the application faces BOM cost pressure. This solution can help save the external LDO, but it cannot support BUS short-to-battery protection. The cable compensation voltage must also be limited, as some applications require higher cable compensation voltage due to the long cable.

7 References

1. Texas Instruments, *TPS2583x-Q1, USB Type-C and BC1.2 5-V 3.5-A Output, 36-V Input Synchronous Step-Down DC/DC Regulator with Cable Compensation Data Sheet*
2. *Universal Serial Bus Type-C Cable and Connector Specification*

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