Application Note

Intro to Multi-function Pins and their Applications in TI Step-down Converters

Stefano Panaro

ABSTRACT

Today, more and more engineers are asking for smaller components when designing their systems. This application report explains the Multi-function pin present in some of TI step-down converters (VSET/VID for TPS62864/6/8/9, VSET/MODE for TPS62865/7 and TPSM82864/6A and VSEL/MODE for TPS62800/1/2/6/7/8). Several applications can benefit from the Multi-function pins; they enable the engineers to introduce additional features into their design while assuring a minimal solution size.

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1 Introduction

Today, more and more engineers are asking for smaller components when designing their systems.

Smaller parts lead to a reduced board size, with the benefit of space critical applications (wearables, personal electronics, and so on) and reducing the cost.

Also, more devices can be incorporated on the same boards, leading to an increased complexity and additional capabilities per board area.

In the past, power managements DC-DC Buck ICs had an independent pin for every function, as power good, output voltage setting, mode of operation, and so on.

This limitation led to an intrinsic tradeoff; for space critical applications, the designer had to choose the simplest component, without any additional features, to assure the smallest package possible. For more complex designs, where more features are required, the only choice were bulky components with a big package and an elevated number of pins.

To overcome this tradeoff, Multi-function pins were introduced. A Multi-function pin is simply a single pin where more than one features are integrated.

This application note considers the TPS6280x, TPS6286x and TPSM8286xA family, that are capable of offering many features in a small size package.

With this intent, an input pin is multiplexed to provide two different functions (VSET/VID for TPS62864/6/8/9, VSET/MODE for TPS62865/7 and TPSM82864/6A and VSEL/MODE for TPS62800/1/2/6/7/8), usually separated in time domain as shown in Figure 1-1.

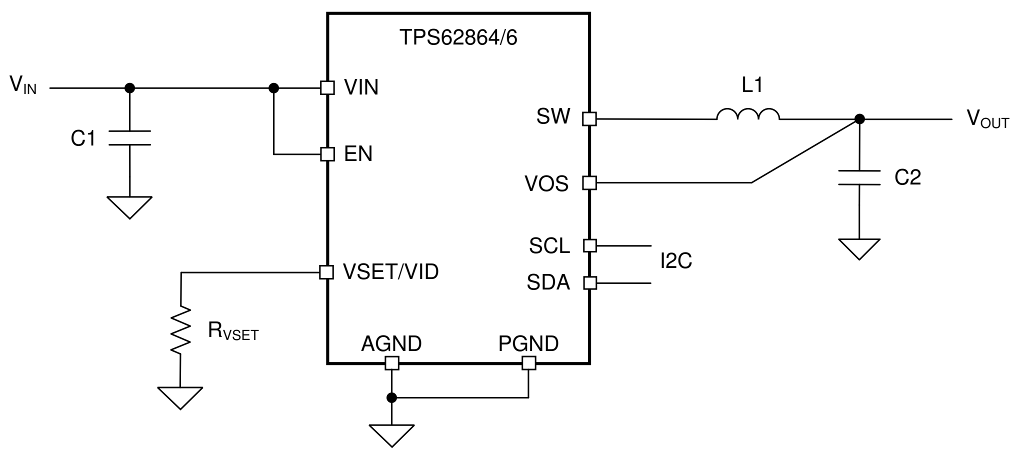

Figure 1-1. TPS62864/6 Typical Application Schematics

At the beginning, directly after enabling the startup (t_startup_delay), the ICs use the multiplexed pin for resistance measurement (R2D conversion, see Benefits of a Resistor-to-Digital Converter in Ultra-Low Power Supplies for reference), where the result allows to correctly set the output voltage value. During operation, the pin acts as a digital input as shown in Figure 1-2, to correctly configure the corresponding setting.

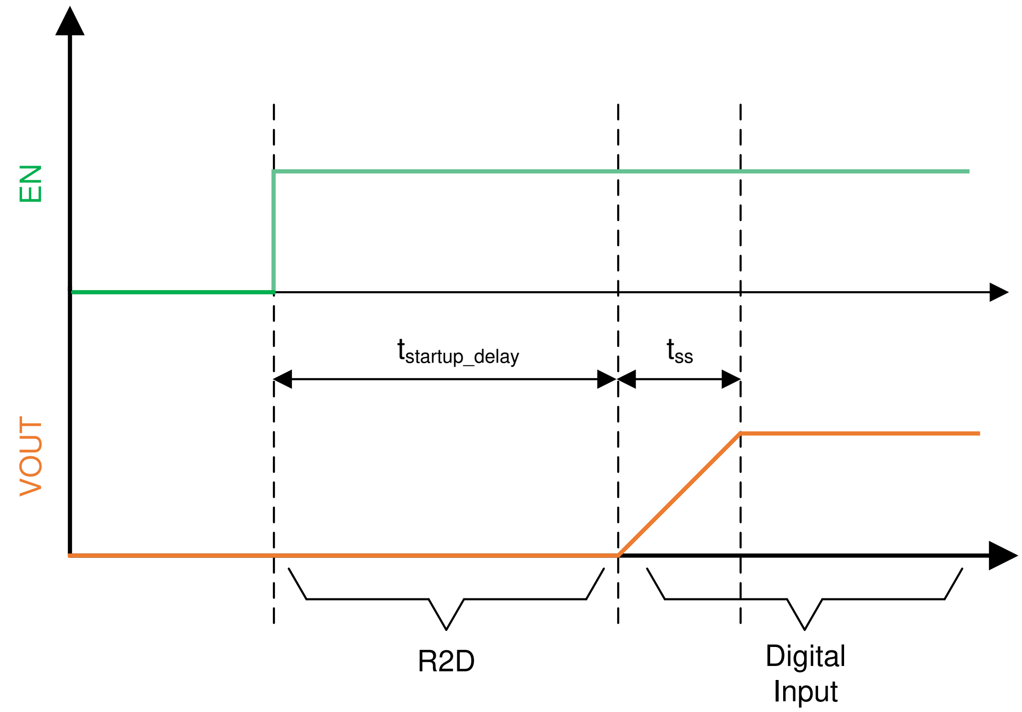

Figure 1-2. VSET/MODE Pin Time Multiplexing

This application note describes the Multi-function pin behavior and it proposes some driving circuitry to effectively multiplex between the different features while avoiding measurement errors.

2 Standard Device Operation: Resistance Measurement and Digital Input

During t_startup_delay, the IC needs to perform a resistance measurement on the Multi-function pin.

The resistance measurement is done by injecting a small current I_{MEAS} in the external resistor R_{VSET}, and reading the correspondent voltage V_{MEAS} as shown in Figure 2-1 The value of R_{VSET} can be computed as: $R_{VSET} = V_{MEAS} / I_{MEAS}$;

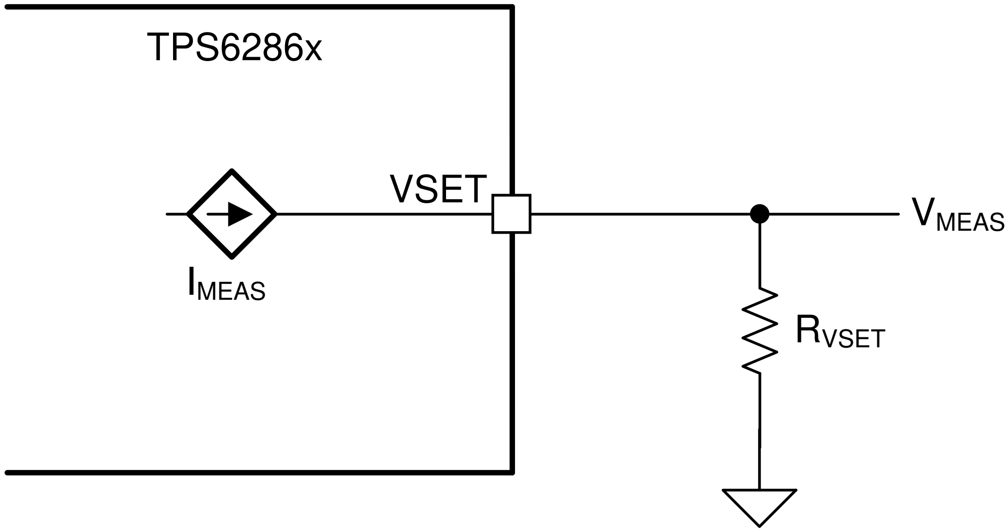

Figure 2-1. R2D Conversion on VSET Pin

This operation has to be as precise as possible, since any measurement errors could cause an erroneous output voltage setting, with possible damages to the load.

For example, referring to TPS62864/6 2.4-V to 5.5-V Input, 4-A and 6-A Synchronous Step-Down Converter with I2C Interface in WCSP Package data sheet: *The R2D converter has an internal current source which applies current through the external resistor, and an internal ADC which reads back the resulting voltage level. Depending on the level, the correct start-up output voltage and I2C slave address are set.... Ensure that there is no additional current path or capacitance greater than 30 pF from this pin to GND during R2D conversion. Otherwise a false value is set.*

The previous limits must to be considered when designing the driving circuit.

The capacitance limit is expressly given in the data sheet, whereas the maximum additional current is not specifically defined. In most cases it is okay to consider *40nA* as maximum additional current.

3 TPS62864/6/8/9: VSET/VID Pin

As previously described, VSET/VID pin is used as startup to correctly set the output voltage and the I2C address of the device. During operation, the pin can be used to select the VOUT registers for the output voltage (Low = VOUT register 1; high = VOUT register 2) (TPS62868x 2.4-V to 5.5-V Input, 4-A/6-A Synchronous Step-Down Converter with I2C Interface in QFN Package data sheet and TPS62864/6 2.4-V to 5.5-V Input, 4-A and 6-A Synchronous Step-Down Converter with I2C Interface in WCSP Package data sheet).

If the designer wants to set VSET/VID pin to a low level, then the standard configuration can be adopted as shown in Figure 3-1: it is sufficient to place a resistor connected to ground. During t_startup_delay, the R2D conversion can be performed without additional parasitics and during operation it pulls down the pin to GND.

Instead, if the designer wants to set VSET/VID pin to High level, they need to put in parallel to the resistor a driving circuit to properly drive the input.

The preferred solution is to use an external digital circuit (for example, an FPGA or an MCU) to correctly drive the pin during operation, as shown in Figure 3-1.

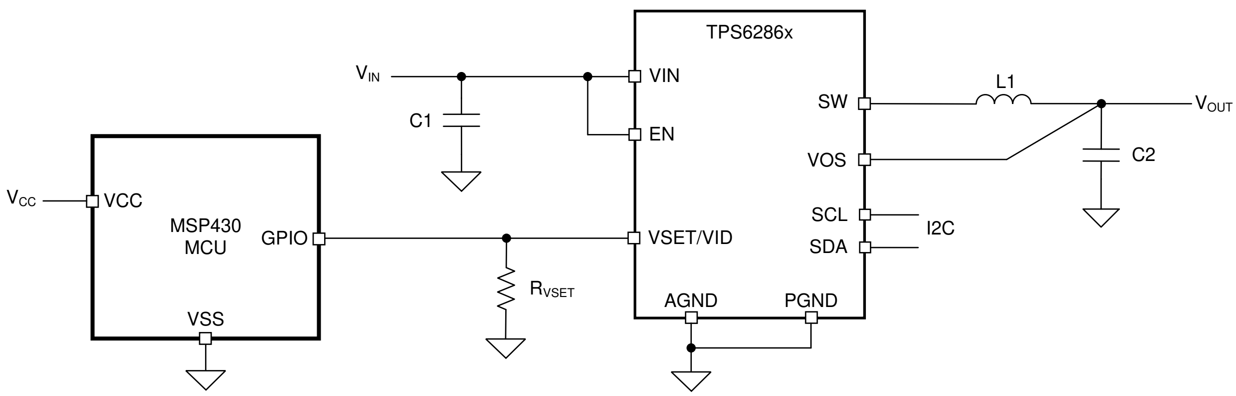

Figure 3-1. Typical Application Schematics, VSET/VID Driving Circuit with MCU

At startup the GPIO should be in high impedance state: VSET/VID pin sees only the resistor (plus GPIO parasitics) that sets the correct output voltage. After the startup phase, the designer can decide to pull the pin high or low according to the preferred operation changing the GPIO state (the polarization of the pin can also be switched during run time to adapt to any particular necessity).

The designer is only required to assure that the GPIO parasitics are lower than the maximum ones, as specified in section Section 2.

For example, the MSP430FR2000 data sheet specified a High-impedance leakage current of 20nA and an input capacitance of 5pF, compliant with the above specifications.

Table 3-1. Digital Inputs

Parameter		Test Conditions	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		2 V	0.90		1.50	V
			3 V	1.35		2.25	
V_{IT-}	Negative-going input threshold voltage		2 V	0.50		1.10	V
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis ($V_{IT+} – V_{IT-}$)		2 V	0.3		0.8	V
			3 V	0.4		1.2	
R_{Pull}	Pullup or pulldown resistor	For pullup: $V_{IN} = V_{SS}$ For pulldown: $V_{IN} = V_{CC}$		20	35	50	kΩ
$C_{I,dig}$	Input capacitance, digital only port pins	$V_{IN} = V_{SS}$ or V_{CC}			3		pF
$C_{I,ana}$	Input capacitance, port pins with shared analog functions	$V_{IN} = V_{SS}$ or V_{CC}			5		pF
$I_{lkg(Px.y)}$	High-impedance leakage current		2 V, 3 V	–20		+20	nA
$t_{(int)}$	External interrupt timing (external trigger pulse duration to set interrupt flag)	Ports with interrupt capability (see block diagram and terminal function descriptions)	2 V, 3 V	50			ns

4 TPS62800/1/2/6/7/8: VSEL/MODE Pin

VSEL/MODE pin has a similar structure to VSET/VID pin, but it is used for a different setting. During t_startup_delay, RVSEL resistance set the output voltage value, whereas during operation the pin allows to enable either forced-PWM mode (connect it to a high level) or Power-Save Mode (connect it to a low level) (TPS6280x 1.8-V to 5.5-V, 0.6A / 1-A, 2.3-µA IQ Step Down Converter 6-Pin, 0.35-mm Pitch WCSP Package data sheet).

The same considerations made for VSET/VID pin are still valid. If the designer wants to run the device in PSM, the standard configuration can be adopted as shown in Figure 4-1: it is sufficient to place a resistor connected to ground. During t_startup_delay, the R2D conversion can be performed without additional parasitics and during operation it pulls down the pin to GND.

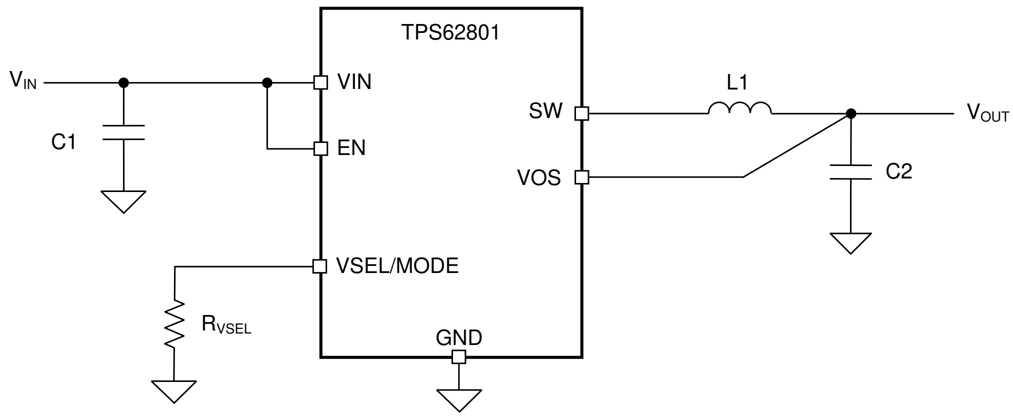

Figure 4-1. TPS62801 Typical Application Schematics

Instead, if the designer wants to set VSEL/MODE pin to High level (forced-PWM operation), they need to put in parallel to the resistor a driving circuit to properly drive the input.

The preferred solution is to also use an external digital circuit (for example, an FPGA or an MCU) to correctly drive the pin during operation as shown in Figure 4-2. As before, the designer needs to assure that the GPIO parasitics are lower than the maximum ones, as specified in section Section 2.

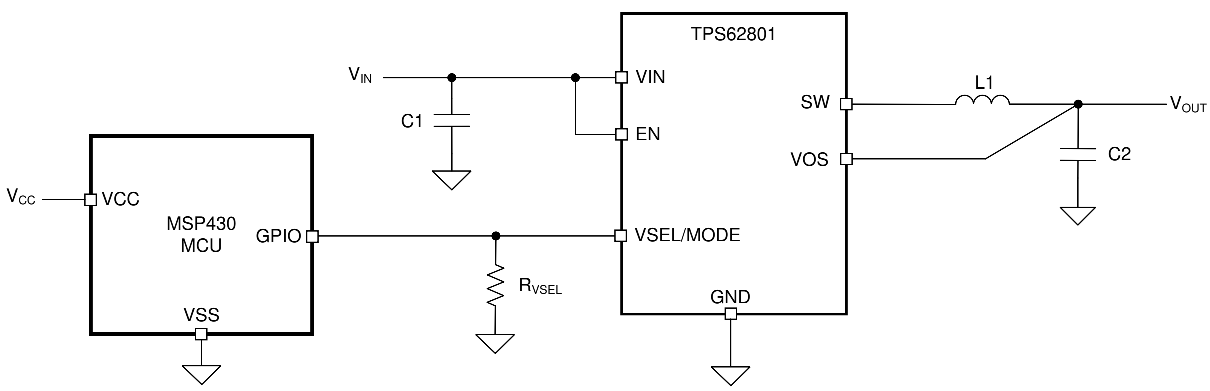

Figure 4-2. Typical Application Schematics, VSEL/MODE Driving Circuit with MCU

5 TPS62865/7 and TPSM82864/6A: VSET/MODE Pin

TPS62865/7 and TPSM82864/6A ICs have the VSET/MODE pin, that is functionally equivalent to the previously described VSEL/MODE pin (TPS62865/TPS62867 2.4-V to 5.5-V Input, 4-A and 6-A Synchronous Step-Down Converter in 1.5-mm × 2.5-mm QFN Package and TPSM82864A/TPSM82866A 2.4-V to 5.5-V Input, 4-A/6-A Step-Down Power Module with an Integrated Inductor in a 3.5-mm × 4.0-mm Thin Overmolded QFN Package data sheets).

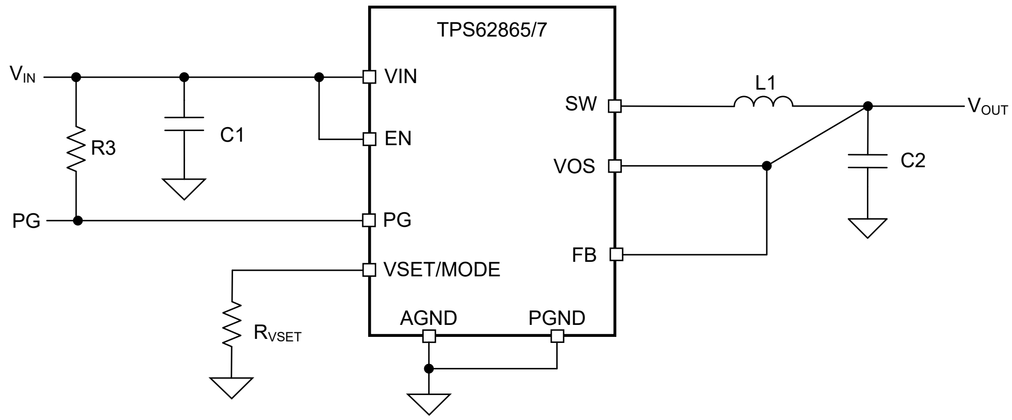

Figure 5-1. Typical Application Schematics TPS62865/7 – Fixed Output Voltage

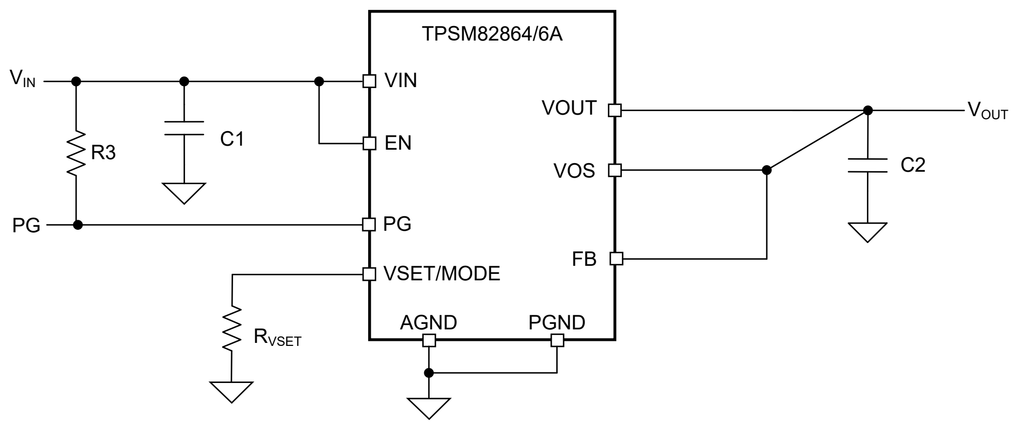

Figure 5-2. Typical Application Schematic TPSM82864/6A - Fixed Output Voltage

The main difference with respect to the previous devices is that here an additional pin (FB) is present. The FB pin can to be used to properly select the output voltage with the classical feedback divider when VSET/MODE pin is connected to a logic high or logic low level.

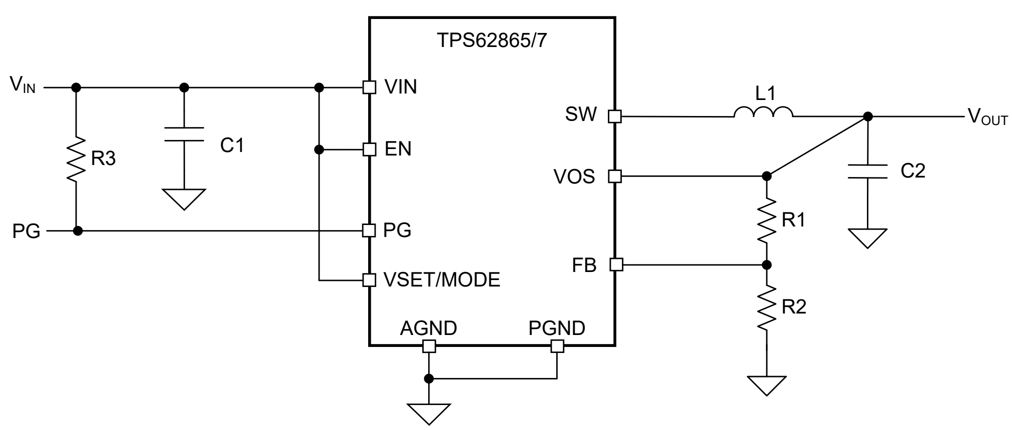

Figure 5-3. Typical Application Schematics TPS62865/7 – Forced PWM Operation

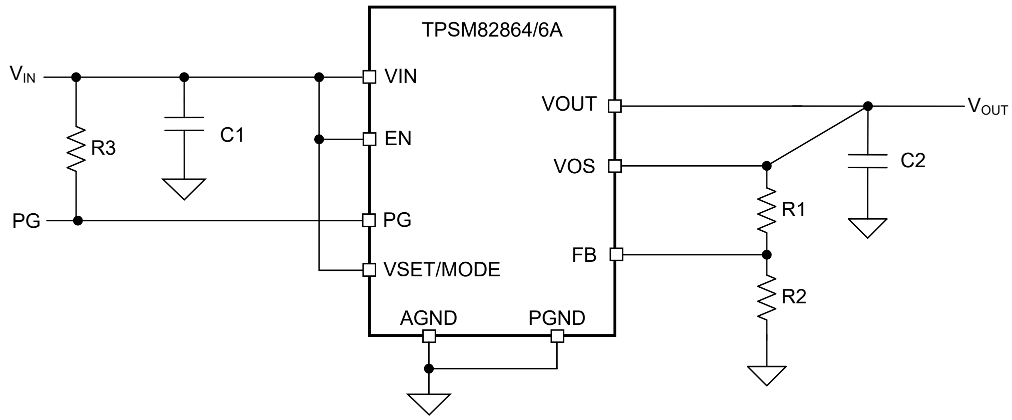

Figure 5-4. Typical Application Schematics TPSM82864/6A – Forced PWM Operation

With these devices, the simplest solution to select the forced-PWM mode is to connect the VSET/MODE pin to high potential and then use the FB divider to properly select the output voltage as shown in Figure 5-3 and Figure 5-4.

The main advantage of the last configuration is the possibility to decouple VSET and MODE functionality, giving the possibility to the designer to effectively select the mode of operation without limiting the output voltage level selection. With this solution, no additional components are required and no parasitics are introduced, leading to a simple and straightforward design process.

6 Summary

Table 6-1 includes the summary of the described ICs and the preferred solutions to achieve the pin's secondary function. Achieving this second function is not required in some applications.

Table 6-1. Summary Table

Device	Preferred Solution
TPS62864/6 and TPS62868/9 (VSET/VID)	GPIO driving to achieve VID function (see Section 3): VSET/VID = LOW → HIGH
TPS62800/1/2/6/7/8 (VSEL/MODE)	GPIO driving to achieve MODE function (see Section 4): VSEL/MODE = LOW → HIGH
TPS62865/7 (VSET/MODE)	VSET/MODE = HIGH to achieve forced PWM Use FB resistor divider (see Section 5)
TPSM82864/6A (VSET/MODE)	VSET/MODE = HIGH to achieve forced PWM Use FB resistor divider (see Section 5)
TPS62901/2/3 (MODE/S-CONF)	MODE/S-CONF = HIGH to achieve forced PWM Use FB resistor divider (same implementation as section Section 5)

Looking at the TI portfolio, the use of Multi-function Pins is not limited to the selection of the operationg mode (PFM/PWM or forced PWM), but it has been used for a wide variety of features.

Table 6-2 reports some of the other TI Buck Converters with Multi-function Pins.

Table 6-2. Other TI Buck Converters with Multi-function Pins

Device	Multi-function Pins
TPS62810/1/2/3/6-Q1	• MODE/SYNC: PFM/PWM (LOW), forced PWM (HIGH); the pin can be used to synchronize to an external frequency. • COMP/FSET: a resistor defines the compensation of the control loop as well as the switching frequency if not externally synchronized.
TPSM82810/3	• MODE/SYNC: PFM/PWM (LOW), forced PWM (HIGH); the pin can be used to synchronize to an external frequency. • COMP/FSET: a resistor defines the compensation of the control loop as well as the switching frequency if not externally synchronized.
TPS62912/3	• EN/SYNC: Disable (LOW), Enable (HIGH); the pin can be used to synchronize to an external frequency. • S-CONF: the pin is used to select switching frequency, spread spectrum, output discharge and synchronization range.

7 Revision History

Changes from Revision * (July 2021) to Revision A (November 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added *TPSM82864/6A*	1
• Added *Typical Application Schematics TPS62865/7 – Forced PWM Operation* image	8
• Added *Typical Application Schematic TPSM82864/6A – Forced PWM Operation* image	8
• Added *TPSM82864/6A (VSET/MODE)* to table	10

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