TEXAS INSTRUMENTS

APPLICATION NOTE

GC2011-AN9804

Upconverting Signals With The GC2011 For Easier Digital To Analog Conversion

December 20, 1998

Revision 0.0

This application note describes how signals sampled at a rate of F_{in} and centered from 0 to $F_{in}/2$ can be upconverted to be centered from $F_{in}/4$ to $3F_{in}/4$ and output to a digital to analog converter (DAC) at a sample rate of $2F_{in}$. This simplifies the analog upconversion of the signal to a higher IF frequency. For example, the output signal from a GC4114 transmitter chip operating at a 60 MHz clock rate, might center its data from 2.5 to 27.5 MHz. This application note describes how the GC2011 chip can be used to move the signal up by 15MHz so that it is centered from 17.5 to 42.5 MHz and sent to a DAC operating at 120 MHz. The DAC output can be filtered by a lowpass filter, mixed up by 110MHz to be centered at 140 MHz, and bandpass filtered. Without the GC2011 chip the lowpass and bandpass filters would have to have 5 MHz transition bands (a roll off from 0dB to -60dB within 5MHz). With the GC2011 chip the transition band is relaxed to an easily achieved 35 MHz.

1.0 Theory

An input signal to the GC2011 at a sample rate of F_{in} can be up-converted by $F_{in}/4$, and output at twice the rate for input to a digital to analog converter (DAC). The processing flow is illustrated in Figure 1.

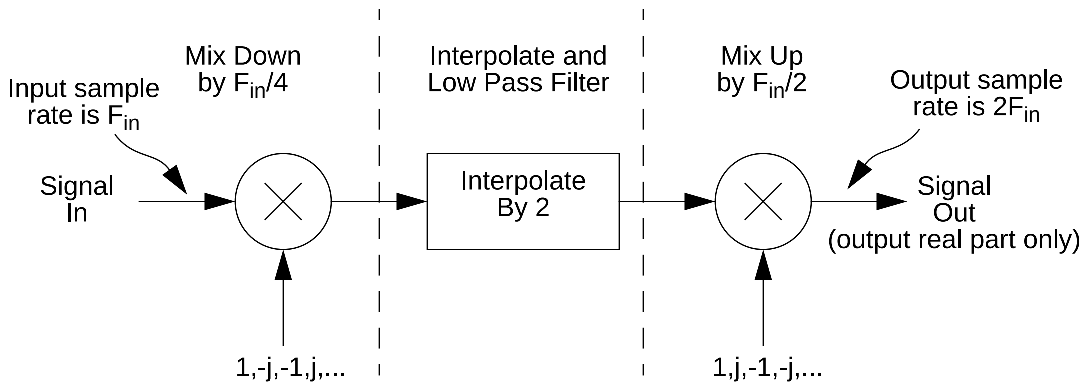

Figure 1. Up-conversion and Interpolation

The signal processing performed in Figure 1 is shown in Figure 2:

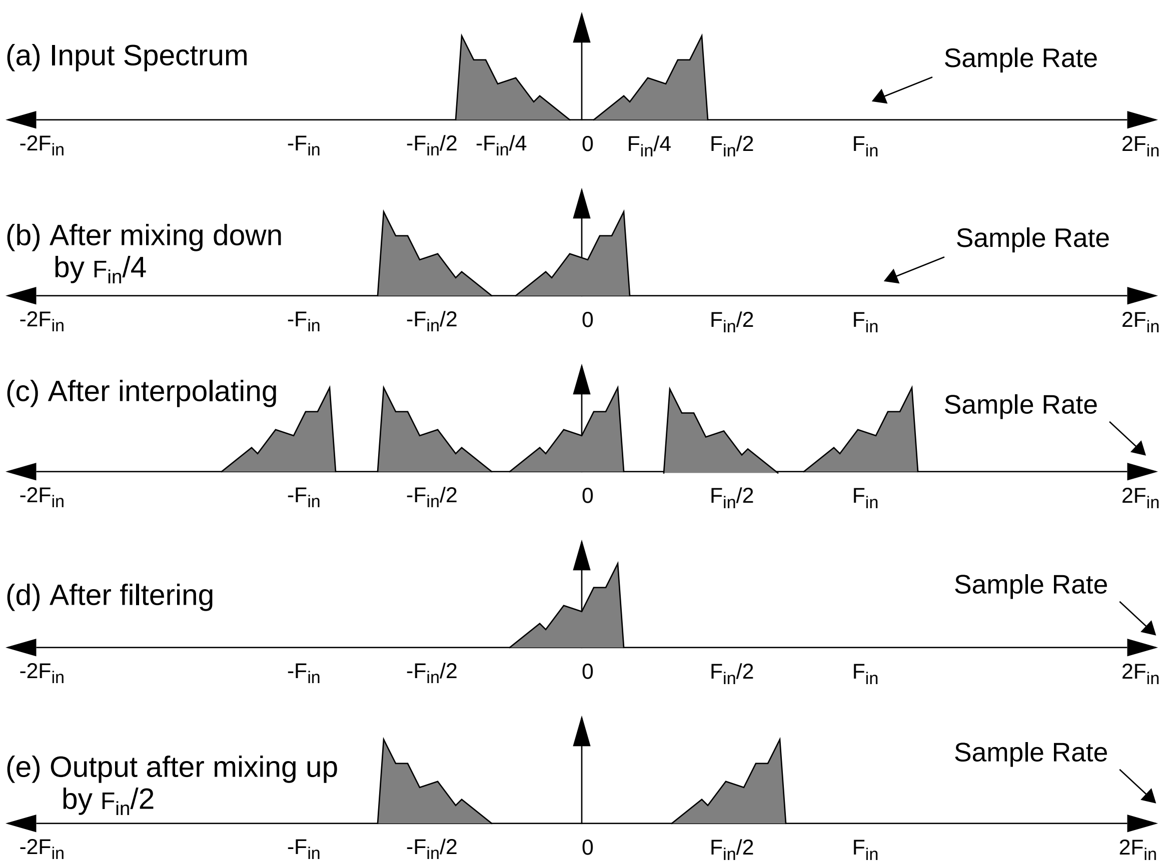

Figure 2. Signal Processing

Figure 2a shows the input spectrum with the signal centered between 0 and $F_{in}/2$. Figure 2b shows the spectrum after it is mixed down by $F_{in}/4$ so that it is centered between $-F_{in}/4$ and $+F_{in}/4$. Figure 2c shows the spectrum after doubling the sample rate by inserting zeroes between each sample. Figure 2d shows the spectrum after low pass filtering the interpolated data. Figure 2e shows the final output after mixing up by $F_{in}/2$. The output is the real half of the complex mixer's output.

Figure 2e shows that the end result of the manipulations is that the input sample rate has been doubled and the input signal's spectrum has been moved up in frequency by $F_{in}/4$.

2.0 Suggested GC2011 Circuit

The manipulations described in Figures 1 and 2 can be done with a single GC2011 Digital Filter chip, a multiplexor, three high speed registers and a clock doubler as shown in Figure 3. The GC2011 accepts the data and clock at sample rates (F_{in}) up to 80 MHz. The chip performs the upconversion by $F_{in}/4$ and doubles the sample rate of the data. The double rate data is clocked out of the GC2011 chip in pairs of samples at the F_{in} clock rate. The even time samples are output on the Aout pins and the odd time samples are output on the Bout pins. The multiplexor sends the Aout bits to the digital to analog converter (DAC) when the clock is high and sends the Bout bits when the clock is low. The high speed registers are used to meet the timing requirements of the output rate which can be up to 160 MHz. The worst case timing delay path is from the two 12 bit registers through the multiplexors and into another 12 bit registers. The delay through this path must be less than the clock period of the CK_2X clock. At 160 MHz, the clock period is 8.3 nsecs. The register-multiplexor-register structure can be imbedded in a high speed programmable device (PLD or FPGA), or built using 74FCT374C octal registers from IDT (www.idt.com) and QS3357 quick switch multiplexors from Quality Semiconductor (www.qualitysemi.com). Appropriate clock doublers are available from IDT (CSP2509) or Quality Semiconductor.

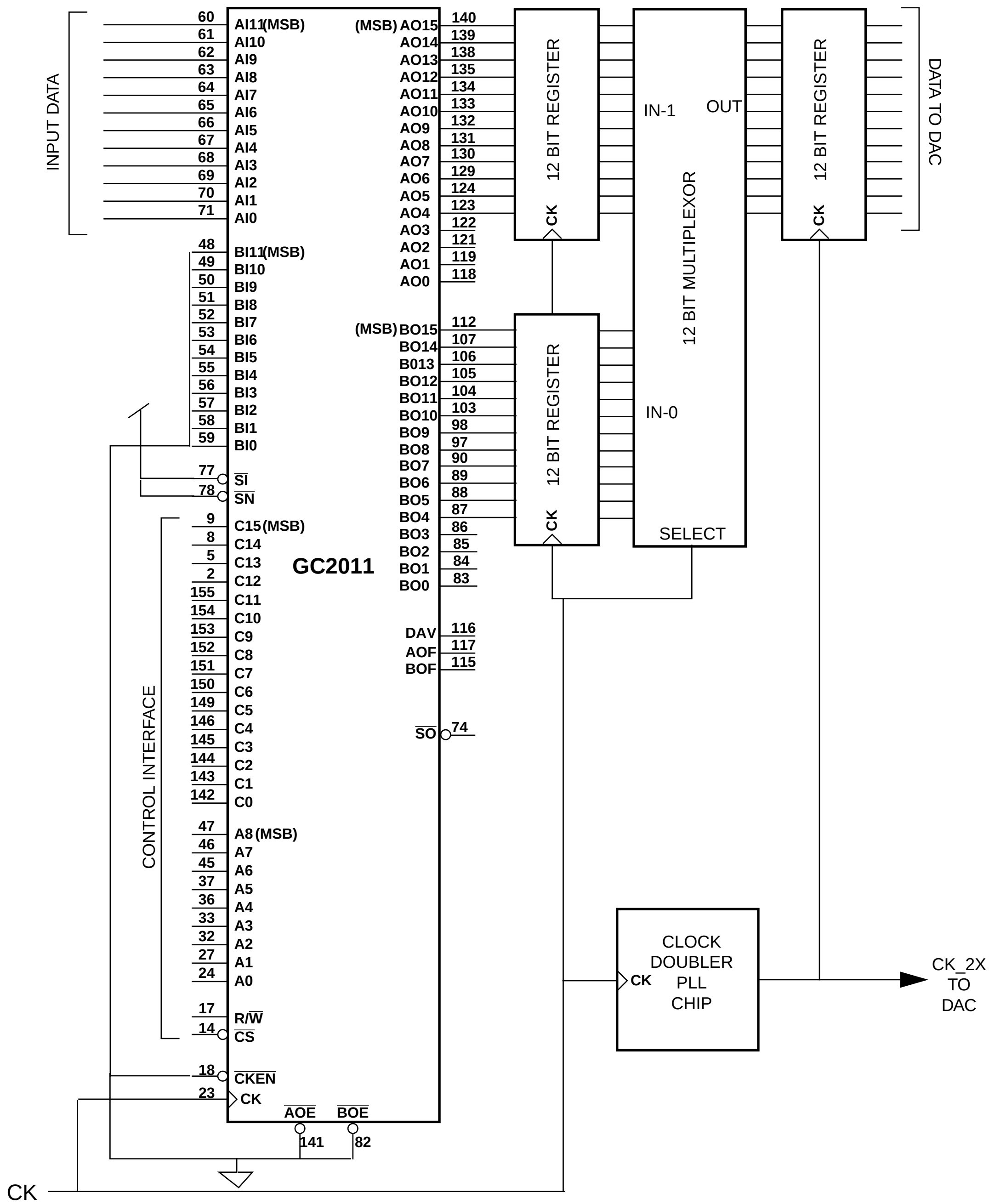

Figure 3. Suggested Schematic

3.0 Programming the GC2011 Chip

The mathematics of the manipulations shown in Figures 1 and 2 can be reduced to dividing the input data into even and odd samples, and filtering them separately, the even samples in the A-path of the GC2011 chip, and the odd samples in the B-path. The mix down by $F_{in}/4$ is performed by negating every other A-path and B-path sample. The A-path and B-path inputs are now at half the clock rate, these are interpolated by a factor of two in each path back up to the F_{in} rate. The output is mixed up by $F_{in}/2$ by negating every other output.

The GC2011 register settings are the “dual path, no-symmetry, interpolate by 2, half in, full out” setting shown in Table 7 of the GC2011 data sheet, but modified to:

(1) introduce a clock cycle delay into the A-path (to separate the even and odd samples)

(2) Select the A-input for the B-path,

(3) Negate every other input (even time half rate inputs for the A-path, odd time for the B-path),

(4) Negate every other output sample (even time for the A-path, odd-time for the B-path).

The proper settings are:

Table 1: UPCONVERSION MODE CONTROL REGISTER SETTINGS

I/O Rates		# of Taps (N)	A-PATH		B-PATH		Cascade	Output	Gain	Tap Storage
In	Out		REG0	REG1	REG0	REG1	REG	REG	REG	
Full	Double	64	7B88	2E00	2B88	2E00	2000	0001	0460	See Below

The gain is set according to the formula:

$$GAIN = 2^{(S-21)}(1+F/16)(DC\_GAIN)$$

Where DC_GAIN is the sum of the 64 coefficients and S and F are the values programmed into the Gain Register. Setting the Gain Register to 0x0460 gives unity gain for a filter with DC_GAIN=32768.

The 64 filter taps are stored in registers 0 and 1 within each filter cell. The odd indexed taps are stored in the A-path and the even indexed taps are stored in the B-path. If the taps are identified as h(k) for k=0 to 63, then the taps are stored in addresses:

```
Store h(4k)   in memory address 192+4*k for k=0 to 15
Store h(4k+1) in memory address 128+4*k for k=0 to 15
Store h(4k+2) in memory address 193+4*k for k=0 to 15
Store h(4k+3) in memory address 129+4*k for k=0 to 15
```

4.0 Cellular Base Station Transmitter Example

This section describes using the GC2011 with GC4114 Quad transmitter chips to build a cellular base station transmit module. The module shown in Figure 4 accepts up to 16 baseband inputs (each input may be a multi-user TDMA signal). The GC4114 chips modulates them up to center frequencies between 2.5 and 27.5 MHz at a sample rate of 60 million samples per second (MSPS). The GC2011 chip up converts the signal by 15 MHz and doubles the sample rate to 120 MSPS. The digital to analog converter (DAC) output is low pass filtered to eliminate high frequency images. The low pass filter output is mixed up by 110 MHz to a center frequency of 140 MHz. The bandpass filter then removes the images below 140 MHz.

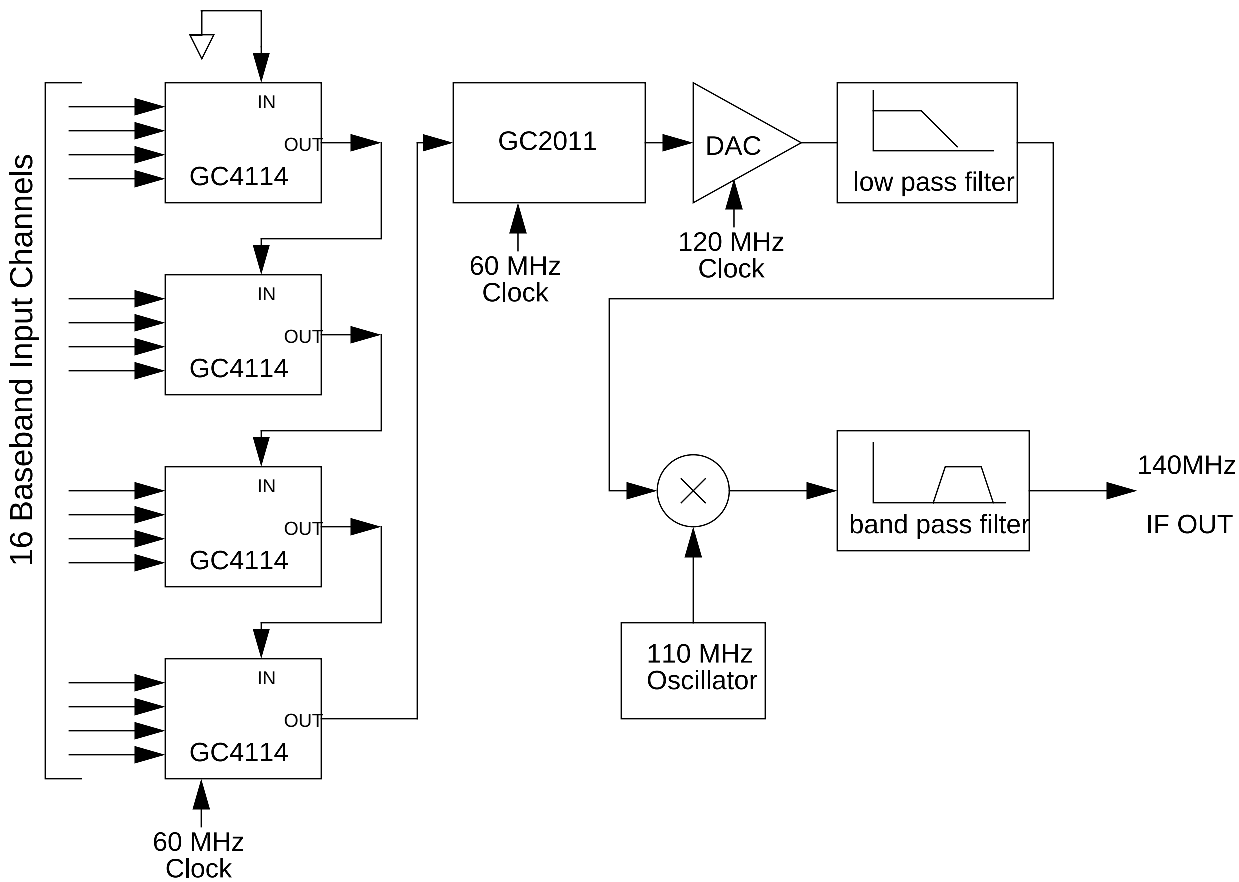

Figure 4. Multi-Carrier Transmit Module Example

The filter in the GC2011 chip is a 64 tap filter designed to interpolate the 60MHz data up to a 120 MHz sample rate. The filter is designed relative to the 120 MHz sample rate and has a passband from 0 to 12.5 MHz and a stopband from 17.5 MHz to 60 MHz. A 64 tap filter suitable for this application is listed below:

11 46 90 137 155 121 31 -89 -183 -192 -88 97 272 330 203 -81 -391 -543 -403 23 552 889 771 129 -812 -1578 -1623 -583 1516 4203 6695 8191 8191 6695 4203 1516 -583 -1623 -1578 -812 129 771 889 552 23 -403 -543 -391 -81 203 330 272 97 -88 -192 -183 -89 31 121 155 137 90 46 11

The DC_GAIN of this filter is 35792 so that the GC2011 gain is set by:

$$\text{GAIN} = 2^{(S-5)}(1+F/16)(0.546)$$

Settings of S=5 and F=13 will give unity gain within 0.1 dB. The gain register should be set to 0x045d.

The spectral response of this filter is shown in Figure 5. This filter has less than 0.4 dB peak to peak ripple and 70 dB of out of band image rejection.

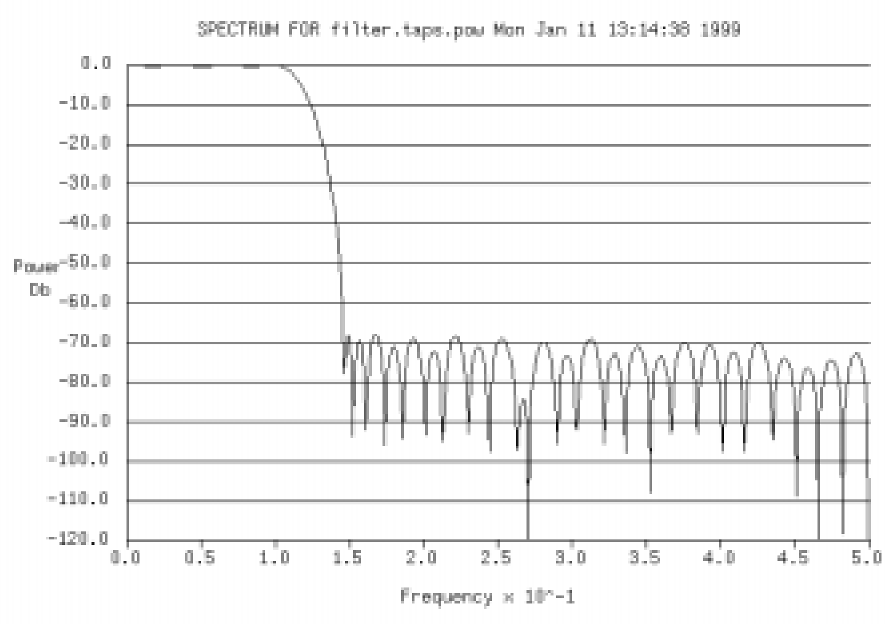

Figure 5. GC2011 Filter Response

The low pass filter which follows the DAC must remove spectral energy above 245 MHz to prevent distortion after the mixer. This analog lowpass filter can be a simple filter with a passband cut off frequency of 47.5MHz and a stopband starting at 245 MHz. Note that frequencies above 245 MHz would mix down by 110 MHz in the mixer and fall into the final passband region around 140 MHz.

The mixer output will have the desired 25 MHz signal band centered at 140MHz, but there will be unwanted components at frequencies below 90 MHz and above 180 MHz. The band pass filter is used to eliminate the unwanted spectral energy. The bandpass filter is centered at 140 MHz, has a passband width of 25 MHz, and a stopband skirt width of 90 MHz.

The IF center frequency of 140 MHz is arbitrary. Other frequencies, such as 900 MHz can be achieved by choosing an oscillator frequency equal to 900MHz minus 30MHz.

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