GC3011 AP NOTE:

USING THE RATE-LOCKED-LOOP (RLL) MODE

1.0 INTRODUCTION

The RLL mode of the GC3011 chip is used to convert an input data rate to an output data rate when the exact ratio between the rates is unknown. The RLL mode drives the resampling ratio to a value which keeps the chip's output FIFO half full. A block diagram of the chip operating in this mode is shown below:

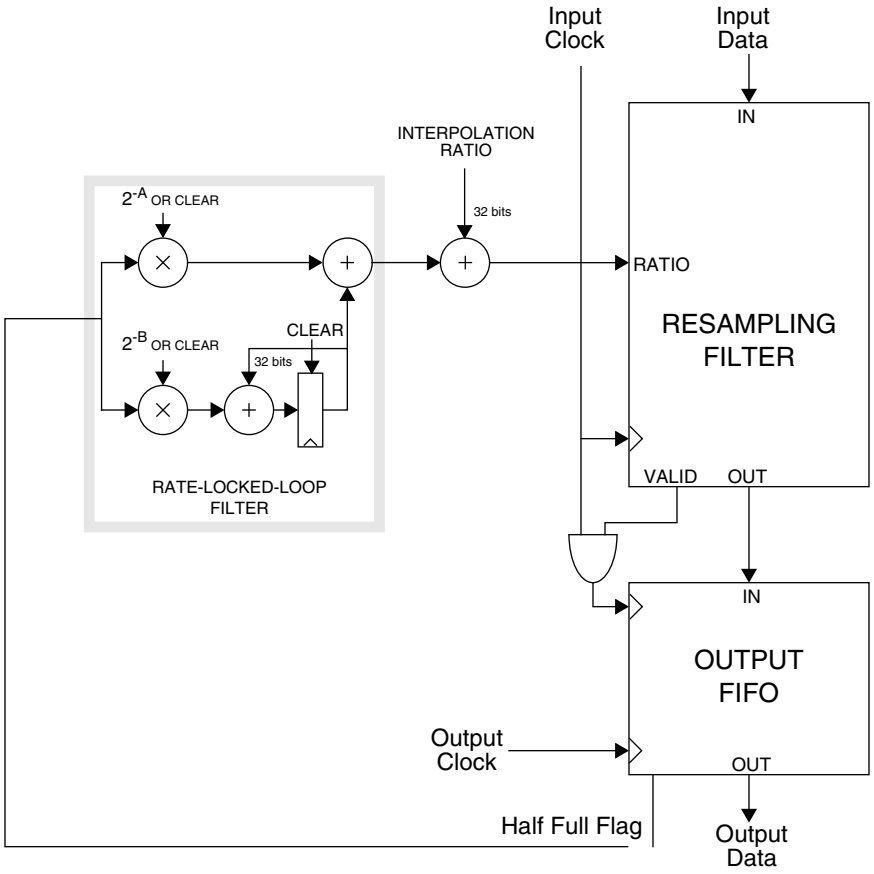

Figure 1. Resampler in RLL Mode

The restrictions on this mode is that the output rate must be less than the input rate, but not less than one-fourth the input rate. If one wishes to up or down sample the data, then one should use the GC2011 Digital Filter chip to double the data rate before using the GC3011 chip to downsample.

2.0 LOOP PARAMETERS

One controls the RLL mode by setting the initial interpolation ratio and the loop filter parameters A and B as shown in Figure 1. The interpolation ratio is the ratio of the input clock rate to the output clock rate. The ratio should be preset to an estimate of the resampling ratio if it is known, other wise it should be set to 2. The ratio is programmed as a 32 bit integer formatted as:

$$RATIO = (\text{desired ratio}) * 2^{30}$$

For example, a resampling ratio of 2.0 would be programmed as 2^{31} = (HEX) 80000000 and a resampling ratio of 1.5 would be (HEX) 60000000.

The values of A and B are critical to in order to insure loop convergence and stability. The matrix shown in the following table shows which combinations of A and B will converge, and what jitter performance can be expected for each combination. No entry in the table means that it was unstable and a U in the table indicates that the jitter was unacceptable. The number in the table is the peak to peak residual jitter measured in parts per 1000 of the output clock period. One can show that the worst case rms noise level due to a jitter of one part per 1000 is A*0.8*π/(2450), where A is the rms amplitude of the signal. This means that the worst case noise level is 60 dB below the signal level.

The -60 dB noise level due to jitter is for a sinewave near 40% of F_{out}, where F_{out} is the output sample rate. The noise level will be lower for broadband signals and sinewaves at lower frequencies.

Table 1: LOOP PARAMETERS

A	B								
	16	17	18	19	20	21	22	23	24
8	U	U	U	U	U	U	U	U	
9	U	U	U	4	U	U	U	U	
10	U	U	2	1.5	1.5	2	U		
11		U	1.5	1	1.3	4	U		
12			2	2	5	U			
13			U	U	U				
14									

As one can see the loop filter shows the minimum jitter at A=11 and B=19 or 20.

3.0 SUGGESTED OPERATING PROCEDURE

To use the RLL mode the user should initialize the control registers with the following settings

Table 2: INITIAL CONTROL REGISTER SETTINGS

Register	Value (hex)	Comment
0	00	Ratio
1	00	
2	00	
3	80	
4	00	No offset
5	C0	
6	0B	A=11
7	D3	B=19
8	FF	Force all syncs
9	30	Counter is unused
10	03	reset FIFO
11	00	PLL is unused
12	20	
13	00	used for status selection

and then turn on the RLL mode by setting registers 8 and 9 to 0. The RLL is locked when the FIFO depth toggles between 7 and 8 and the FE (FIFO ERROR) output pin stays low.

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