GC4016 and GC4116 Power Cycling Considerations

Wireless Infrastructure

ABSTRACT

The GC4016 and GC4116 chips have internal power up reset circuits that need time to discharge before power can be reapplied after VCore power has been turned off. If power is re-applied too soon, the power up reset is not triggered, and the chip's JTAG scan logic may come up in an unknown state which will prevent any control bus accesses. This application note describes what causes the power up cycling problem and how the control bus lock-out condition can be avoided.

1 Introduction

The GC4016 and GC4116 have power-up reset detection circuitry internal to the device. These circuits have an internal RC time constant, and a voltage monitor, with hysterisis. When the RC time constant voltage output is less than the voltage monitor set point, the powerup_reset signal is active. The powerup_reset signal is used to pre-set the Global Reset register bits, and reset the JTAG logic (see Figure 1).

The powerup-reset for the JTAG logic causes the JTAG Controller state machine to initialize to the IDLE mode. If the powerup-reset signal does not occur, the JTAG Controller state machine may initialize in a JTAG test mode, and lock-up the chip's I/O pins. If this happens, the JTAG control signals TMS, TDI, and the TCK are used to force the JTAG state to IDLE. If TMS = 1, and TDI = 1, for at least 5 TCK cycles the JTAG Controller state machine will be in the IDLE mode. See IEEE 1149.1 for JTAG mode definitions (see Figure 2).

2 Condition Causing Loss of Function (See Figure 2)

1. The GC4016 or GC4116 powerup reset capacitor is charged to a voltage above the set point.
2. VCore Power is removed, and reapplied before the Power up capacitor discharges below the setpoint.
3. JTAG controller pin TCK is not clocked
4. In the power up sequence, the JTAG controller does not receive the power-up signal, and initializes in a non-IDLE state

3 Control Bus Test

If the GC4016 or GC4116 is in the JTAG mode, the Control Bus commands will not program the internal registers. The test indicated checks two internal registers for proper operation:

1. Reading the reset register to determine if power-up reset has occurred:
   (GC4016) Read address x0, the value read should be xF0.
   (GC4116) Read address x5, the value read should be xFF
2. Write to the Control Bus
   (GC4016) Write to address x0, the value xF8
   Write to address x2, the value x0B
   (GC4116) Write to address x5, the value xFE
   Write to address x1, the value x01
3. Read from the Control Bus
   (GC4016) Read from address x0, the value should be xF8
   Read from address x2, the value should be x0B
   (GC4116) Read from address x5, the value should be xFE
   Read from address x1, the value should be x01

NOTE: If the device does not read back properly, it may be in JTAG mode.

4 Items used to eliminate the Loss of Function failure

1. The TMS, TDI pins are not pulled down. These pins are left open, or connected in a JTAG chain and are pulled up.
2. The TCK pin is not pulled down or pulled up, but is connected to a low speed clock or pulse source (such as WR#, or RD#). The TCK has at least 5 cycles before the user device programming through the Control Bus.
3. The user device programming after the OFF −> ON power cycle writes to the reset register first, to place the logic in the GC4016 or GC4116 in the reset mode

NOTE: If Power On−> Off −> On cycles are required with Off to On cycles of less than 1 minute, the above method to cause the JTAG Controller to be in IDLE mode is required.

5 Perform Diagnostic Test after Startup

Test to determine if the GC4016, GC4116 Control Bus, clock, and logic are OK

After the Device startup, it is recommended that one of the diagnostic tests is performed. These tests check the internal logic, and power, and clock input.

GC4016, GC4116 POWER ON−>OFF−>ON CYCLE, where VCore has >1 minute OFF Time

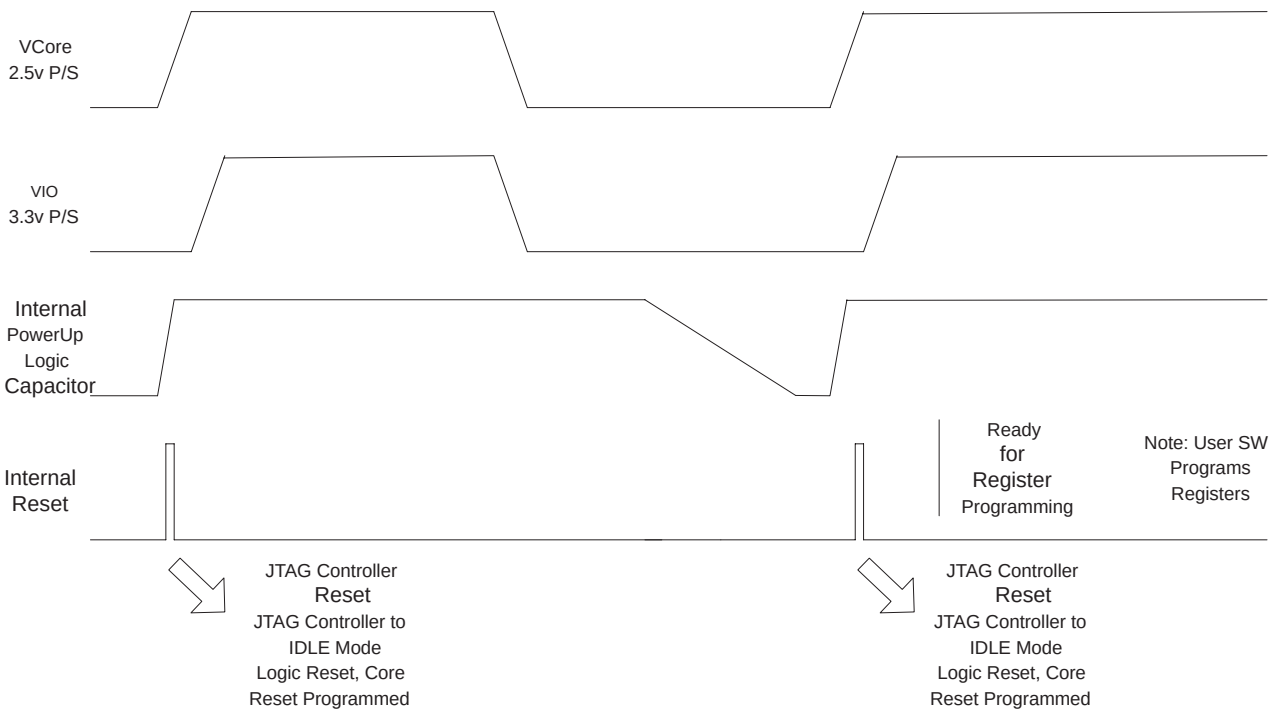

Figure 1. Power On−Off−On Cycle, 1 Minute Off

GC4016, GC4116 POWER ON−>OFF−>ON CYCLE, where Incorrect JTAG operation occurs, recovery using JTAG TCK, TMS, TDI

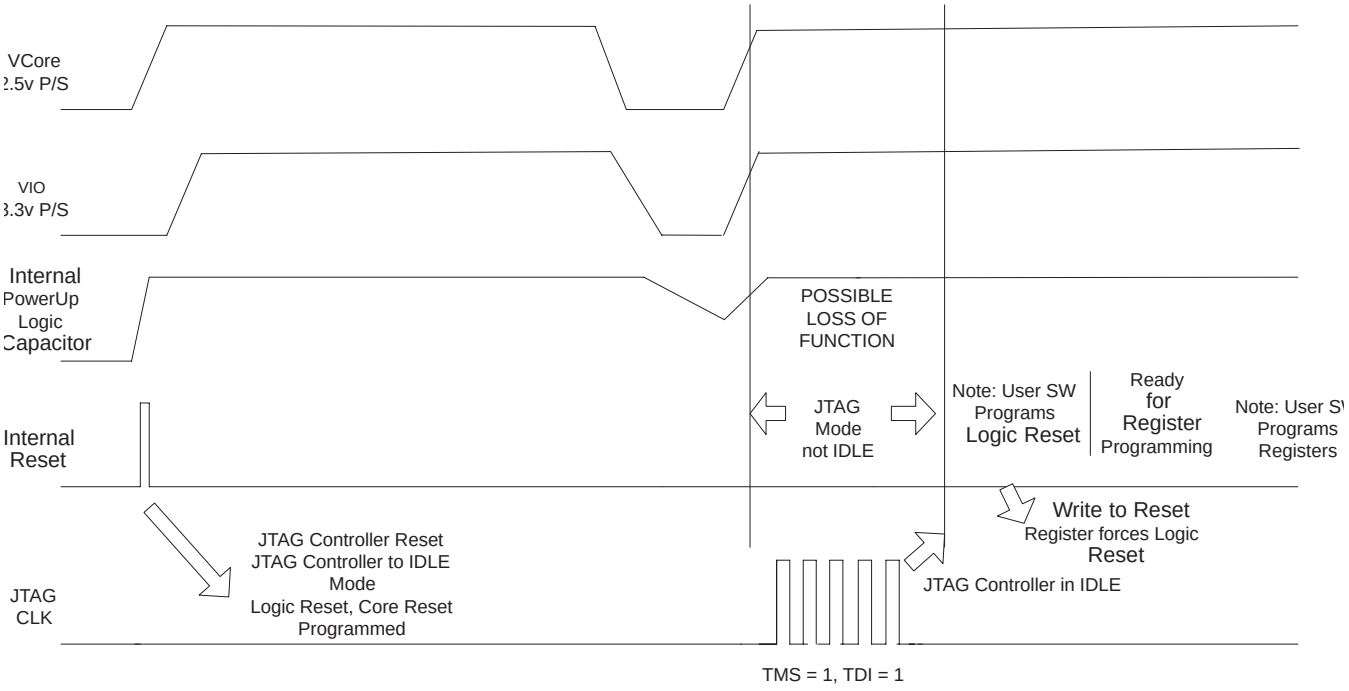

Figure 2. Power On−Off−On Cycle, Incorrect JTAG Operation

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