Application Report
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Synchronization of GC5016 DDC/DUC on TSW4100 EVM

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ABSTRACT

TSW4100 is a digital repeater board containing two GC5016 chips which act as DDC and DUC. A repeater application requires syncronization between the DDC output and the DUC input data to observe the desired repeater functionality. This requires the DDC to operate as a master and DUC as the slave. However, the GC5016 is designed for Master mode only. The board uses FPGA to achieve this sychronization. However, there is a time when the FPGA logic and the synchronization method designed with the FPGA fails in practice. A method to achieve synchronization for lower decimation rates has been proposed in this application report which overcomes the glitch in the FPGA logic.

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Theory behind Synchronization of Data

There are two GC5016 chips on the TSW4100 board. One of them functions as the DDC, and the other functions as the DUC. Data to be repeated is fed to the input of the DDC. The DDC processes the data to the baseband and makes it available to the DUC. The DUC upconverts the data and sends it to the output section of the TSW4100 board. Ideally, the DDC should signal the DUC when data is available at its output. (DDC should act as a master to the DUC slave). However, the GC5016 which is used here as DDC, and the DUC can only functions as a master.

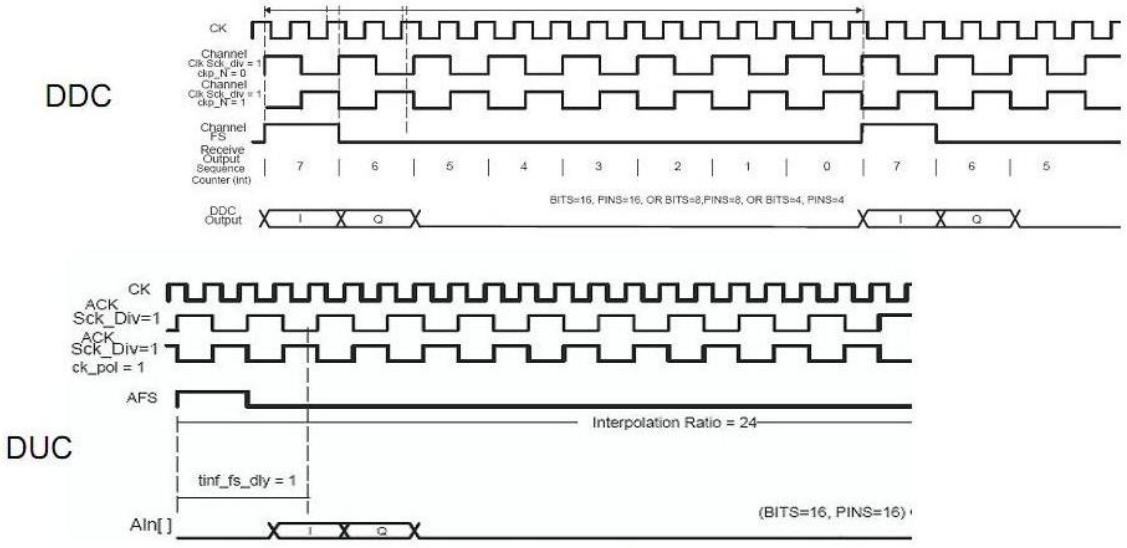

Figure 1. DDC output and DUC input time alignment

Figure 1 shows three clocks viz. CK, ACK and AFS. The clock CK is the primary clock used in GC5016. The ideas behind using a slower channel clock ACK is that it can be used as a reference for the relatively slower operating devices like the data convertors that reside in the singal chain. The data signal A0 and the frame strobe AFS are synchronized to the channel clock ACK. AFS indicates when the data is ready (DDC output) or expected to be ready (DUC input). Since GC5016 can only act as a master (as mentioned previously), the two frame strobes (DDC AFS and DUC AFS) need to be synchronized in order to synchronize the data. The only way to synchronize the data is by delaying the data at the output of the DDC so that it is present at the input of the DUC when it asserts a DUC AFS (i.e when the DUC expects the data at its input).

The data at the input of DDC is latched to CK. The data at the output of the DDC is latched to AFS. Thus, it is observed that CK/AFS = *total decimation rate*. The on-time of AFS equals one ACK clock cycle. Also, CK/ACK is called the *clock ratio*. Since the AFS is tied to ACK, the ratio ACK/AFS has to be an integer. (Since AFS occurs after certain number of ACK clock cycles) *Thus, the clock ratio should always divide the total decimation rate*. Taking this result into consideration, *the clock ratio can be any integer from '1' to 'total decimation rate'.*

The DDC and DUC ACK and AFS will have the same frequency but a phase offset between them. (as shown in the Figure 1). Instead of changing the clock phase offsets of the two ACKs (which is not possible), shift the data with respect to one of the clocks.

The TSW4100 uses a synchronizing logic programmed in the FPGA on TSW4100 to synchronize the data to the clocks. What this does is that it simply delays the data present on the DUC input bus with respect to the DDC output ACK signal based on the sync delay provided by the user.

The sync delay (TSW4100 GUI) is nothing but number of CK clocks between AFS and data A. Note that the user can always delay data and not advance it. Relative to a particular point in the AFS signal, data A can be pushed anywhere from 0 CK cycles to 'total decimation rate' clock cycles. (since the maximum value of clock ratio = total decimation rate). *Thus, sync delay is any number between 0 to the 'total decimation rate'*. Any number exceeding the 'total decimation rate' leads to a configuration of signals which is redundant.

Point to be notes about sync delay: The TSW4100 GUI gives us the flexibility to set the sync delay to any integer multiples of CK clocks. However, since the data is always synchronized to the ACK, theoretically, any values of sync delay that offsets the data relative to ACK are meaningless. But, on a more pragmatic scale this is not observed to be true due to the imperfections in the synchronizing logic.

Data Frame Length

The number of bits of data that is output by GC5016 is asserted by the equation mentioned below.

Data frame length = floor (bits/pins) x (2 if complex) x (n channels if TDM).

Where,

floor (x) = least integer greater than x

TDM = time division multiplexed channels, if any
Now, there should be sufficient ACK clocks between the successive data frames; else there would be data corruption. Number of ACK clocks between two data frames
(or two AFS is) = total decimation rate/clk ratio

Thus,
Data frame length = floor (bits/pins) x (2 if complex) x (n channels if TDM) <= Number of ACK clocks between two data frames (or two AFS pulses) = total decimation rate/clk ratio

For TSW4100, floor (bits/pins) = floor (16/16) =1, since 16 pins are used for 16 bits (see the TSW4100 schematic)

The key results from the above discussion are mentioned in the equations below:

1. CK/AFS = total decimation rate
2. On-time of AFS equals one ACK clock cycle.
3. CK/ACK = clock ratio
4. The clock ratio can be any integer from '1' to 'total decimation rate'

5. The clock ratio should always divide the total decimation rate
6. Sync delay is any number between 0 to the 'total decimation rate'
7. Data frame length = floor (bits/pins) x (2 if complex) x (n channels if TDM) <= Number of ACK clocks between two data frames (or two AFS pulses) = total decimation rate/clk ratio

Note: Constraints (2) and (4) are taken care of by the TSW4100 software.

Thus, in order to synchronize the data, a trial and error method needs to be followed where all possible values of syc delays are experimented and the value which gives the best possible outcome is assigned as the sync delay for a particular GC5016 configuration. (This method is mentioned as the Oscilloscope Method of Synchronization in the User's guide). The various configurations of GC5016 can then be calibrated to the sync delays assigned to them and theoretically, this experiment should be repeatable. However, it is observed in a more pragmatic scenario that this never happens. The value of the sync delay that gives the best outcome is never repeatable for the same configuration of GC5016 (This is due to the glitch in the FPGA logic used on the board)

In order to overcome the above constraint, a method has been developed below which always synchronizes data for a zero sync delay. The only constraint here is that the total decimation rate <=16. This method is foolproof and suffices most of the applications since the total decimation rate is below 16 for most of the customers.

Syncronization at Lower Decimation Rates

It is observed that if the ACK frequency is decreased (clk ratio is increased), then the delay between successive AFS pulses and hence the succesive data frames decreases, since the data is latched for more time. At clk ratio = total decimation rate, the successive data are adjacent to one another. The AFS is always high. Thus, no synchronization is needed in this case.

The above discussion assumes that the data frame is just one bit long (*split IQ mode*). In *4 channel mode of TSW4100*, since the data strobe consists of I and Q (2 bits), the clk ratio = ½ x Total Decimation rate. And so on, for other data frames of other lengths.

Using this observation, the case of clk ratio = total decimation rate should always work for Split IQ mode. Similarly, if the of clk ratio = ½ x Total Decimation rate should always work for 4 channel mode. The sync delay is zero in both the cases. (Note: The TSW4100 software sets the clk ratio to the total decimation rate by default)

However, this method works only for lower decimation rate, due to practical constraints of realizing the circuit with a data convertor. At higher decimation rates (>16), if the clk ratio is assigned close to the total decimation rate, then the ACK clock will be too slow to operate the data convertors used in the signal chain.

Synchronization Test

Before starting this test, make sure that the data setting in the input options tab of the DAC5688 is set to 2's complement format. If the setting in this tab is offset binary, then erroneous results are obtained in the synchronization test.

A) Split IQ Mode (Spectrum Analyzer Method):

Pull open the TSW4100 GUI and configure it to look like Figure 2. TSW4100 is configured to set the 'clk ratio' equal to the total decimation rate. This configuration always synchronizes the DDC and DUC for all possible modes of channel configurations.

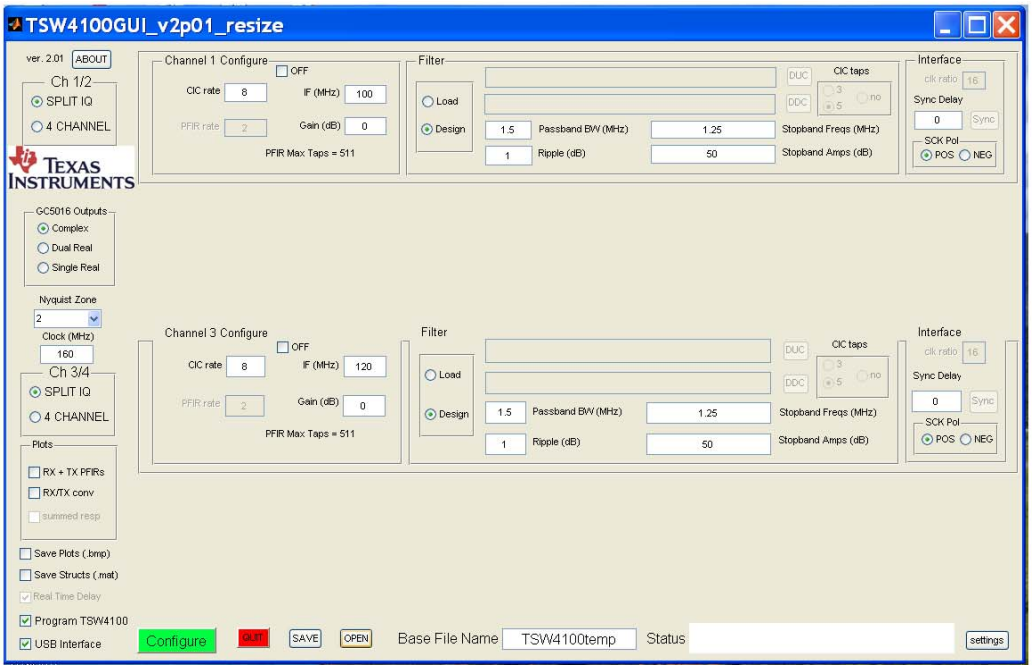

Figure 2. Split IQ Mode

The user should observe a tone at the input frequency of 100.1 MHz as shown in the Figure 3 (The input should be within the passband of the filter and should not be exactly equal to the IF frequency). The signal experiences an attenuation of 7dBm through the ADC and DAC and 3dBm attenuation due to the cables. So, a tone should be observed at the input frequency with -10dBm peak. This confirms the functionality of the digital repeater.

Note: There is a small signal trace at 120MHz; this is because the signal output by the signal generator has harmonics at frequencies other than the frequency that it is supposed to output

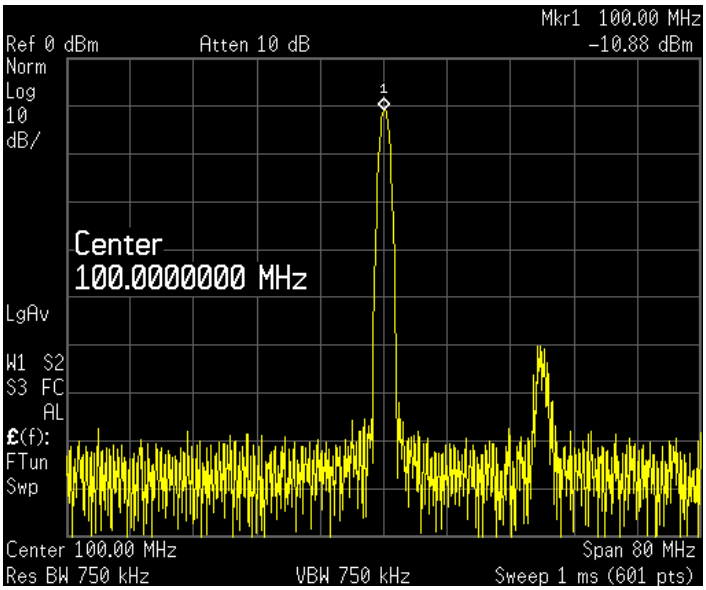

Figure 3. Output of the Spli IQ Mode

B) 4 Channel Mode (Spectrum Analyzer Method):

Pull out the TSW4100 GUI and configure it look like Figure 4. TSW4100 is configured to set the 'clk ratio' equal to the ½ x total decimation rate. This configuration always synchronizes the DDC and DUC for all possible modes of channel configurations. *All the four channels should be symmetric (should have identical configuration) to obtain desired results. (except for the IF frequency)*

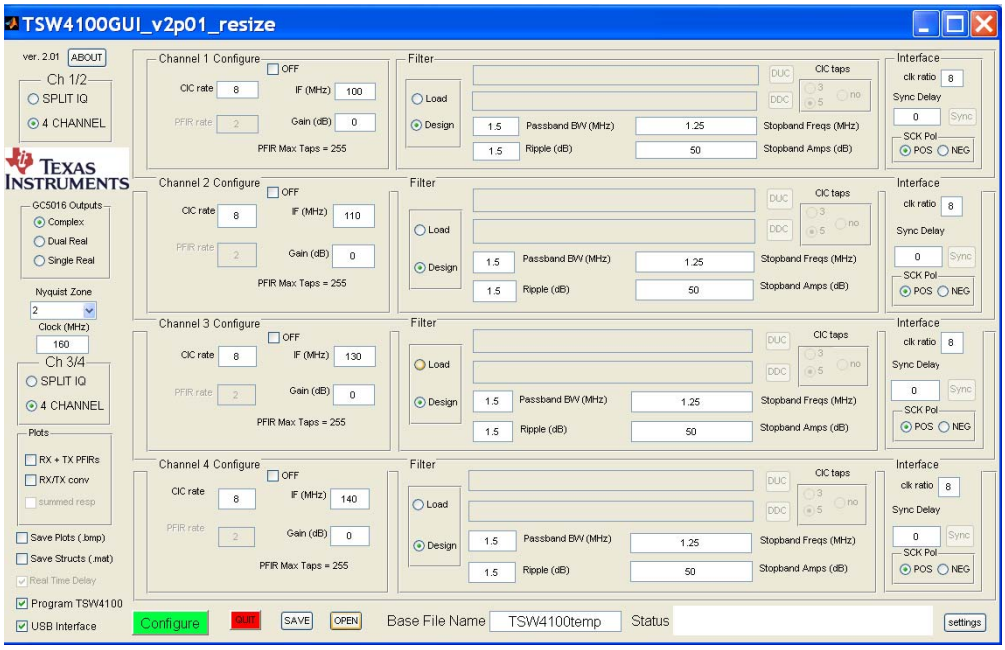

Figure 4. Four Channel Mode Configuration

The user should observe a tone at the input frequency as shown in the Figure 5 (The input should be within the passband of the filter and should not be exactly at the IF frequency). The signal experiences an attenuation of 7dBm through the ADC and DAC and 3dBm attenuation due to the cables. So, a tone should be observed at the input frequency with -10dBm peak. This confirms the functionality of the digital repeater.

Note: There is a small signal trace at three other intermediate frequencies. Because the signal output by the signal generator has harmonics at frequencies other than the frequency that it is supposed to output.

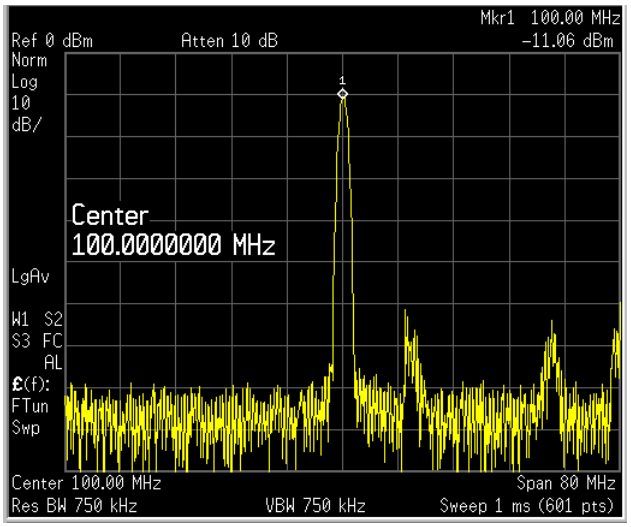

Figure 5. Output of four channel Mode

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