

Keep an eye on the LVDS input levels

By E.D. Cole, P.E.

Application Engineer, Data Transmission

Introduction to LVDS input levels

Low-voltage differential signaling (LVDS) systems (see Figure 1) run at extremely high data rates. These systems are unusually robust in terms of noise immunity and V_{CC} stability, and provide an easy way to get data between two points very quickly. One of the design parameters for an LVDS system is the level of the signal provided to the input of the LVDS driver. It is important that the high-level and low-level inputs to the LVDS driver be kept balanced (symmetrical) about the threshold voltage where the driver switches the output between states.

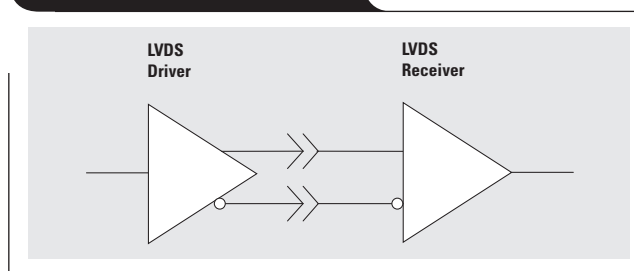
Impact of non-symmetrical inputs

It is easy to see the effects of a non-symmetrical input. As shown in Figure 2, the receiver output appears distorted when the inputs are not centered on the V_{THRES} switching level of the driver.

LVDS level specifications

The input levels to a 3.3-V LVDS line driver are specified as $0.0 V_{DC}$ to $0.8 V_{DC}$ for a logic-0 and $2.0 V_{DC}$ to $3.0 V_{DC}$ for a logic-1. Input levels between $0.8 V_{DC}$ and $2.0 V_{DC}$ are undefined, which means that a driver's switching threshold voltage is also undefined, but it is not hard to determine. By applying a clock signal into the system and adjusting the input levels V_{IH} and V_{IL} while monitoring the receiver output for a 50% duty cycle, the data in Figure 3 is obtained. The values of V_{THRES} shown in Figure 3 are calculated from the V_{IH} and V_{IL} input levels. Note that this can be interpreted as the input sensitivity, not just for the

Figure 1. An LVDS system



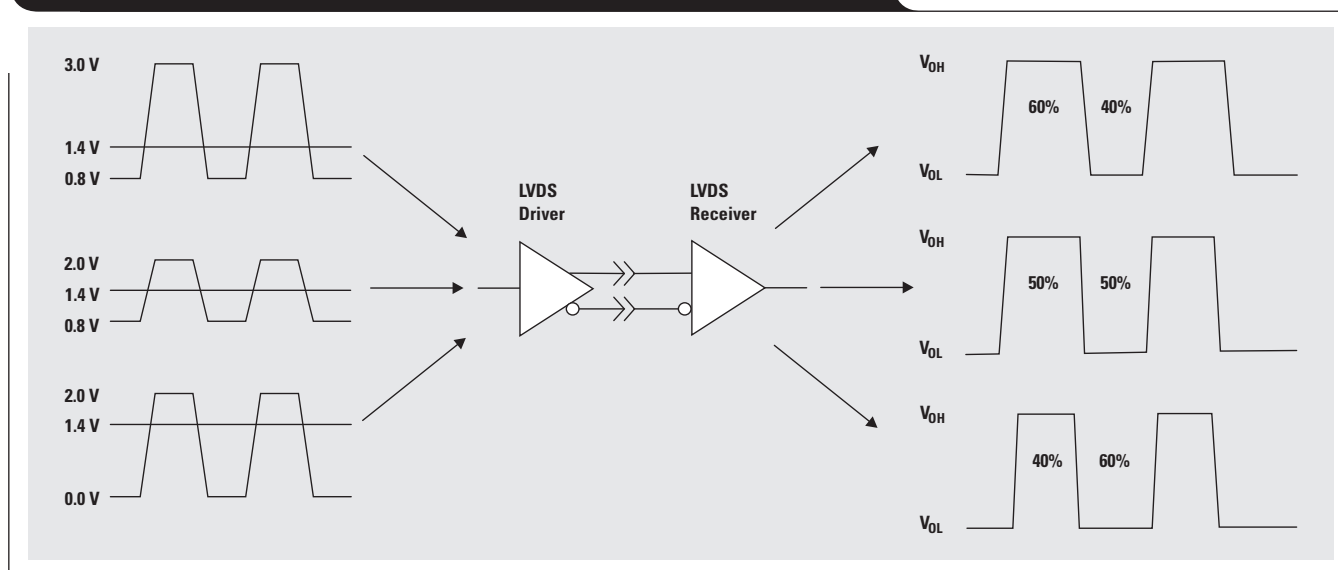
LVDS driver but for the entire LVDS system. The calculated results show a V_{THRES} of approximately $1.35 V_{DC}$ independent of the data (or clock) rate.

Amplitude and offset

Figure 4 shows the driver output when the input levels are not centered on the input threshold. The Channel 1 output (approximately 52% duty cycle) is the driver output when $V_{IH} = 2.35 V_{DC}$ and $V_{IL} = 0.35 V$, which is closely centered about the 1.35-V threshold. But note the Channel 2 waveform in Figure 4 (approximately 60% duty cycle). This shows the driver output response to an input with $V_{IH} = 2.5 V_{DC}$ and $V_{IL} = 0.5 V_{DC}$. This is still at a $2.0 V_{PP}$ amplitude but is centered at $1.5 V_{DC}$. The result is a slight "skew" in the output. The duration of a logic-1 has increased by approximately 640 psec at the expense of the duration (or width) of the logic-0.

Continued on next page

Figure 2. Outputs appear distorted when inputs are not symmetrical



Continued from previous page

When used for clock distribution, this skew is not a problem because the rising and falling edges are clean and stable. High-speed clock signals are rarely perfect square waves with a 50% duty cycle, but when transmitting data (in this example it would become 200 Mbps) this skew could present a problem. At 200 Mbps, each data bit would be 5 nsec wide, but the results in Figure 4 show the Channel 2 waveform with a 0 bit that is 4.36 ns wide (5.0 ns - 0.64 ns) and a 1 that is 5.64 ns wide (5.0 ns + 0.64 ns). The difference between a 0 and 1 would be 1.28 ns, with $V_{IH} = 2.5 V_{DC}$ and $V_{IL} = 0.5 V_{DC}$ —well within the specification.

As long as the inputs are centered about the input threshold, the output will maintain the correct duty cycle and bit width. The reader should think of this as an input amplitude and offset. In Figure 5, Channel 1 is the driver output when the input amplitude is $1.5 V_{DC}$ with an offset of $1.35 V_{DC}$ ($V_{IH} = 2.1 V_{DC}$ and $V_{IL} = 0.6 V_{DC}$). Channel 2 is the driver output after the input amplitude has been

Figure 4. Effects of non-symmetrical inputs on the output waveform

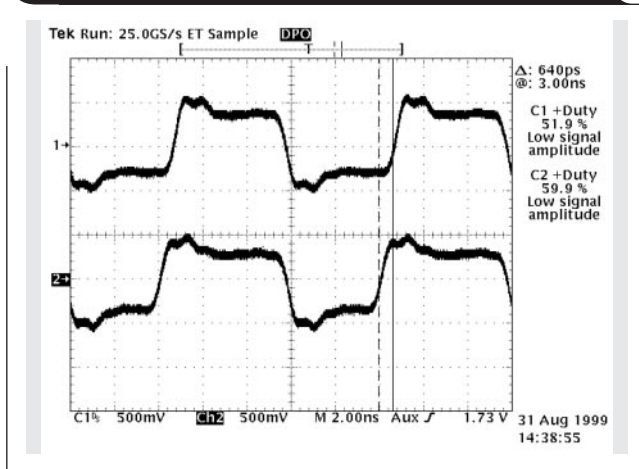


Figure 5. Output response to different amplitude levels but the same offset voltage

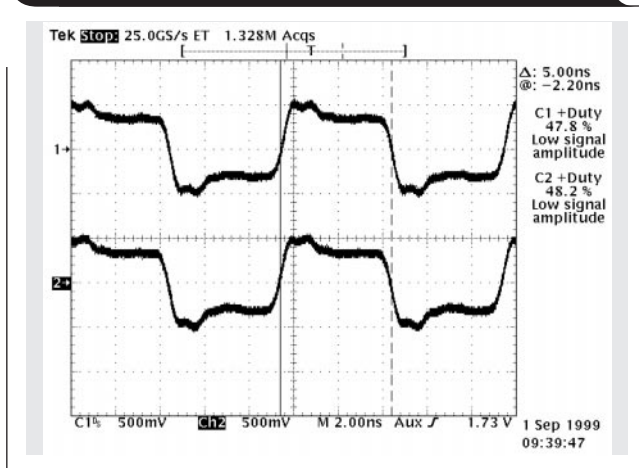
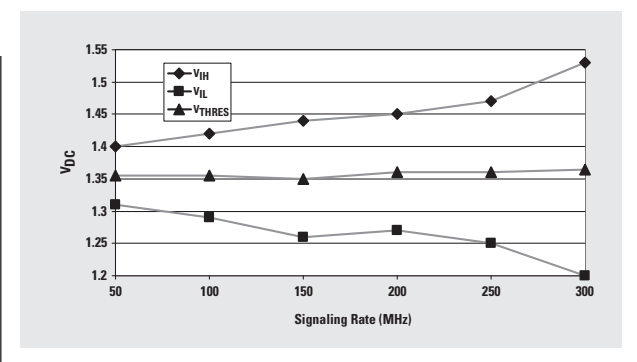


Figure 3. Minimum differential input levels to an LVDS system

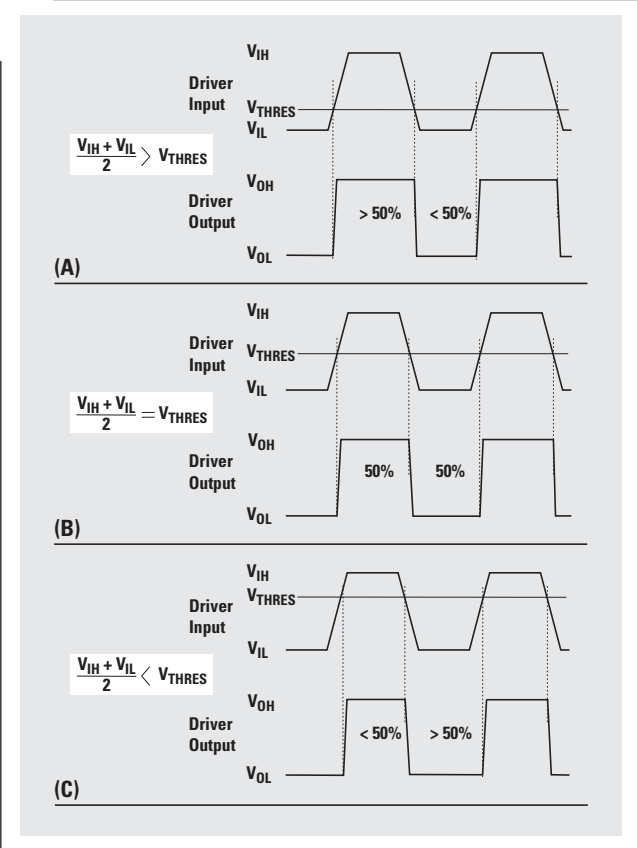


reduced to $0.5 V_{DC}$ with no change in the $1.35 V_{DC}$ offset (now $V_{IH} = 1.85 V$ and $V_{IL} = 0.85 V$). There is no noticeable difference in propagation delay (through the driver) or shift in duty cycle out of the driver. These inputs levels do not meet the LVDS specification, but work well.

Why does the duty cycle change?

The answer to this question is shown in Figure 6. In Figure 6(A), the input levels are centered above the threshold, which results in an increase in the positive

Figure 6. Driver output characteristics vs. input levels



duty cycle. In Figure 6(B), the inputs are centered, which results in a 50%/50% duty cycle. Figure 6(C) shows the input levels centered below the threshold, a condition resulting in a decrease in the positive duty cycle. Figure 6(C) also shows the driver's response to its input signal. This change in duty cycle for NRZ data streams translates into a difference between the width of 0's and 1's.

Threshold adjustment

The threshold cannot be adjusted, but the input levels might be adjustable. The data in Figure 3 shows that even at high signaling rates the input sensitivity to an LVDS driver is approximately 300 mV (and less at slower signaling rates). This means it may be possible to adjust the input signal by installing a resistor divider at the driver input.

The author simulated a 100-MHz clock distribution system with $V_{IH} = 3.5$ V and $V_{IL} = 0.5 V_{DC}$ (amplitude = 3.0 V, offset = $2.0 V_{DC}$) to the driver. To bring the offset voltage down near the driver's threshold voltage, the resistor divider network shown in Figure 7 was installed.

This divider reduces the offset from 2.0 V to 1.4 V, very near the threshold voltage of the driver. It also reduces the input amplitude by 30%, making $V_{IH} = 2.46 V_{DC}$ and $V_{IL} = 0.35 V_{DC}$.

Performance of this modified input was compared to another driver having the standard 50-ohm input termination. The results are shown in Figure 8. Notice that the Channel 1 waveform is very symmetrical with a very good duty cycle. The Channel 2 waveform has an offset voltage of $2.0 V_{DC}$ and produces the increased (57%) positive duty cycle result expected.

Data transmission

What happens when the driver is sending data? A shift in duty cycle is the same as a "skew" in the width of data bits—1's and 0's will not be the same width. This can be seen using eye patterns to view the serial data stream. Figure 8 shows how, using two clock inputs, the resistor divider can be used to center the offset level. By changing these inputs from "clocks" to random data (NRZ formatted) the serial data stream using eye patterns can be viewed. The input levels have not been changed.

Figure 8. Resistor divider input vs. standard input to an input clock

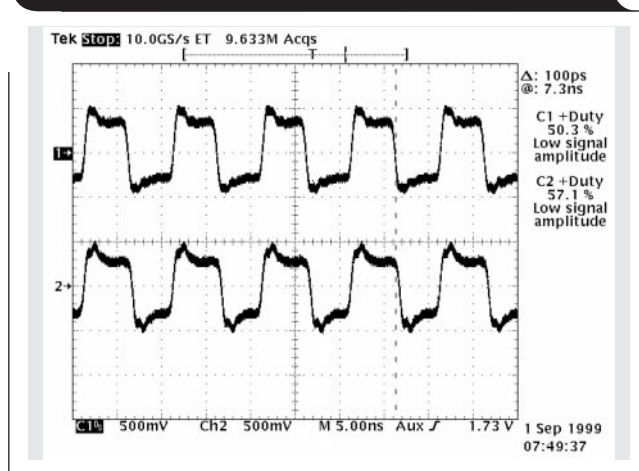
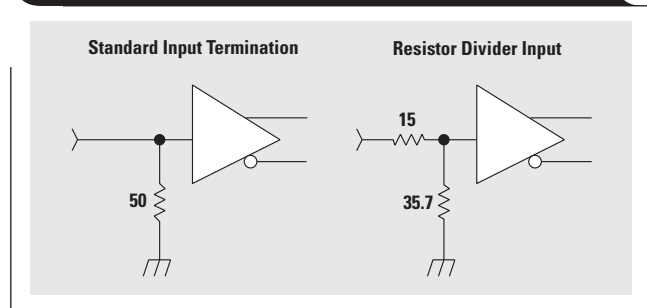


Figure 7. Using a resistor divider to "center" the input levels



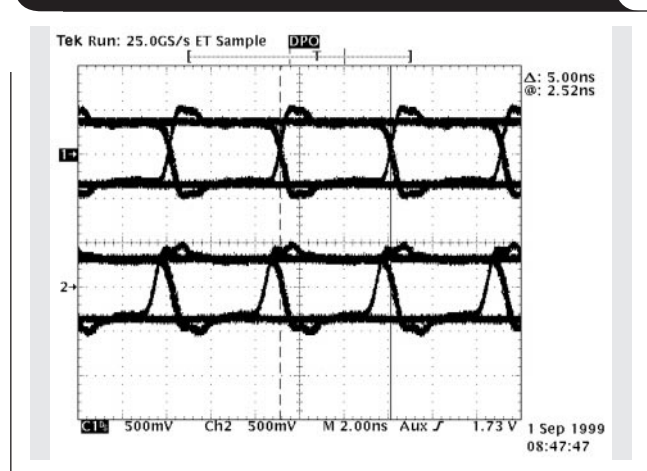
The Channel 1 trace contains the eye pattern for the adjusted signal. The divider has aligned the input very near the switching threshold of the LVDS driver, and the output has the familiar "X" at the crossovers indicating the system is switching 1's to 0's and 0's to 1's at the same time. In other words, each bit is the same width.

The Channel 2 trace is the eye pattern for the unadjusted signal. These input levels resulted in the 57% duty cycle waveform shown in Figure 8, and after the format is changed to "data" the corresponding eye pattern shows that the data bits are not the same width. The falling edges are outside the rising edges, so the 1's are wider than the 0's.

Conclusion

In any transmission system, the input levels to the driver are one of many factors that will influence the quality of the signal out of the line receiver. This is true for any line driver, RS-422, LVDS, SCSI, etc. Keep in mind that the distortion evident in the Channel 2 waveform as shown in Figure 9 can be caused by several factors, and in some cases may not even be related to driver input levels. Also, remember that the Channel 2 waveform is the result of input levels ($V_{IH} = 3.5$ V) that are not even within specified limits.

Figure 9. Resistor divider input vs. standard input using eye patterns on serial data



IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DSP	dsp.ti.com
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital control	www.ti.com/digitalcontrol
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

TI Worldwide Technical Support

Internet

TI Semiconductor Product Information Center Home Page
support.ti.com

TI Semiconductor KnowledgeBase Home Page
support.ti.com/sc/knowledgebase

Product Information Centers

Americas

Phone	+1(972) 644-5580	Fax	+1(972) 927-6377
Internet/Email	support.ti.com/sc/pic/americas.htm		

Europe, Middle East, and Africa

Phone			
Belgium (English)	+32 (0) 27 45 54 32	Netherlands (English)	+31 (0) 546 87 95 45
Finland (English)	+358 (0) 9 25173948	Russia	+7 (0) 95 7850415
France	+33 (0) 1 30 70 11 64	Spain	+34 902 35 40 28
Germany	+49 (0) 8161 80 33 11	Sweden (English)	+46 (0) 8587 555 22
Israel (English)	1800 949 0107	United Kingdom	+44 (0) 1604 66 33 99
Italy	800 79 11 37		
Fax	+(49) (0) 8161 80 2045		
Internet	support.ti.com/sc/pic/euro.htm		

Japan

Fax			
International	+81-3-3344-5317	Domestic	0120-81-0036
Internet/Email			
International	support.ti.com/sc/pic/japan.htm		
Domestic	www.tij.co.jp/pic		

Asia

Phone			
International	+886-2-23786800		
Domestic	Toll-Free Number		
Australia	1-800-999-084	New Zealand	0800-446-934
China	800-820-8682	Philippines	1-800-765-7404
Hong Kong	800-96-5941	Singapore	800-886-1028
Indonesia	001-803-8861-1006	Taiwan	0800-006800
Korea	080-551-2804	Thailand	001-800-886-0010
Malaysia	1-800-80-3973		
Fax	886-2-2378-6808	Email	tiasia@ti.com
Internet	support.ti.com/sc/pic/asia.htm		ti-china@ti.com

C011905

Safe Harbor Statement: This publication may contain forward-looking statements that involve a number of risks and uncertainties. These "forward-looking statements" are intended to qualify for the safe harbor from liability established by the Private Securities Litigation Reform Act of 1995. These forward-looking statements generally can be identified by phrases such as "TI or its management believes," "expects," "anticipates," "foresees," "forecasts," "estimates" or other words or phrases of similar import. Similarly, such statements herein that describe the company's products, business strategy, outlook, objectives, plans, intentions or goals also are forward-looking statements. All such forward-looking statements are subject to certain risks and uncertainties that could cause actual results to differ materially from those in forward-looking statements. Please refer to TI's most recent Form 10-K for more information on the risks and uncertainties that could materially affect future results of operations. We disclaim any intention or obligation to update any forward-looking statements as a result of developments occurring after the date of this publication.

Trademarks: All trademarks are the property of their respective owners.

Mailing Address: Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

© 2005 Texas Instruments Incorporated

SLYT188