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Introduction

Analog Applications Journal is a collection of analog application articles designed to give readers a basic understanding of TI products and to provide simple but practical examples for typical applications. Written not only for design engineers but also for engineering managers, technicians, system designers and marketing and sales personnel, the book emphasizes general application concepts over lengthy mathematical analyses.

These applications are not intended as "how-to" instructions for specific circuits but as examples of how devices could be used to solve specific design requirements. Readers will find tutorial information as well as practical engineering solutions on components from the following categories:

- Data Acquisition
- Power Management
- Interface (Data Transmission)
- Amplifiers: Op Amps

Where applicable, readers will also find software routines and program structures. Finally, *Analog Applications Journal* includes helpful hints and rules of thumb to guide readers in preparing for their design.

Matching the noise performance of the operational amplifier to the ADC

By Bonnie C. Baker (Email: bonnie@ti.com)
Senior Applications Engineer

Proper selection of the operational amplifier that drives an analog-to-digital converter (ADC) in a mixed-signal application is critical. The designer must compare issues such as amplifier noise, bandwidth, settling time, and slew rate to the ADC's signal-to-noise ratio (SNR), spurious-free dynamic range (SFDR), input impedance, and sampling time. This article specifically addresses the matching of the noise specifications and performance of an op amp and a successive approximation register (SAR) ADC in a single-supply environment.

The noise that the amplifier generates originates from the input differential stage. The input stage of every amplifier generates transistor-device noise, which spot-noise graphs describe as referred-to-input (RTI) noise. With this graphical information we can determine how much noise reaches the input terminal of the ADC by calculating the referred-to-output (RTO) amplifier noise.

This discussion begins with a description of the amplifier's device noise. The amplifier noise sources are then tied together into one figure of merit, and the units are converted from volts to an SNR in decibels. Finally, the impact of the op amp in this mixed-signal circuit (Figure 1) is determined by calculating the combination of the op amp SNR value with the ADC's SNR performance.

Characteristics of the amplifier noise

It is important to understand the noise that the operational amplifier generates in this application. The typical performance of the amplifier given in its product datasheet shows that the op amp noise behavior over frequency has a signature that is unmistakable (see Figure 2). In this article, since we will consider the effects of using a single-supply CMOS amplifier, the input current noise is low enough that we can ignore it. Here we will consider only the effects of the amplifier's voltage noise.

The amplifier noise specification in the typical amplifier datasheet is an RTI specification. We can model the amplifier noise as a voltage source at the non-inverting input of the amplifier. The electrical characteristics table of an operational amplifier gives the input voltage noise

Figure 1. Typical driver circuit for SAR ADC

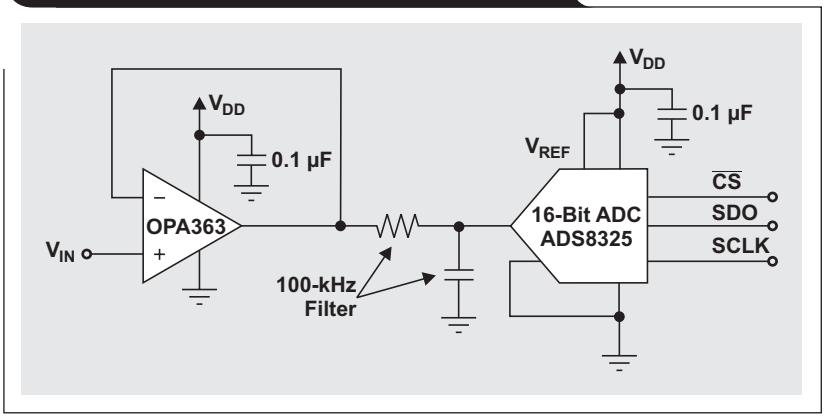
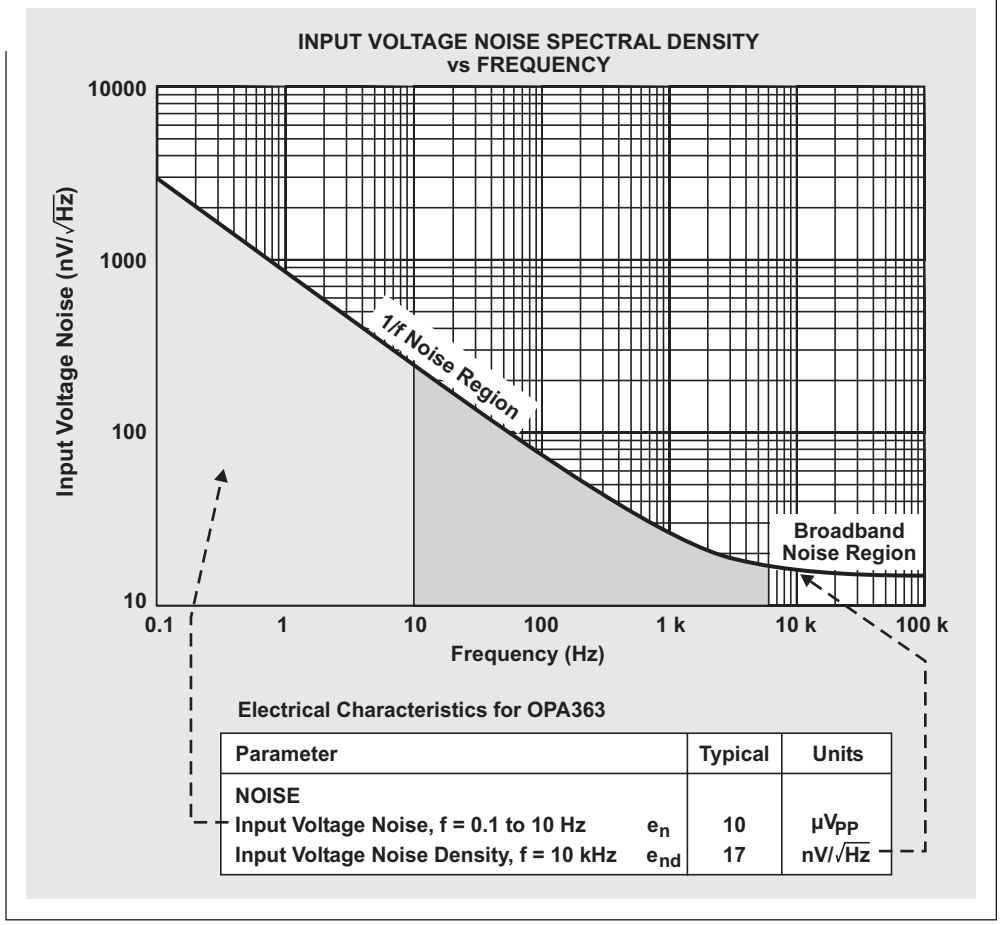


Figure 2. OPA363 amplifier noise parameters



and input voltage noise density specifications (see Figure 2). The input voltage noise specification (10 μV_{PP}) describes the low-frequency noise of the amplifier in terms of a bandwidth. This bandwidth is part of the 1/f noise region of the amplifier. The transistors in the input stage of the amplifier, along with the input-stage active load, generate this noise.

Input voltage noise density calls out a noise figure that refers to one frequency. For instance, the electrical characteristics table in Figure 2 shows that the input voltage noise density (e_{nd}) at 10 kHz is equal to 17 $nV/\sqrt{Hz}$. Usually this specification appears in the broadband-noise portion of the frequency plot (Figure 2). Theoretically, this broadband noise is flat. Assuming that it is flat is a good estimate of the amplifier's behavior. The resistors inside the operational amplifier primarily generate the broadband noise whether they are diffused resistors or the source and drain of the transistors.

The amplifier datasheet contains a typical specification graph that shows the input voltage noise density versus frequency. Figure 2 is an example of this type of graph. In this example, the input voltage noise specification is equal to the area beneath the input-voltage, noise-density curve between the specified frequencies of 0.1 and 10 Hz. Note that the units for this specification are peak-to-peak. To convert this to an rms value, simply divide the peak-to-peak value by 6.6 (industry-standard crest factor [CF] = 3.3).

Table 1 contains typical CF values used to convert rms to peak-to-peak values (and vice versa). To estimate the peak-to-peak operational amplifier output noise voltage, multiply the rms output voltage by 2 × CF. To estimate the ADC peak-to-peak output bit performance, subtract the bit crest factor (BCF) from the rms specification.

Table 1. Crest factor and bit crest factor values used for conversions from rms to peak-to-peak

CREST FACTOR (CF) (V)	BIT CREST FACTOR (BCF) (Bits)	ADC CONVERSIONS WITHIN THE PEAK-TO-PEAK LEVELS (%)
2.6	2.38	99
3.3*	2.72	99.9
3.9	2.96	99.99
4.4	3.14	99.999
4.9	3.29	99.9999

*Industry standard

We can easily calculate the noise underneath the curve in Figure 2 for different input voltage noise bandwidths in the 1/f region. The first order of business in this calculation is to determine the input noise density at 1 Hz. Once we find that value, the following simple formula will provide the rms noise under the curve.

$$V_{(1/f):\,f1\text{-}f2} = C\sqrt{\ln\left(\frac{f_2}{f_1}\right)},$$

where C is equal to the input noise density at 1 Hz.

As an example, the amount of rms noise produced by the amplifier shown in Figure 2 from 0.1 Hz to 6000 Hz is:

$$V_{(1/f):\,f1\text{-}f2} = C\sqrt{\ln\left(\frac{f_2}{f_1}\right)},$$

$$V_{(1/f):\,f1\text{-}f2} = 700\ \text{nV}\sqrt{\ln\left(\frac{6000}{0.1}\right)}, \text{ and}$$

$$V_{(1/f):\,f1\text{-}f2} = 2.32\ \mu\text{Vrms}.$$

With this calculation, and with the amplifier noise gain G = 1, the SNR at the output of the amplifier for the 1/f noise is:

$$SNR_{OPA} = 20\log_{10}\left(\frac{V_{OUT\text{-}rms}}{G \times V_{(1/f):\,f1\text{-}f2}}\right),$$

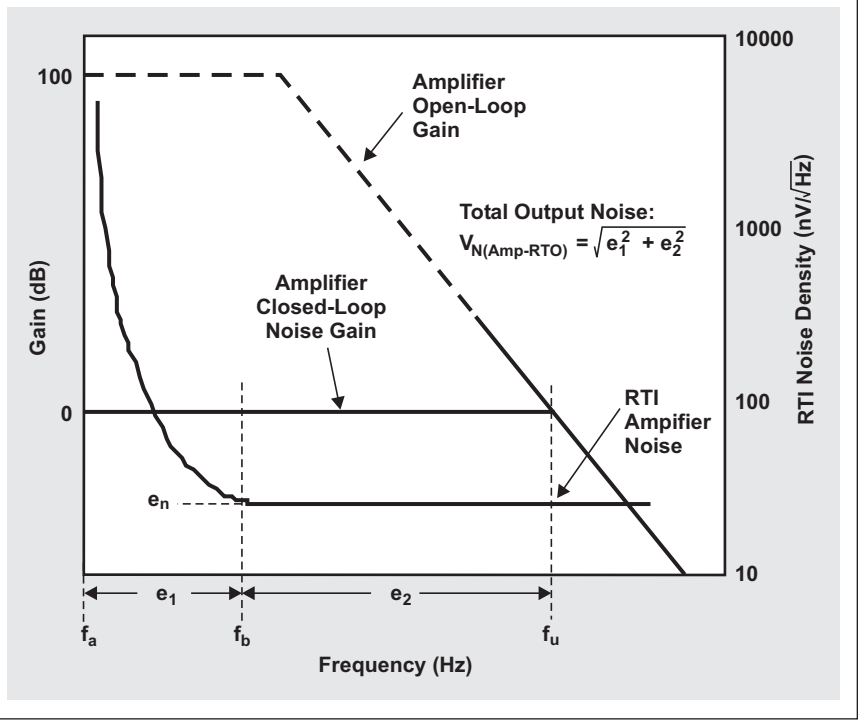
$$SNR_{OPA} = 20\log_{10}\left(\frac{5\ \text{V}}{\frac{2\sqrt{2}}{2.32\ \mu\text{V}}}\right), \text{ and}$$

$$SNR_{OPA} = 117.6\ \text{dB}.$$

When we think about noise at these low frequencies, we may jump to the conclusion that we should take this formula down to a very low frequency, such as 0.0001 Hz (0.0001 Hz = 1 cycle per 2.8 hours). However, at frequencies lower than 0.1 Hz, which is one cycle every 10 seconds, it is very possible that other things such as temperature, aging, or component life are changing in the circuit. Realistically, low-frequency noise from the amplifier will probably not appear at this sample speed; but changes in the circuit, such as temperature or power supply voltage, may.

The amplifier table of specifications (Figure 2) also gives the input noise density value. This specification is always at a higher frequency, in the area where the input voltage noise is relatively constant. For this region of the curve, multiplying the square root of the bandwidth and the noise density derives the noise across this bandwidth. For example, if the noise of the amplifier is 17 nV/√Hz at 10 kHz, the noise from the amplifier across the bandwidth of 6 kHz to 100 kHz is:

Figure 3. Typical RTI noise evaluation



$$V_{1\text{-}100\ \text{kHz}} = (\text{Noise Density at 10 kHz})\sqrt{BW},$$

$$V_{1\text{-}100\ \text{kHz}} = e_{nd}\sqrt{BW},$$

$$V_{1\text{-}100\ \text{kHz}} = \left(17\ \text{nV}/\sqrt{\text{Hz}}\right)\left(\sqrt{100{,}000 - 1{,}000}\right), \text{ and}$$

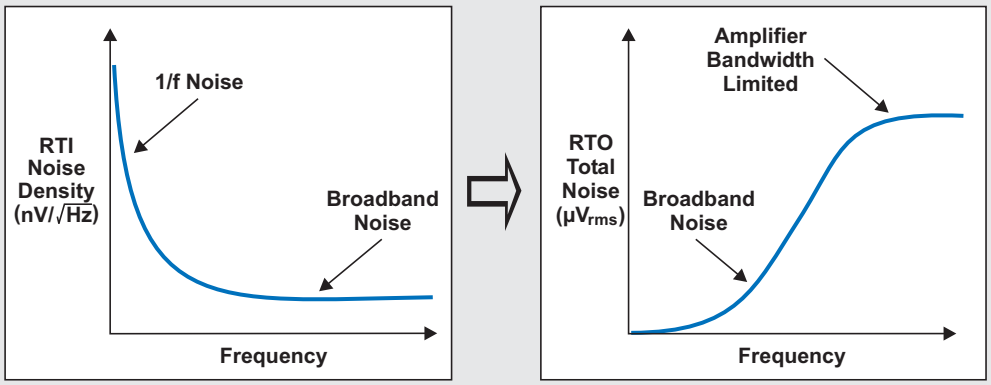
$$V_{1\text{-}100\ \text{kHz}} = 5.21\ \mu\text{Vrms},$$

where BW is equal to the bandwidth of interest.

So how do we get from the manufacturer's graph to an RTO noise value? We calculate the area beneath the noise curve and multiply that times the noise gain of the amplifier. In this example, the noise gain of our circuit is +1 V/V. We determine the noise that the amplifier contributes in both regions and then add the two values together using the square root of the sum of the squares. Figure 3 shows the formula for this calculation and illustrates the two regions.

Figure 3 separates the noise into two parts. In region e_1, we gain the 1/f noise of the amplifier by the dc gain of the amplifier circuit, which is +1 V/V. The specifications for amplifier noise are in nanovolts per square root of hertz. So the analysis is complete when we multiply the average noise over the region by the square root of the bandwidth of that region. For CMOS amplifiers, the 1/f region is usually from 0.1 Hz to 100 Hz up to 1000 Hz. Since this noise value is multiplied by the square root of the bandwidth, its

Figure 4. Graphical representation of RTI noise density and RTO noise



(a) Simulated Noise Response (b) Cumulative Noise

Note: The area under the RTI plot of a frequency region is multiplied by the square root of that bandwidth and closed-loop gain to calculate the RTO plot.

contribution is low. In region e_2, the broadband noise of the amplifier is multiplied by the amplifier circuit gain, which is again +1 V/V, and the square root of the bandwidth.

Each region contributes to the overall circuit noise:

$$e_1 = C\sqrt{\ln\left(\frac{f_b}{f_a}\right)} = 2.32\ \mu\text{Vrms}$$

$$e_2 = e_n\sqrt{f_2 - f_1} = 5.21\ \mu\text{Vrms}$$

The total noise at the output of the amplifier is:

$$V_{N(\text{Amp-RTO})} = \sqrt{e_1^2 + e_2^2}$$

$$= 5.70\ \mu\text{Vrms}.$$

With this calculation, the SNR at the output of the amplifier for the 1/f noise is:

$$\text{SNR}_{\text{OPA}} = 20\log_{10}\left(\frac{V_{\text{OUT-rms}}}{V_{N(\text{Amp-RTO})}}\right),$$

$$\text{SNR}_{\text{OPA}} = 20\log_{10}\left(\frac{\frac{5\ \text{V}}{2\sqrt{2}}}{5.70\ \mu\text{V}}\right), \text{ and}$$

$$\text{SNR}_{\text{OPA}} = 109.8\ \text{dB}.$$

We can validate this noise calculation using the Texas Instruments (TI) SPICE simulation tool, TINA-TI™. This tool can be found at amplifier.ti.com under "Engineering Resources."

The two graphs in Figure 4 demonstrate how TINA-TI can help us understand the noise in our circuit. Figure 4(a) shows the simulated noise response of an amplifier. Figure 4(b) provides the cumulative noise as frequency increases. Notice that the noise is very low at the lower frequencies in Figure 4(b). This is because the lower bandwidths are multiplied by the square root of a small number, the bandwidth. As frequency increases, the cumulative noise also increases. One would think that at higher frequencies the increases in noise would be less because of the characteristics of Figure 4(a). As we can see, this is not true, because the bandwidth multiplier (square root of the bandwidth) is larger at higher frequencies.

Combining the op amp and ADC noise figures

Once we examine the amplifier for possible noise sources, it is easy to evaluate the total noise of the system in Figure 1. This system uses the 16-bit ADC, ADS8325, whose maximum sample rate is 100 ksps. The typical SNR of this device is 91 dB.

As we found before, the OPA363 RTO noise is 109.8 dB. Now we can determine the total noise of the system by using the op amp SNR and ADC SNR, and applying the theorem of taking the square root of the sum of the squares.

$$\text{SNR}_{\text{Total}} = -20\log_{10}\sqrt{10^{-\text{SNR Op Amp}/10} + 10^{-\text{SNR ADC}/10}}$$

$$\text{SNR}_{\text{Total}} = 90.94\ \text{dB}$$

From this calculation we can see that the amplifier noise has very little impact on the resolution of the system.

With the devices in the circuit, the SNR performance will always be equal to or less than the lowest value. Given this interaction between the amplifier and ADC, picking a higher-noise amplifier will give the worst results. For instance, if we use an amplifier in a gain of 10 V/V that has a typical voltage noise specification of e_{nd} = 45 nV/$\sqrt{Hz}$ at 10 kHz, then SNR_{Total} is 82.2 dB. If we use the 16-bit ADS8325, then SNR_{Total} is 81.6 dB. In this example, the amplifier is dominating the noise of the circuit.

There are more factors that have an effect on the amplifier selection process, but amplifier noise can have a significant effect on the digital code outcome. If the amplifier is too noisy, the ADC will reliably convert the noise from the amplifier circuit to the digital output. On the other hand, it is possible to have an ADC that is noisier than the amplifier circuit. If we choose an extremely low-noise amplifier without evaluating the system, we will probably spend too much money on one component or the other. Determining the potential noise in a circuit is always a daunting challenge, but there are some general rules of thumb that can be applied to overcome these problems. We can use the circuit's frequency range to our advantage in the calculations; and, when we combine noise sources, we can use the equation for the square root of the sum of the squares. By using these tricks we can quickly determine the compatibility of our amplifier/ADC combination.

In this circuit an amplifier isolates impedances in the signal chain. Other features, like gain or filtering, can be added; but regardless of the features we put around the amplifier, we should always ensure that the amplifier circuit preserves the integrity of the ADC.

References

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Document Title	TI Lit. #
1. "1.8V, 7MHz, 90dB CMRR, Single-Supply, Rail-to-Rail I/O Operational Amplifier," OPA363/2363, OPA364/2364, OPA4364 Datasheet	sbos259
2. Bonnie Baker, *A Baker's Dozen: Real Analog Solutions for Digital Designers* (Newnes-Elsevier, 2005).	—
3. Howard Johnson and Martin Graham, *High-speed Digital Design: A Handbook of Black Magic* (Prentice-Hall, 1993).	—
4. Henry Ott, *Noise Reduction Techniques in Electronic Systems* (New York: John Wiley, 1998).	—
5. *The RF Capacitor Handbook* (American Technical Ceramics Inc.).	—
6. Tim Williams, *The Circuit Designer's Companion*, 2nd ed. (Newnes-Elsevier, 2005).	—
7. Edward C. Jordan, Ed., *Reference Data for Engineers: Radio, Electronics, Computer & Communications*, 7th ed. (Sams, 1985).	—

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dataconverter.ti.com
www.ti.com/sc/device/ADS8325
www.ti.com/sc/device/OPA363

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TLC5940 PWM dimming provides superior color quality in LED video displays

By Michael Day (Email: m-day@ti.com)
Applications Manager, Portable Power Products

A design technique called dot correction was discussed in Reference 1. This technique is used to calibrate each individual pixel in large form-factor displays. Once calibrated, or dot corrected, each pixel provides the same brightness level when commanded to a specific brightness. This technique calibrates the analog current supplied through individual LEDs in an array. While dot correction offers an excellent solution that compensates for the variation of lumen output between pixels, this analog brightness adjustment is only the first step in developing a high-quality LED display. This article presents a technique called pulse width modulation (PWM) dimming that can be used to adjust LED brightness while maintaining superior color quality. This technique is also referred to as PWM grayscaling.

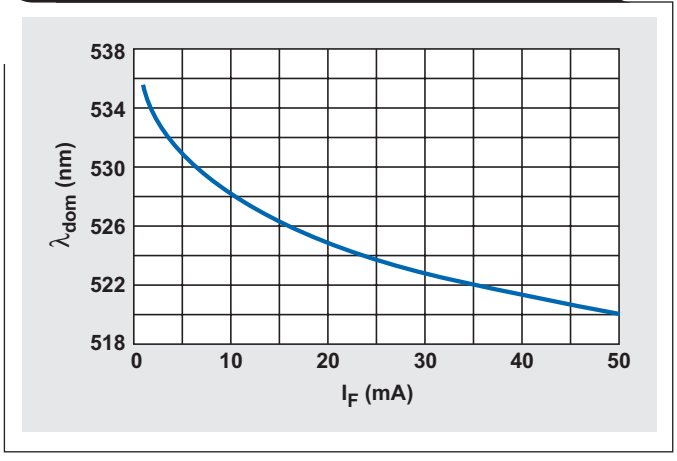
Low-end displays typically require only monochromatic LEDs. Applications include simple sporting scoreboards, single-line scrolling displays, and transportation road signs. A newer and growing market requires high-quality video displays capable of full-motion video shown in millions of colors. These applications include ever-expanding advertising markets encompassing convenience stores, shops, gas stations, and stadiums. An emerging market for LEDs is in DLP- and LCD-based televisions. Accurate color reproduction in these televisions is dependent on the available colors in the backlight. Proper control of the red, green, and blue (RGB) LEDs produces a color spectrum that is larger than the NTSC color space for television broadcasts. By contrast, cold cathode fluorescent lamp (CCFL) backlighting only produces about 85% of the NTSC color spectrum.

These displays require sophisticated LED drivers capable of providing multiple brightness levels. The number of colors available in the display is proportional to the number of brightness levels available for each of the RGB LEDs that make up a single pixel in the overall display. Competition between display manufacturers is driving designers toward high-end LED drivers with integrated PWM functionality capable of delivering thousands of brightness levels. These brightness levels result in enhanced color shading and improved video quality. The TLC5940 is designed to meet these needs.

High-quality, full-color video requires hundreds or thousands of brightness levels between 0% and 100%. Older LED drivers use analog dimming to provide these brightness levels. Analog dimming changes brightness by changing the LED's forward current. For example, if an LED is at full brightness with 20 mA of forward current, then 25% brightness is achieved by driving the LED with 5 mA of forward current. While this dimming scheme is simple and works well for lower-end displays, the drawback with analog dimming is that an LED's color shifts with changes in forward current. Figure 1 shows a true green LED's color variation with changes in forward current. This LED's full brightness is specified at 20 mA. Analog dimming to 25% brightness shifts the color spectrum from 525 nm to 531 nm. This color shift becomes unacceptable in displays requiring a true color representation.

PWM dimming provides reduced brightness by modulating the LED's forward current between 0% and 100%. The LED brightness is controlled by adjusting the relative ratios

Figure 1. Color shift caused by analog dimming



of the on time and off time. A 25% brightness level is achieved by turning the LED on at full current for 25% of each period. Figure 2 shows a comparison between analog and PWM dimming for a 20-mA LED being dimmed to 25% brightness. To keep the user from seeing the LED turn on and off, the switching speed must be greater than 100 Hz. Above 100 Hz, the human eye averages the on and off times, seeing only an effective brightness that is proportional to the LED's on-time duty cycle. The advantage of PWM dimming is that the forward current is always constant, so LED color does not vary with brightness like it does with analog dimming. Pulsing the current provides precise brightness control while preserving the color purity.

Since this type of PWM dimming is microprocessor-driven, it is limited to a maximum number of discrete brightness levels, commonly referred to as grayscale steps, for each LED. The total available number of discrete steps during any one period determines the LED's brightness resolution. High-quality displays require hundreds to thousands of brightness steps to accurately reproduce the full color spectrum necessary for full-motion video. The TLC5940 provides 12 bits of PWM dimming to meet this need. These 12 bits of resolution provide 2^{12} = 4096 shades for each LED. Each pixel in a color display is composed of three LEDs—red, green, and blue. Individually driving each of these LEDs to one of 4096 brightness levels renders the RGB cluster capable of 68.7 billion colors.

The following example illustrates the TLC5940 PWM dimming capabilities. For simplicity, the example assumes there are only 3 bits of PWM dimming. Since 3 bits is equivalent to 2^3 = 8 shades, each LED can be programmed to stay on anywhere from 0 to 7 PWM grayscale steps. Each video frame starts with all LEDs turned off. At the rising edge of the first PWM clock, all LEDs turn on except ones that are programmed with grayscale values of zero. The IC increments a grayscale counter at the beginning of each PWM clock cycle. Each LED stays on until the PWM grayscale counter goes above the LED's programmed PWM value. This is better explained by Figure 3, which shows waveforms and a block diagram for a simplified 3-bit PWM dimming controller. Programming the grayscale value of the red, green, and blue

Figure 2. Analog dimming vs. PWM dimming

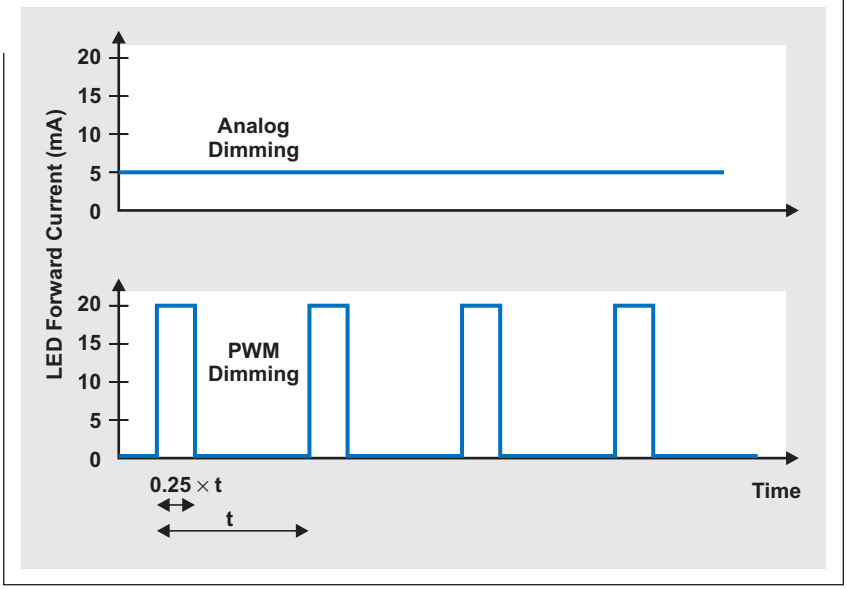


Figure 3. Orange pixel generated with 3-bit PWM dimming

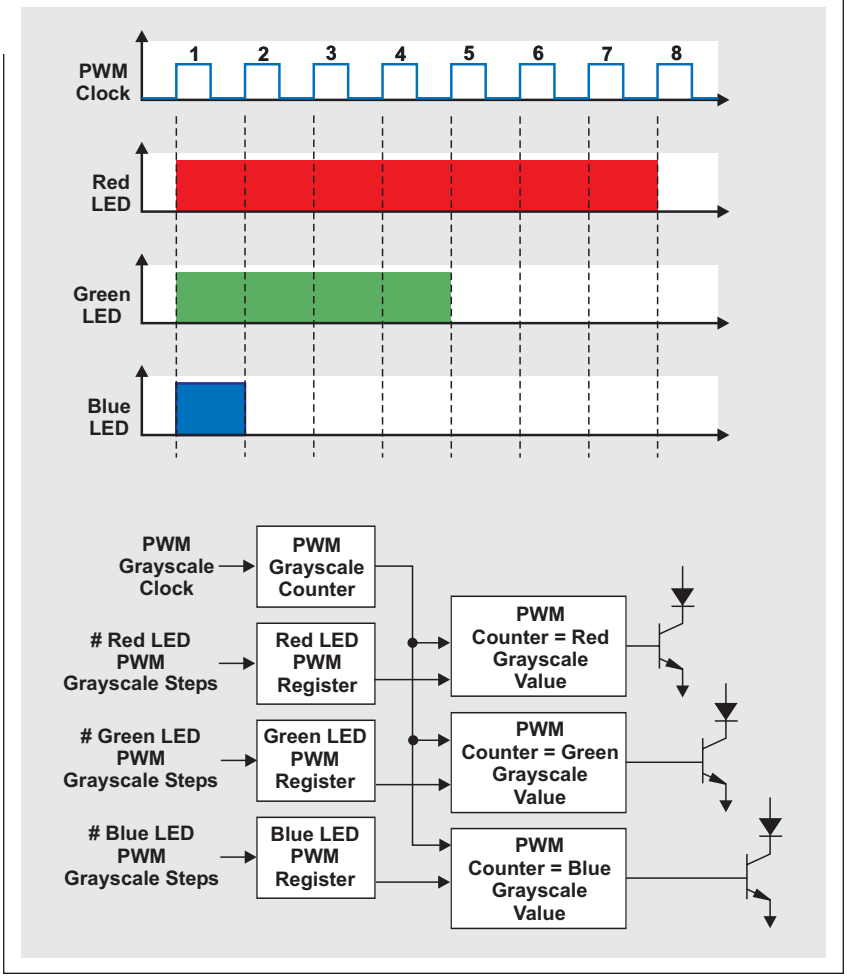
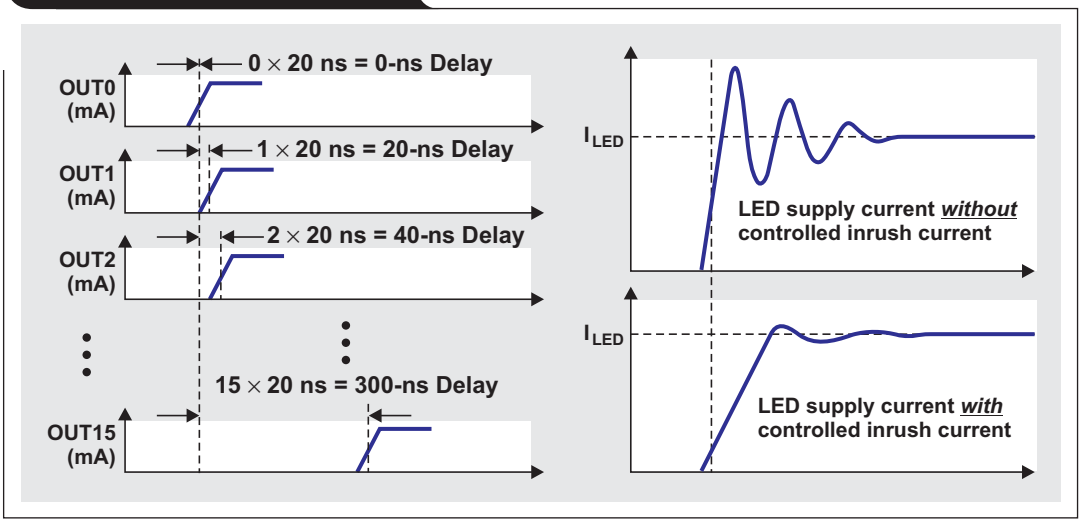


Figure 4. Inrush current control



LEDs to 7, 4, and 1, respectively, produces an orange pixel on the screen. The green LED is programmed to a grayscale value of 4. It turns on at the rising edge of the first PWM clock cycle and stays on for four full PWM clock cycles. This 3-bit PWM dimming example is capable of producing $2^3 \times 2^3 \times 2^3 = 512$ colors for each RGB pixel. Expanding this math to the TLC5940's 12-bit PWM dimming shows that this part is capable of providing a palette of $2^{12} \times 2^{12} \times 2^{12} = 68.7$ billion colors.

PWM dimming is not without its drawbacks. The discrete switching cycles can cause noise in the system. Simultaneously turning on all LEDs at the start of a video frame requires a large inrush current with a very steep rising edge. Without a method to reduce this inrush current, the higher-end LED drivers capable of driving 16 LEDs with up to 120 mA of current in each channel would require excessive input bypass capacitance. Turning on all 16 LEDs simultaneously requires the input capacitor to deliver 1.92 A within the turn-on time of the IC. The upper right graph in Figure 4 shows the ringing present during the leading edge of the current pulse when all LEDs are turned on simultaneously. Parasitic inductance on the PWM creates this noise and ringing. The TLC5940 significantly reduces the effect by staggering the turn-on of each LED. The left side of Figure 4 shows this staggered turn-on. The lower right graph in Figure 4 shows how the staggered turn-on reduces the rise time of the inrush current, which in turn reduces the ringing, the noise in the system, and the input capacitor requirement. The TLC5940 staggers LED turn-off as well; however, this is not typically needed in most systems. Figure 2 shows that turn-off is inherently staggered when the LEDs are programmed to different dimming levels.

The TLC5940 combines both PWM dimming and dot correction to produce extremely high-quality video. Dot correction produces an accurate LED color by adjusting for changes in an LED's wavelength caused by temperature variations or aging. PWM dimming then provides the shading necessary to provide thousands or millions of individual colors from three individual LEDs. PWM dimming coupled with dot correction is clearly the choice for both existing and future markets requiring high-quality color control in LED-based lighting applications.

Reference

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Document Title	TI Lit. #
1. Michael Day and Tarek Saab, "TLC5940 dot correction compensates for variations in LED brightness"	slyt225

Related Web sites

power.ti.com
www.ti.com/sc/device/TLC5940

Wide-input dc/dc modules offer maximum design flexibility

By Geoff Jones (Email: gjones@ti.com)
Marketing Manager

Introduction

When a system designer specifies a nonisolated dc/dc power module, considering the needed input voltage range is equally as important as considering the required performance attributes and features. Generally, nonisolated modules have either a narrow or a wide input voltage range. Narrow-input modules typically have a nominal input voltage of 3.3, 5, or 12 V. For systems that operate from a tightly regulated input bus—such as those that do not use battery backup—a narrow-input module is often adequate since the input remains fairly stable.

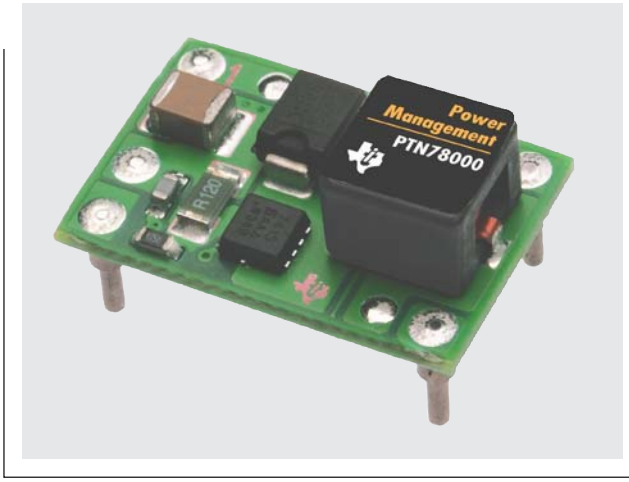
Offering greater flexibility, wide-input modules operate within a range of 7 to 36 V, which includes the popular 12- or 24-V industrial bus. This enables a single module to be used for generating multiple voltages. These modules are ideal for industrial controls, HVAC systems, vehicles, medical instrumentation, and other applications that use a loosely regulated distribution bus. In addition, systems powered by a rectifier/battery charger with lead-acid battery backup almost always require wide-input modules. System designers who choose power supplies may want to take a close look at the latest generation of wide-input dc/dc modules.

What are they?

Wide-input voltage modules are available in three basic types: positive output, positive-to-negative output, and boost output. These modules are designed to operate from a loosely regulated industrial bus input (12 or 24 V nominal) while maintaining a regulated output. Modules from the Texas Instruments (TI) PTN78 series (one of which is shown in Figure 1), for example, accept an input from 7 to 36 V and deliver an output voltage from 2.5 to 12.6 V at 1.5, 3, or 6 A. The output voltage is set with a single external resistor.

Newer wide-input modules are available in double-sided, open-frame construction to minimize cost and weight and to simplify thermal management. The modules are constructed entirely from surface-mount components (including magnetic devices) and are designed for fully automated assembly to help keep manufacturing costs as low as possible. The module's compact packaging yields significant space savings on the PC board and allows the device to be placed close to its load.

Figure 1. TI's PTN78000 module



Wide-input power modules typically integrate input and output capacitors. However, additional input or output capacitors may be needed on the host PC board if there are long input lines to the module coupled with high di/dt requirements or if very low-noise outputs are required.

Most wide-input modules feature an industrial operating temperature range of –40 to +85°C. They offer efficiencies as high as 95% and can deliver their full-rated output current at temperatures of up to 60°C with only 200 LFM of airflow.

TI's PTN78 series uses large (up to 0.08-inch-diameter) interconnect pins. The large pins help extend a module's current-carrying capacity so that it requires fewer pins, which saves board space. In the pick-and-place operation during assembly, the module's pins are placed on the PC board along with its other components. This eliminates the need for a secondary pin-attach operation, simplifying assembly.

Wide-input modules also employ built-in functionality such as soft start, on/off inhibit control, current-limit protection, overtemperature protection, and an undervoltage lockout feature to prevent system failure. The devices are available in surface-mount or horizontal through-hole packages. The newer devices like the PTN78 series are designed for RoHS and lead-free compliance.

Input voltage considerations for positive step-down modules

The majority of nonisolated wide-input modules are step-down switching regulators. To keep the output in regulation, the input voltage must exceed the output by a minimum differential voltage due to the limitations of the pulse width modulation (PWM) internal control circuit. This differential voltage can be used to define the maximum advisable ratio between the device's input and output voltages.

As an example, TI's PTN78000W accepts an input from 7 to 36 V and has an adjustable output voltage range from 2.5 to 12.6 V with a single resistor, R_{SET}. Requirements for satisfactory performance of this module are as follows:

- For output voltages lower than 10 V, the minimum input voltage is (V_O + 2 V) or 7 V, whichever is higher.
- For output voltages equal to 10 V and higher, the minimum input voltage is V_O + 2.5 V.
- The maximum input voltage is ($10 \times V_O$) or 36 V, whichever is less.

Table 1 shows the operating input voltage range for common output bus voltages.

Positive-to-negative modules

Positive-to-negative, wide-input modules are buck-boost switching regulators that accept a positive input voltage and produce a negative dc output voltage. The devices are well suited for telecom, industrial tests and measurement, instrumentation, distributed power, and general-purpose circuits.

Latest-generation modules like TI's PTN78000A provide high-efficiency, positive-to-negative voltage conversion for loads of up to 1.5 A. The module has a wide input voltage range of 7 to 29 V and an adjustable wide output voltage range of –3.3 to –15 V. The output voltage is set with a single external resistor.

To ensure that the output remains in regulation, the input voltage must not exceed the output by a maximum differential voltage. For satisfactory performance, the maximum operating input voltage is 32 – $|V_O|$. As an example, Table 2 gives the operating input voltage range for common output bus voltages.

Some operational amplifiers require positive and negative operating voltage. Figure 2 shows a PTN78000A module converting a +12-V input to a regulated –5-V output to an op amp.

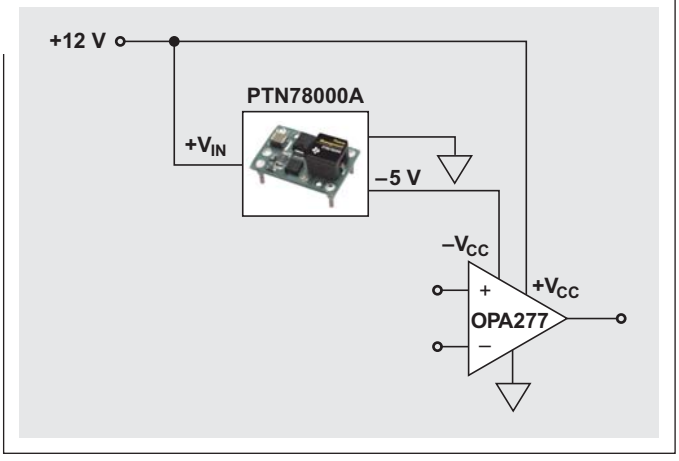
Table 1. PTN78000W standard R_{SET} values for common output voltages

REQUIRED V_O (V)	STANDARD R_{SET} VALUE	ACTUAL V_O (V)	OPERATING V_I RANGE (V)
2.5	Open	2.5	7 to 25
3.3	78.7 kΩ	3.306	7 to 33
5	21 kΩ	4.996	7 to 36
12	732 Ω	12.002	14.5 to 36

Table 2. Positive step-down module standard R_{SET} values for common output voltages

REQUIRED V_O (V)	STANDARD R_{SET} VALUE	ACTUAL V_O (V)	OPERATING V_I RANGE (V)
–15	100 Ω	–14.997	9 to 17
–12	2 kΩ	–12.006	9 to 20
–5	28.7 kΩ	–5.000	9 to 27
–3.3	221 kΩ	–3.303	9 to 28.7

Figure 2. Positive-to-negative voltage conversion in an operational amplifier application



Boost modules

Boost modules provide high-efficiency, step-up voltage conversion. They generate a stable output voltage that can be adjusted by an external resistor divider. For maximum power efficiency, the integrated devices use a switching rectifier based on a PWM controller.

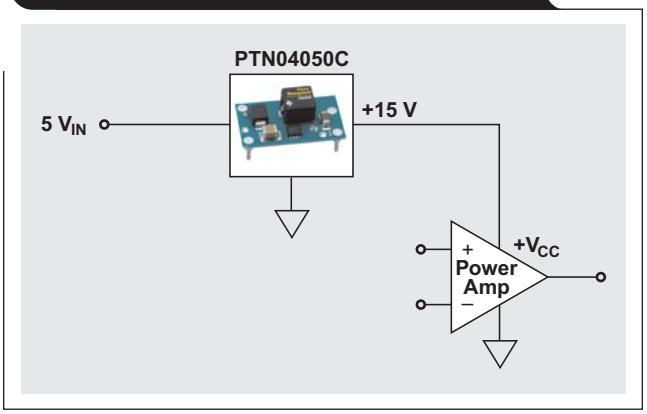
Table 3. Boost module standard R_{SET} values for common output voltages

REQUIRED V_O (V)	STANDARD R_{SET} VALUE	ACTUAL V_O (V)	OPERATING V_I RANGE (V)
5.0	Open	5.00	2.9 to 4.5
9.0	4.53 kΩ	9.01	2.9 to 5.5
12.0	1.33 kΩ	12.03	2.9 to 5.5
15.0	60.4 kΩ	14.99	2.9 to 5.5

TI's PTN04050C is a boost module designed for use with 3.3- or 5-V bus systems that require an additional regulated 5 to 15 V with up to 12 W of output power. The output voltage is set with a single external resistor and may be set to any value within the 5- to 15-V range. The output voltage can be as little as 0.5 V higher than the input, allowing an output voltage of 5 V with an input voltage of 4.5 V. Table 3 shows standard resistor values for several common output voltages, along with the actual output voltage that the value provides.

Target applications for boost modules include telecom, industrial tests and measurement, instrumentation, distributed power, and general-purpose circuits. With the ability to operate from 3.3- or 5-V bus systems, a boost module can be used together with a positive step-down module to create plus and minus voltage rails required by many analog ICs such as op amps and data converters.

Figure 3. Boost module providing step-up voltage conversion for a power amplifier



The module in Figure 3 is shown operating from a +5-V input and producing a +15-V output to a power amplifier.

What's available?

The number of wide-input modules introduced to the marketplace is growing. The wide product choice facilitates precise application matching and simplifies migration to higher-current modules when needed. Table 4 lists some of the products available from TI.

Table 4. TI's wide-input, nonisolated dc/dc modules

DESCRIPTION	MODEL	INPUT VOLTAGE (V)	OUTPUT VOLTAGE (V)	OUTPUT CURRENT	PACKAGE
Positive Step-Down	PTN78000W/H	7 to 36	2.5 to 12.6/12 to 22	1.5 A	SMD, TH
	PTN78060W/H	7 to 36	2.5 to 12.6/12 to 22	3 A	SMD, TH
	PTN78020W/H	7 to 36	2.5 to 12.6/12 to 22	6 A	SMD, TH
Positive to Negative	PTN04050A	+2.9 to +7	–3.3 to –15	1 A (6 W)	SMD, TH
	PTN78000A	+7 to +29	–3.3 to –15	1.5 A (9 W)	SMD, TH
	PTN78060A	+9 to +29	–3.3 to –15	3 A (15 W)	SMD, TH
	PTN78020A	+9 to +29	–3.3 to –15	4 A (25 W)	TH
Positive Boost	PTN04050C	2.9 to 5.5	5 to 15	1 A (12 W)	SMD, TH

The ultimate in design flexibility

TI's wide-input modules provide system designers increased migration-path flexibility to accommodate evolving system power requirements. The wide-input range and output voltage combinations eliminate redesign of an existing power architecture when voltage requirements change. The following system examples show that wide-input modules are suitable for a variety of applications.

Vending machines

Wide-input modules are ideal for vending-machine applications. Vending machines connected to a wireless network help vending-machine managers perform remote diagnostics, monitor inventory levels, schedule service calls, and track real-time sales through a wireless interface. Sending data via a cell phone within each vending machine provides an instant snapshot of the user's entire vending system.

As shown in Figure 4, the wide-input modules accept the loosely regulated output (18 to 32 V) from the vending machine's inexpensive ac/dc converter. One module is providing a 12-V/1.5-A output for the cell phone; the other is providing a 5-V/3-A output for the displays and logic PC board. Modules that can operate in an environment of –40 to +85°C are ideal for vending equipment that is placed outdoors and are effective for embedded applications in industrial and other challenging environments.

Security cameras

Wide-input modules simplify power management in security cameras. Figure 5 shows a typical power-management circuit powered by a wall-mount ac/dc adapter. A 24-V battery is used to provide emergency backup power. Because of the wide output voltage tolerance of the 24 V from the ac/dc adapter, the circuit requires dc/dc modules capable of operating over a wide input voltage range.

The wide-input modules in Figure 5 are shown operating from a 24-V input. One module is providing a 12-V output to a motor control circuit for the camera's focus and zoom

Figure 4. Vending-machine application

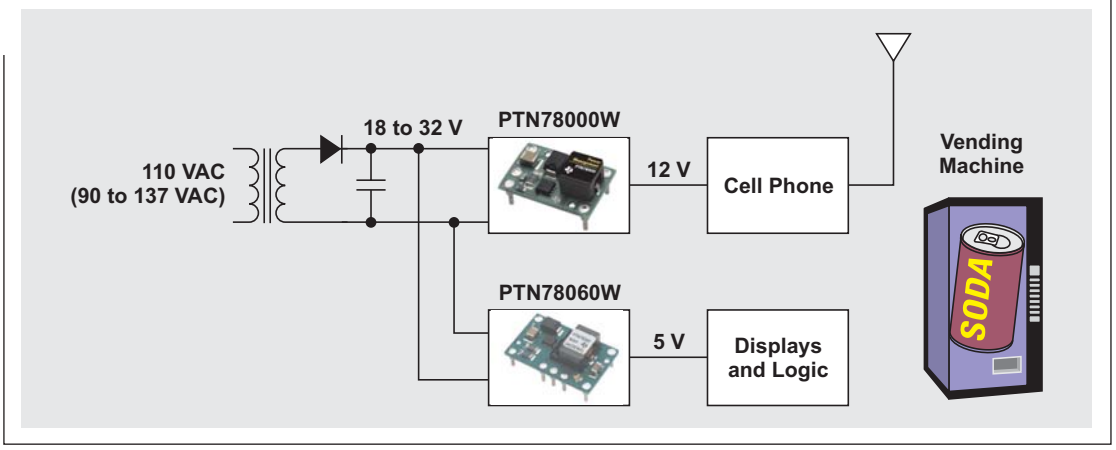


Figure 5. Security-camera application

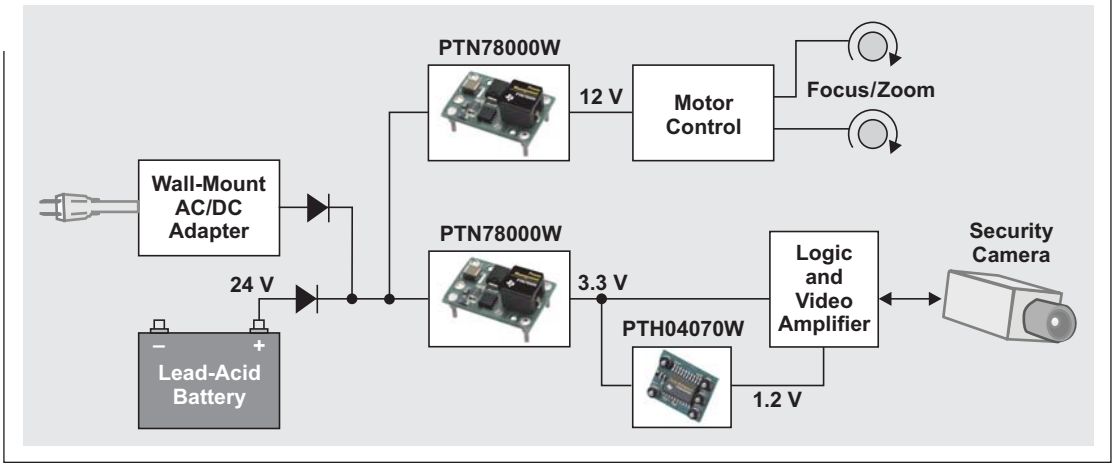
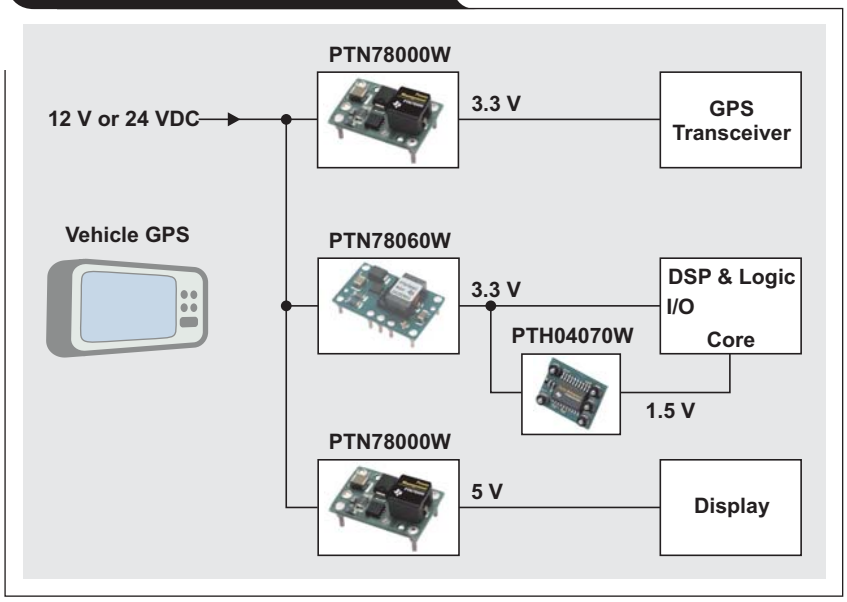


Figure 6. Vehicle GPS application



functions. The other module is providing a 3.3-V output to a video amplifier and a nonisolated module, which is producing a 1.2-V output for a DSP's core voltage.

Vehicle GPS systems

Wide-input modules provide high-efficiency, step-down voltage conversion for a wide variety of vehicle GPS navigation systems. Aftermarket dash-mount GPS systems such as those from Garmin, Magellan, and other manufacturers are popular applications. There are also marine GPS systems and golf carts that use GPS-based range finders. More advanced applications include commercial truck and rail-car monitoring systems. These small, self-contained units, about the size of a paperback novel, have no display. They consist of a black box that enables a central tracking center to monitor the position of entire fleets or rail cars.

As shown in Figure 6, vehicle GPS systems need to be powered by either 12 V (in a car) or 24 V (in a truck or bus). One module provides a 3.3-V/1.5-A output to a GPS transceiver and a 5-V/1.5-A output to the LCD display. The other module provides a 3.3-V/3-A output for the DSP's I/O voltage. It also powers a nonisolated module that delivers a 1.5-V/3-A output for the core voltage.

Purchasing flexibility

The commercial availability of wide-input modules offers purchasing flexibility. Leading distributors provide samples and production quantities in volume for quick design qualification or last-minute changes. Numerous output voltage and current combinations as well as package options are offered.

Large OEMs prefer to work with a small base of approved suppliers to keep costs down. With a wide input voltage range and adjustable output, one module can be used in a variety of applications. Using fewer modules reduces the number of parts that OEMs must keep in stock.

Summary

System designers are employing increasing numbers of nonisolated dc/dc power modules in their designs. Wide-input, nonisolated modules provide precise power at the load and a great deal of flexibility, helping system designers cope with changes in power requirements. These modules provide all the active functions for local dc/dc conversion with fast transient response and accurate regulation in the smallest possible PC board area. Their wide operating voltage range makes them ideal for industrial, battery-powered, and advanced computing and server applications that use a loosely regulated distribution bus.

Related Web sites

power.ti.com
www.ti.com/sc/device/*partnumber*
Replace *partnumber* with PTH04070W, PTN04050A, PTN04050C, PTN78000A, PTN78000H, PTN78000W, PTN78020A, PTN78020H, PTN78020W, PTN78060A, PTN78060H, or PTN78060W

Powering today's multi-rail FPGAs and DSPs, Part 2

By Jeff Falin (Email: j-falin1@ti.com)
Power Management Products/Portable Power dc/dc Applications

Introduction

Most electronics have one or more digital processing ICs, such as FPGAs or DSPs, that require multiple power-supply rails. There are various options to consider and potential pitfalls to avoid in powering these digital ICs. This article, Part 2 of a two-part series, provides recommendations and guidance for developing a power solution for multi-rail applications where the input power supply voltage is assumed to be equal to or greater than the system rail voltage (e.g., 12, 5, or 3.3 V). While Part 1 (see Reference 1) discussed system-level concerns such as the power budget and sequencing options, this article focuses on how to choose between the types of point-of-load (POL) dc/dc converters and how to design them to meet dc accuracy, start-up, and transient requirements.

Review of step-down dc/dc converter topologies

There are two types of step-down or "buck" POL dc/dc converters: linear regulators and inductor-based switching regulators. Figure 1 shows the functional diagram of a linear regulator.

The primary benefit of linear regulators is the low cost of their ICs, design time, and board area, since they have an internal switch and need only an input and output capacitor. In addition, linear regulators provide a clean, low-noise output voltage. Their primary drawback is low efficiency, equal to V_{OUT}/V_{IN} at heavy load, resulting in a power dissipation of $(V_{OUT}–V_{IN}) \times I_{OUT}$. Power is lost as heat that must be dissipated by the regulator's package and/or external heat sink. Since the minimum input voltage for most regulators currently on the market is 1.8 to 2.7 V, linear regulators are best suited for higher-voltage rails with lower load currents. A second drawback seen in the lowest-cost, feature-less regulators is fast, uncontrollable startup, which will be discussed later in this article.

Figure 1. Linear regulator

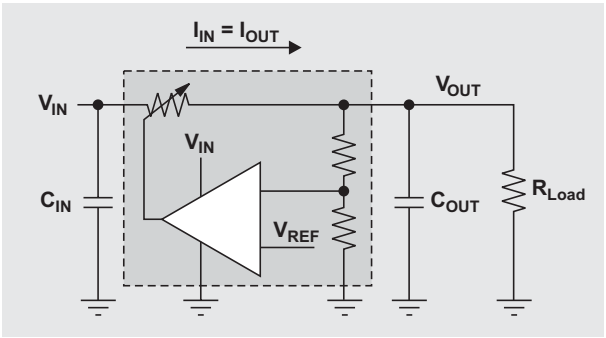
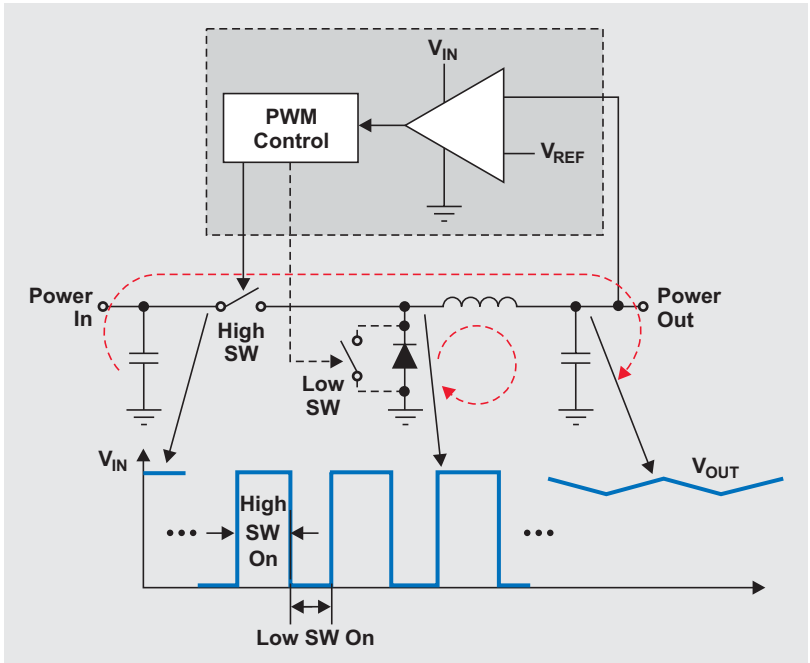


Figure 2 shows a block diagram of a synchronous buck switching regulator. Buck switching regulators use two switches to generate a pulse train with a duty cycle equal to V_{OUT}/V_{IN}. The regulator's feedback control loop modulates either the pulse width of a fixed-frequency pulse train or both the pulse frequency and width to maintain regulation as the load varies, hence the term "pulse width modulation" (PWM). The square-wave pulse train is then filtered by an inductor and capacitor (the LC output filter) to provide a dc output voltage with a triangular-shaped output voltage ripple.

The converter's topology, whether with fixed- or variable-frequency PWM, influences output ripple. The control loop for fixed-frequency PWM converters uses an error amplifier with a negative feedback loop that regulates the output voltage across a load range by modulating the pulse width.

Figure 2. Synchronous buck switching regulator



The output ripple of these regulators is formed by the product of the inductor ripple current and the output capacitor's equivalent series resistance (ESR). Thus, choosing a larger inductor than necessary and a low-ESR output capacitor minimizes output ripple. However, low-ESR output capacitors make the feedback loop more difficult to compensate. Fortunately, power IC manufacturers provide power-supply design software that greatly reduces the design time for fixed-frequency PWM converters. The control loop for most variable-frequency converters consists of a comparator, with either time or voltage hysteresis, that turns the switch on or off if the output voltage goes respectively below or above the reference voltage. These hysteretic converters require less design time than fixed-frequency converters due to their simplified control loop. In addition, since the comparator turns the switch on almost immediately after the output falls below the comparator's reference voltage, a hysteretic converter may respond faster to current increases (transients) than the fixed-frequency converter with a finite-bandwidth control loop. However, a hysteretic converter requires a minimum output ripple to operate.

Compared to linear regulators, switching converters have much higher efficiency (85 to 95% typically), but the cost of their ICs, support components, design time, and board area is usually higher. Another drawback of switching regulators compared to linear regulators is their switching noise (e.g., EMI) and output ripple. Switching noise can be minimized through careful component selection, such as shielded inductors and low-ESR output capacitors, and through proper board layout. Hysteretic converters produce output voltage ripple and radiated emissions at variable switching frequencies, which may be difficult to filter. However, when either the output current or the input-to-output differential is large or the input supply has limited power—e.g., an inexpensive wall brick—only a switching converter can provide high enough efficiency to minimize the power lost through heat.

Step-down switching converters are available in various levels of integration. Drop-in modules have limited design flexibility and tend to cost more; but they require the least amount of design time, needing only an input and output capacitor. At the other extreme are controllers that require external switches as well as the inductor, filter capacitors, and compensation components. They have the most design flexibility and, with enough design effort, can be the most cost-effective solution; but they usually consume the largest amount of board space. In between are the integrated FET buck converters that require less board area, have somewhat less design flexibility, and vary in total solution cost compared to controllers. A synchronous converter/controller uses transistors for both switches and therefore is typically more efficient than a converter that uses a diode for the low-side switch, especially when the output voltage is below 2 V. Therefore, the choice between a linear regulator, a fixed-frequency controller/converter, or a hysteretic controller/converter depends on application requirements as well as on balancing efficiency, cost, and size.

Converter output voltage accuracy

The dc tolerance of most FPGA and DSP core and I/O rails is still ±5%; however, tolerances for some core rails as well as power rails for other ICs have dropped to ±3%. The lower end of the tolerance range (–5 or –3%) is typically the minimum voltage at which some performance standard (e.g., DSP operating speed) is guaranteed for a particular IC. The upper end of the range may be close to the IC's absolute maximum operating voltage. Understanding how to compute the dc tolerance for a power supply is critical not only to guarantee performance but also for system reliability. The dc tolerance does not include dips due to load-step transients. A load-step transient occurs when a digital device being powered by the POL converter increases its load-current demand very quickly. The factors that contribute directly to the dc tolerance for a power supply are the reference voltage tolerance, the feedback resistor tolerance, and the IC's line and load regulation specifications. As an example, an excerpt from the datasheet of the TPS54310 adjustable buck switching converter (see Reference 2) is shown in Figure 3.

Figure 3. Excerpt from TPS54310 datasheet

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CUMULATIVE REFERENCE					
V_{ref} Accuracy		0.882	0.891	0.900	V
REGULATION					
Line regulation (1) (3)	I_L = 1.5 A, f_s = 350 kHz, T_J = 85°C			0.07	%/V
	I_L = 1.5 A, f_s = 550 kHz, T_J = 85°C			0.07	
Load regulation (1) (3)	I_L = 0 A to 3 A, f_s = 350 kHz, T_J = 85°C			0.03	%/A
	I_L = 0 A to 3 A, f_s = 550 kHz, T_J = 85°C			0.03	

(1) Specified by design
(2) Static resistive loads only
(3) Specified by the circuit used in Figure 10 of TPS54310 datasheet.

Table 1 computes the percentage that the 1.2-V ±5% output can dip during a load transient and still be within regulation, assuming a 5-V ±10% input rail and a 100-mA to 3-A dc output load range. Line regulation and load regulation specifications vary per device, even if those devices are from the same power IC manufacturer, so care must be taken when they are used in a calculation. Most recent converters have voltage feedforward, virtually eliminating the output voltage's dependence on input voltage and making line regulation almost negligible. Load regulation is a function of the power IC's loop gain; higher loop gain gives better load regulation. Note that many converters with fixed output voltages and internal compensation have better output voltage accuracy because the output voltage can be set by trimming the internal feedback resistors.

Table 1. Converter accuracy

CONTRIBUTING FACTOR	COMPUTATION	DROOP (%)
V_{REF} accuracy		–1
1% external feedback resistors	2 x (1–V_{REF}/V_{OUT}) x TOL	–0.5
Worst-case output ripple	Design for $V_{OUT(PP)}$ < 1% x V_{OUT}	–0.5
Line regulation	(0.07%/V) x (5.5 – 4.5) %	–0.07
Load regulation	(0.03%/A) x (3 – 0.1) A	–0.087
Total		–2.157
Remainder for load-transient dips	(5% – 2.157%)	2.843

In the example in Table 1, only 2.843% of 1.2 V or 34.1 mV is available for load transient dip before the output voltage will fall below the –5% minimum tolerance. The capacitor(s) on the power rail must be able to supply this load current until the converter can respond, or the voltage will fall below regulation. Capacitors of various sizes and with low series resistance and inductance are paralleled for handling load transients. Sizing of the capacitors for this "decoupling network" and how that affects converter response time is discussed later in this article.

Implementing a controlled monotonic rise of the power rail

The final recommended power-supply design practice to be discussed is monotonic rise at startup, as shown in the top graph of Figure 4.

Figure 4. Start-up voltage and current

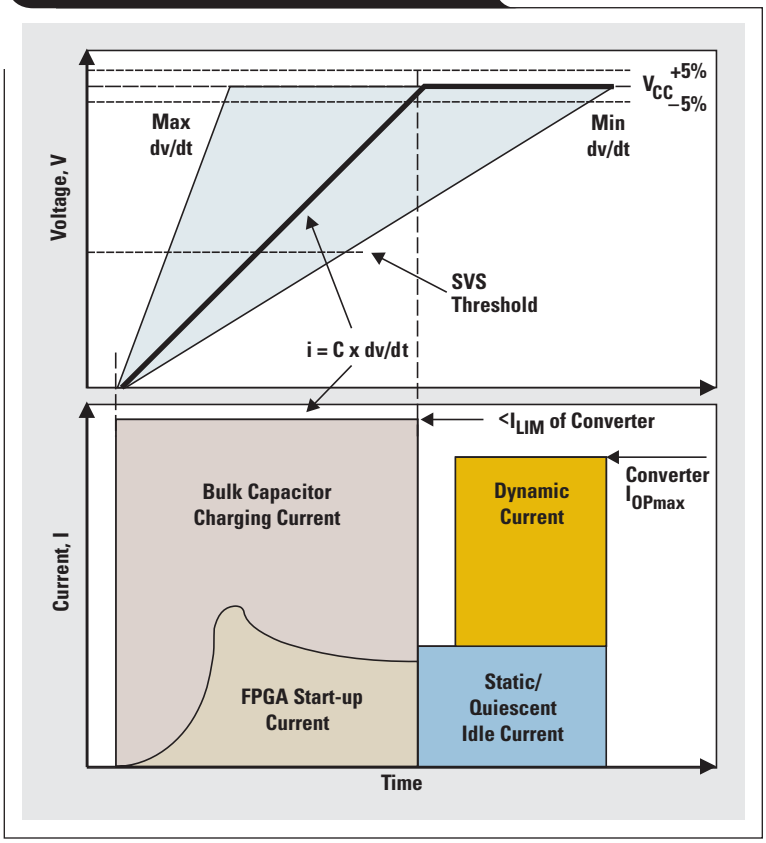
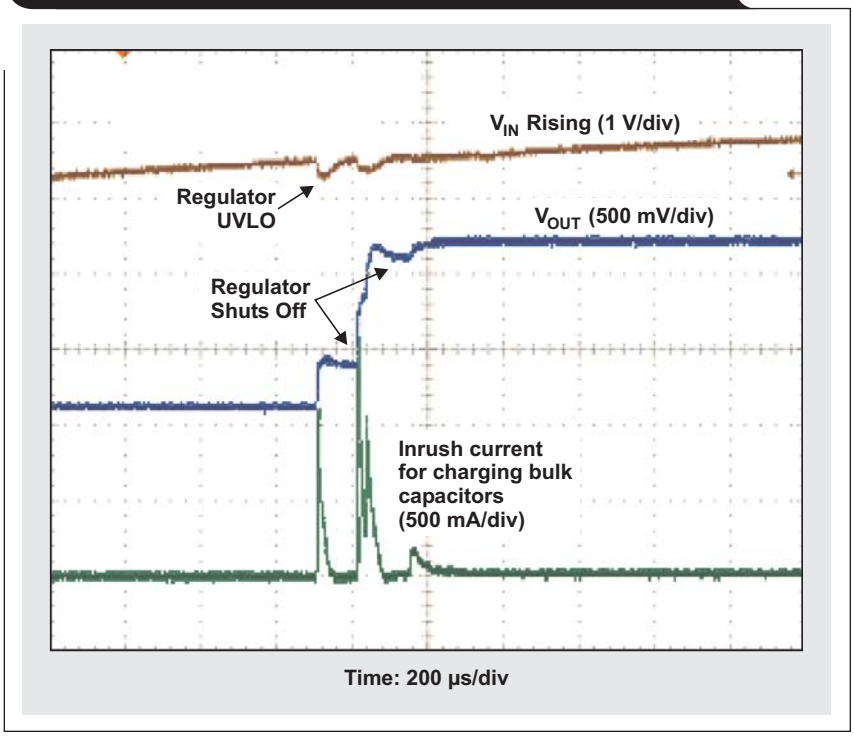


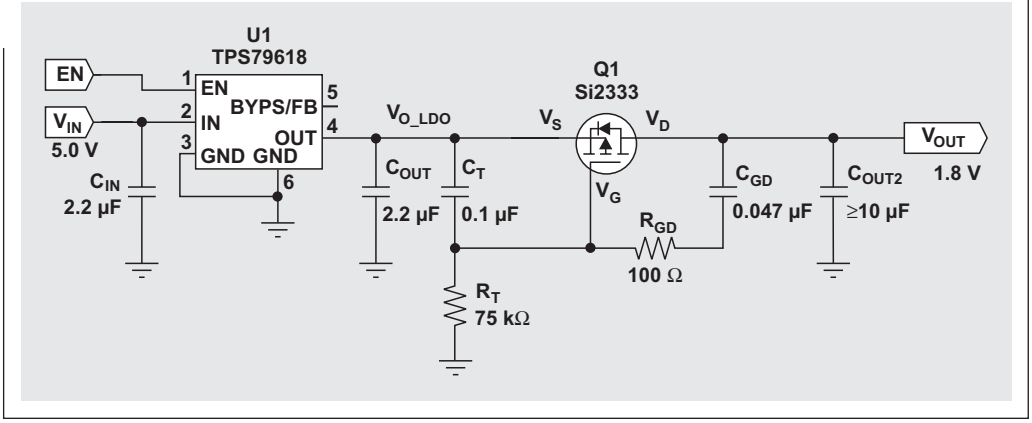
Figure 5. Linear regulator driving a large capacitive load



If the bulk capacitance is too large, thereby forcing the POL converter into current limit during startup, there is a risk of the converter cycling in and out of thermal shutdown and thereby never reaching regulation. A more common start-up problem for fast-starting linear regulators occurs when their input supply gets pulled down at startup, temporarily tripping the regulator's undervoltage lockout (UVLO) until the input capacitor recharges. This causes the regulator to repeatedly turn off briefly and then back on, resulting in the output voltage appearing to oscillate and/or finally ratcheting up to the final voltage. Figure 5 shows an example of a fast-starting linear regulator being powered from a bench supply, pulling the input supply down, tripping UVLO and turning off, repeating the same cycle, then finally reaching its regulated output voltage.

Few linear regulators have a controllable soft start. At startup, they provide current up to their current limit to charge the output capacitance until they either thermally limit themselves or pull down the input rail as shown in Figure 5. All switching converters have some sort of soft start, whether internally fixed or externally adjustable. A FET following any dc/dc converter can be used as a current-limiting switch to provide a soft start. Figure 6, taken from Reference 3, shows such an application; and Figure 7, also taken from Reference 3, shows the results of soft starting.

Figure 6. Linear regulator with FET following to provide soft start



There are two methods that linear regulators and switching converters commonly use to implement a soft start: reference voltage-controlled or current-limit-controlled. In both, a small external capacitor (in the picofarads to 1-µF range) controls the soft-start timing. A voltage-controlled soft start is usually implemented by slowly ramping up the reference voltage. Since the feedback loop forces the converter to provide enough current so that the output voltage follows the reference voltage, the output voltage ramps proportional to the soft-start capacitor that is providing the reference voltage during startup. A simple timing equation determines the size of the external capacitor needed to set the dv/dt of the output voltage. Assuming that the inrush current is predominantly for charging bulk capacitors, C_{Bulk}, the inrush current will be fixed, as shown in Figure 4, at $i = C_{Bulk} \times dv/dt$. Ratiometric sequencing, discussed in Part 1 of this series, can be implemented by having two converters with this type of soft start share the same soft-start capacitor. When using a current-limit-controlled soft start, the converter either slowly ramps or incrementally steps up the current limit to the maximum. The converter then looks like a current source, providing a slowly increasing current to the load. The voltage feedback loop still tries to provide the desired output voltage, so the converter provides as much current as the current limit (and any thermal protection) will allow. The output voltage's exact ramp rate, dv/dt, varies as a function of the absolute value of the output voltage (i.e., a 1.2-V rail will ramp more quickly than a 3.3-V rail), the resistive and capacitive loading on the rail, and the converter's final current-limit setting.

Dealing with load-step transients

All POL dc/dc converters have a finite transient response time, whether it's the loop bandwidth of the traditional PWM converter or the fixed on/off times of the hysteretic converter. Figure 8 shows the response of a low-current linear regulator to a change in the output load current—for example, a line of code that causes a DSP to perform complex computations.

Figure 7. Linear regulator with FET following to provide soft start

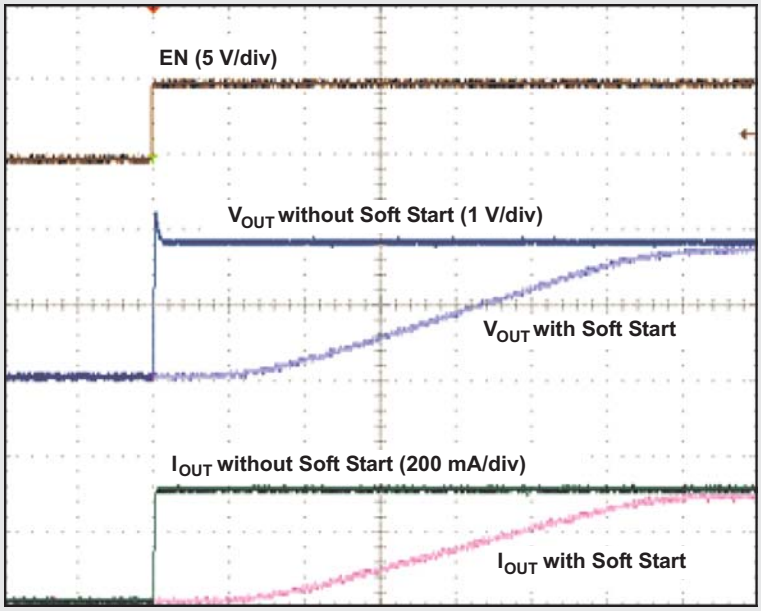


Figure 8. Example load-step transient response

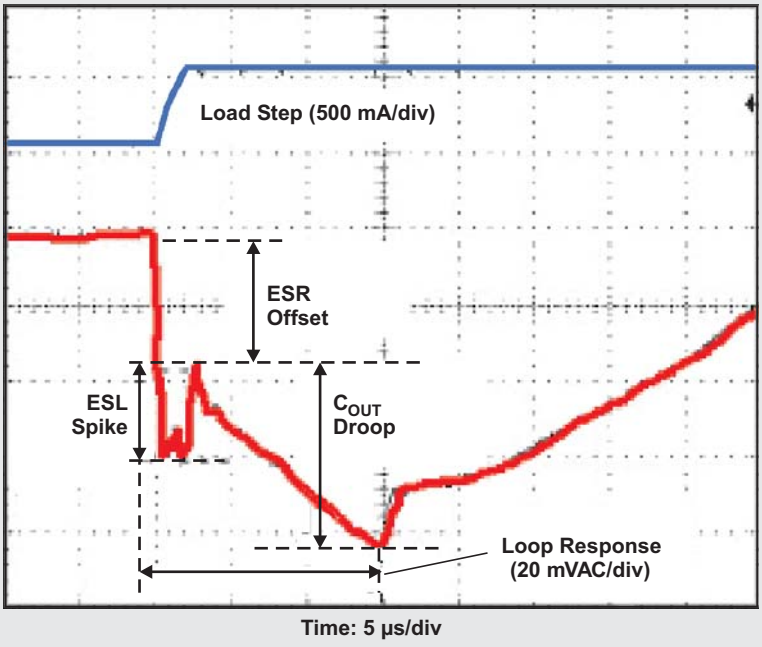
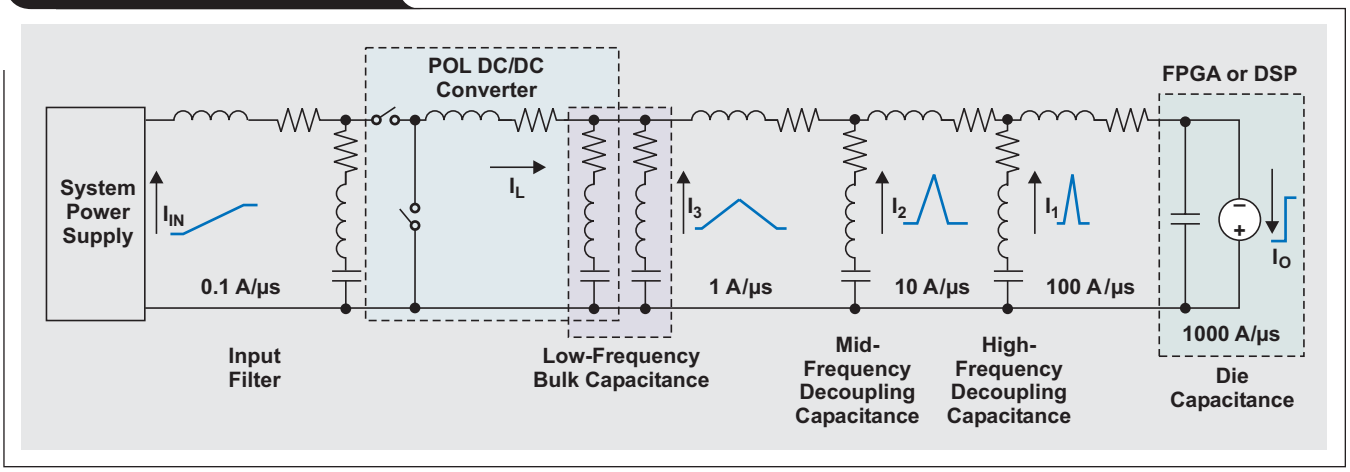


Figure 9. Decoupling network



Using output capacitors with low ESR and equivalent series inductance (ESL) helps to minimize the transient droop. However, additional capacitance is almost always required at the power rail's output and localized bypass capacitance to assist the converter in handling the step transient. Figure 9 shows load-step-transient propagation and its suppression by a decoupling network. The various-sized capacitors suppress the different frequency components of the load-step transient so that the POL converter, and ultimately its input power supply, have to support only the small, low-frequency component of the load step. For example, if the FPGA or DSP gives a load step of 1000 A/µs, then the decoupling network suppresses the transient so that the converter has to respond only to a 1-A/µs transient.

Small capacitors (in the picofarads to 1-µF range) handle the high-frequency component of the load step. Capacitors from 1 to 22 µF handle the mid-frequency component, and low-ESR bulk capacitors from 47 to 1000 µF handle the low-frequency component. A common method for optimizing the decoupling network (i.e., minimizing the amount of capacitance added) is the target-impedance method, which is explained more fully in Reference 4. This method requires that the designer know the worst-case load-step transient of the device being powered (e.g., from 200 mA to 2.2 A in 0.5 µs or 4 A/µs for 10 µs) and have some idea of the transient-response capabilities of the POL converter. If the POL converter is not close to the digital IC being powered and/or the board layout requires that the power rail use small traces and/or vias to get to the load, then approximations of the board resistance and inductance may be necessary for the model, as illustrated in Figure 9.

For most FPGA and DSP applications, the worst-case load-step transient is rarely known and it is simpler to use rules of thumb to design the decoupling network. For example, it is not uncommon to allocate a certain percentage of each capacitor type (high-, mid-, and low-frequency) per the number of power pins used in total or per section of the digital IC. While effective, this method tends to overdesign the decoupling network, underutilizing the linear regulator's or switching converter's transient-response capabilities and consuming board space for extra capacitance.

With rule-of-thumb methods, the decoupling network and POL converter are designed independently. This poses a risk that the POL converter may become unstable due to the additional capacitance of the decoupling network; so it is critical that the converter be compensated for the total capacitance at its output. Texas Instruments has reference documents and design software at power.ti.com/swift to assist with converter design and compensation. Artificially applying a load-step transient to the output of the converter and observing the ringing (oscillations) on the output voltage as the converter responds to the transient is another way to determine stability of the converter. As a rule of thumb, if the converter has over three oscillations before settling, it is considered on the verge of being unstable (underdamped). A slow response with no ringing or overshoot is considered to be very stable (overdamped).

PC processors can have multiple load-step transients in the 1000-A/µs range and so require both a fast transient POL converter and a large decoupling network. To reduce the cost of the decoupling network and minimize the

board space it uses, PC motherboard manufacturers now use the target-impedance method or a similar method to minimize the number of capacitors and to take full advantage of the transient capabilities of the dc/dc converter. Individual FPGA and DSP applications are currently lower-power and slower-switching compared to PC processors. So, until either FPGAs or DSPs generate load steps similar to PC processors or the size or cost of the decoupling network becomes too large, a rule-of-thumb approach to sizing the decoupling network is a reasonable compromise between optimal design and fast time to market.

Conclusion

Choosing the right power-supply solution for multi-rail applications is more than balancing size, efficiency, and cost between a linear regulator and the various types of switching converters. Issues such as power-up sequencing and start-up current management must also be considered. In addition, the converter will most likely need the help of decoupling capacitors to maintain regulation during load-step transient events.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	**TI Lit. #**
1. Jeff Falin, "Powering today's multi-rail FPGAs and DSPs, Part 1,"	slyt232
2. "3-V to 6-V Input, 3-A Output Synchronous-Buck PWM Switcher with Integrated FETs (SWIFT™)," TPS54310 Datasheet	slvs412
3. Jeff Falin, "Monotonic, Inrush Current Limited Start-Up for Linear Regulators," Application Report	slva156
4. "Practical Considerations in Current Mode Power Supplies," Application Report	slua110

Related Web sites

power.ti.com
power.ti.com/swift
www.ti.com/sc/device/TPS54310
www.ti.com/sc/device/TPS79618

Device spacing on RS-485 buses

By Kevin Gingerich (Email: k-gingerich@ti.com)
High-Performance Linear/Interface

The RS-485 bus is a distributed parameter circuit whose electrical characteristics and responses are primarily defined by the distributed inductance and capacitance* along the physical media. The media is defined here as the interconnecting cable(s) or conducting paths, connectors, terminators, and RS-485 devices added along the bus. The following analysis derives a guideline for the amount of capacitance and its spacing that can be added to the bus.

For a starting approximation, the characteristic transmission line impedance at any cut point in the unloaded RS-485 bus is defined by the following equation, where L is the inductance per unit length and C is the capacitance per unit length.

$$Z = \sqrt{\frac{L}{C}}$$

As capacitance is added to the bus in the form of devices and their interconnections, the bus impedance is lowered to Z′, causing an impedance mismatch between the media and the loaded section of the bus.

As the input signal wave arrives at this mismatch in impedance, an attenuation (or amplification) of the signal will occur. The signal voltage at an impedance mismatch is $V_{L1} = V_{L0} + V_{J1} + V_{R1}$, where V_{L0} is the initial voltage, V_{J1} is the input signal voltage, and V_{R1} is the reflected voltage. The voltage reflected back from the mismatch is $V_{R1} = \rho_L \times V_{J1}$, where

$$\rho_L = \frac{Z' - Z}{Z' + Z}$$

and is the coefficient of reflection commonly used in transmission line analysis. The voltage equation can now be written as $V_{L1} = V_{L0} + V_{J1} + \rho_L \times V_{J1}$.

With fast transfer rates and electrically long** media, it becomes essential to achieve a valid input voltage level on the *first* signal transition from an output driver anywhere on the bus. This is called incident-wave switching. If incident-wave conditions are not achieved, reflected-wave switching must be used. To achieve a valid logic voltage level, reflected-wave switching depends upon reflected energy occurring some time after the first transition arrives.

Assuming that the bus is terminated at both ends with the nominal media impedance and no fail-safe offset, an RS-485 driver will create a high-to-low voltage change from at least 1.5 V to –1.5 V, or a V_{J1} of –3 V. The signal voltage at the load, V_{L1}, should go below the minimum receiver input voltage threshold of –0.2 V.

$$-0.2 > 1.5 + (-3) + \rho_L \times (-3)$$

$$\rho_L > \frac{-0.2 - 1.5 + 3}{-3} = -0.43$$

Now we can solve for Z′:

$$\rho_L = \frac{Z' - Z_0}{Z' + Z_0} > -0.43$$

$$Z' - Z_0 > -0.43(Z' + Z_0)$$

$$Z'(1 + 0.43) > Z_0(1 - 0.43)$$

$$Z' > 0.4Z_0$$

If the loaded bus impedance is no less than $0.4Z_0$, the minimum threshold level should be achieved on the incident wave under all allowed cases.

What bus configuration rules should be used to keep the loaded bus impedance above $0.4Z_0$?

In the derivation of the minimum loaded-bus impedance, we treat the addition of devices and their capacitances in a distributed model. As such, the loaded-bus impedance can be approximated by

$$Z' = \sqrt{\frac{L}{C + C'}}$$

where C′ is the added capacitance per unit length. If we knew the distributed inductance and capacitance of the media, we could calculate Z′ directly. Unfortunately, manufacturers do not commonly specify these; but they generally do specify the characteristic impedance, Z_0, and the capacitance per unit length, C. With these and the relationship

$$Z_0 = \sqrt{\frac{L}{C}}$$

we can solve for L, as $L = Z_0^2 C$. Then we can substitute into the equation for Z′ and simplify:

$$Z' = \sqrt{\frac{Z_0^2 C}{C + C'}} = Z_0 \sqrt{\frac{C}{C + C'}}$$

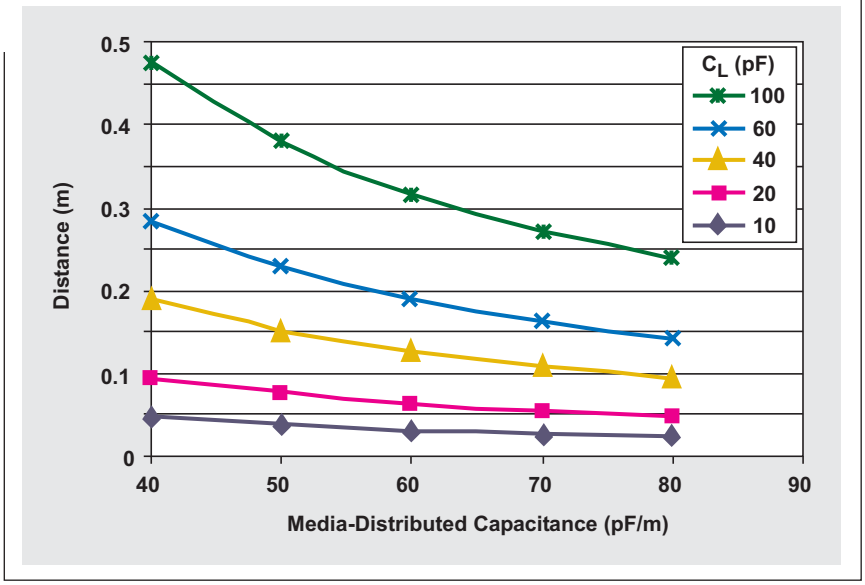
*All capacitances are differential in this article. The differential is approximately one-half of the single-ended capacitance.

**"Electrically long" is defined here as

$$\tau > \frac{t_{10\text{-}90\%}}{3}$$

where τ is the one-way time delay across the bus and $t_{10\text{-}90\%}$ is the 10-to-90% transition time of the fastest driver output signal.

Figure 1. Minimum RS-485 device spacing with device and media capacitance



C′ is the distributed device capacitance (C_L) divided by the distance (d) between devices:

$$C' = \frac{C_L}{d}$$

Substituting this into the equation, we can solve for d:

$$Z' = Z_0 \sqrt{\frac{C}{C + \frac{C_L}{d}}}$$

$$\left(\frac{Z'}{Z_0}\right)^2 = \frac{C}{C + \frac{C_L}{d}}$$

$$C\left(\frac{Z_0}{Z'}\right)^2 = C + \frac{C_L}{d}$$

$$d = \frac{C_L}{C\left[\left(\frac{Z_0}{Z'}\right)^2 - 1\right]}$$

Now substituting our minimum Z′ of $0.4Z_0$ gives us d in meters (if C is pF/m) or feet (if C is pF/ft):

$$d > \frac{C_L}{C\left[\left(\frac{Z_0}{0.4Z_0}\right)^2 - 1\right]}$$

$$d > \frac{C_L}{5.25C}$$

We now have a relationship for the minimum device spacing as a function of the distributed media and lumped-load capacitance. Figure 1 shows this relationship graphically.

Load capacitance includes contributions from the RS-485 line circuit bus pins, connector contacts, printed-circuit-board traces, protection devices, and any other physical connections as long as the distance from the bus to the transceiver is electrically short. RS-485 5-V transceivers, such as the SN65HVD1176, have a capacitance of 7 pF. Transceivers with a 3-V supply, such as the SN65HVD11, have about twice the capacitance that 5-V transceivers have at 16 pF. Board traces add about 0.5 to 0.8 pF/cm depending upon their construction. Connector and suppression device capacitance can vary widely. Media-distributed capacitance ranges from 40 pF/m for low-capacitance, unshielded, twisted-pair cable to 70 pF/m for backplanes.

This derivation gives guidelines for spacing of RS-485 nodes along a bus segment based upon the lumped-load capacitance. The method is equally applicable to other multi-point or multidrop buses, such as CAN, RS-422, or M-LVDS, with appropriate adaptation of the parameter values.

Related Web sites

interface.ti.com
www.ti.com/sc/device/SN65HVD11
www.ti.com/sc/device/SN65HVD1176

Low-cost current-shunt monitor IC revives moving-coil meter design

By Thomas Kugelstadt (Email: tk@ti.com)
Senior Systems Engineer, Industrial Systems

Despite their lack of resolution and accuracy in comparison to digital meters, analog moving-coil meters remain the display of choice when it comes to tracking a reading's trend or drawing information upon a measurement's rate of change. For low-level current measurements, however, the meter current for a full-scale deflection usually exceeds the current to be measured, and a separate supply driving the meter is required. Analog meters of the past, such as the Multavi-10 from Hartmann & Braun, solved this problem by implementing a rechargeable accumulator as the meter supply. Manually selectable shunt resistors in combination with a high-precision chopper amplifier allowed the user to choose from thirteen different current ranges between 1 µA and 1 A.

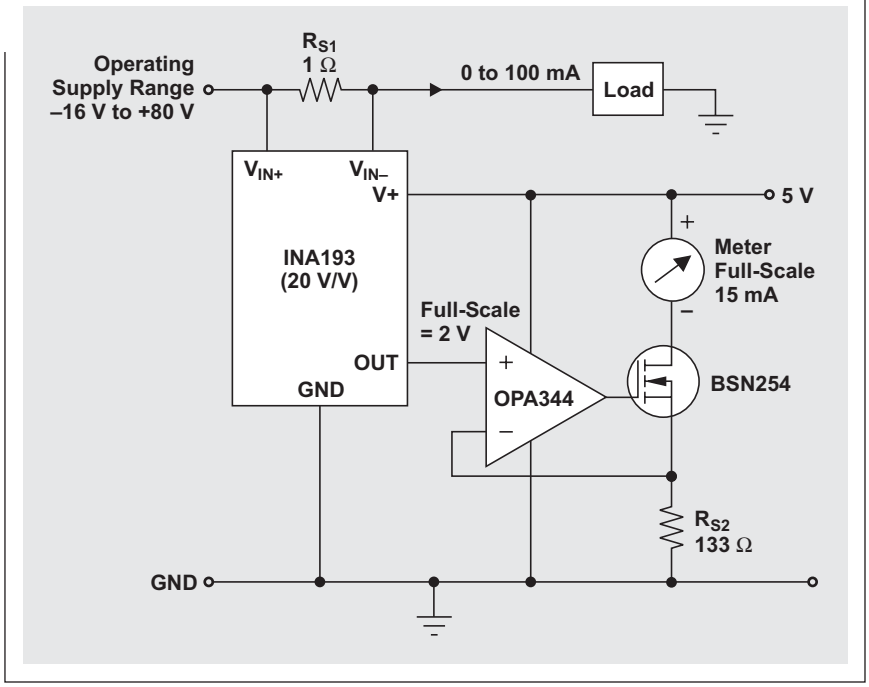
With the introduction of modern current-shunt monitor ICs such as the INA19x family, the amplifier design of moving-coil meters has been drastically simplified. Figure 1 shows the drive circuit of an 8-inch moving-coil meter measuring a current range from 0 to 100 mA. The meter current for a full-scale deflection is 15 mA. The current-shunt monitor, INA193, senses the voltage drop across the 1-Ω shunt resistor, R_{S1}. At a maximum current of 100 mA, the voltage across R_{S1} is 100 mV.

The value chosen for R_{S1} depends on the application and is a compromise between small-signal accuracy and maximum permissible voltage drop in the measurement line. High values of R_{S1} provide better accuracy at lower currents by minimizing the effects of offset, while low values of R_{S1} minimize voltage loss in the supply line. For most applications, the best performance is attained with an R_{S1} value that provides a full-scale shunt voltage range of 50 to 100 mV. The maximum input voltage for accurate measurements is 500 mV.

In this example, the INA193 amplifies the 100-mV full-scale input by a gain factor of 20 V/V, thus providing a full-scale output of 2 V. The succeeding operational amplifier, OPA344, possesses rail-to-rail inputs and outputs; it operates in conjunction with the N-channel MOSFET, BSN254, as a voltage-controlled current source.

Note that the entire meter circuit, including the INA193, operates from a single 5-V supply, which also limits the maximum output voltage swing of the OPA344 to 5 V. It therefore is necessary to choose a MOSFET with a low gate-source threshold voltage, V_{GS}, since this voltage subtracts from the amplifier output swing. The BSN254 has a maximum threshold voltage of 2 V, which satisfies the

Figure 1. Moving-coil meter with separate supply using INA193



low-V_{GS} requirement. Because the voltage at the noninverting OPA344 input equals the one at the inverting input, the full-scale output of 2 V lies across R_{S2}. To allow for the maximum deflection current to flow, R_{S2} is calculated via

$$R_{S2} = \frac{V_{OUT(FS)}}{I_{Meter(FS)}} = \frac{2\text{ V}}{15\text{ mA}} = 133\ \Omega.$$

R_{S2} can be adjusted to calibrate the meter or to change its full-scale current range. R_{S1} can be adjusted to increase low-current measurement accuracy or to extend the measurement range to higher current values. Another benefit of the circuit is that the meter can be separated from the point of measurement. Because moving-coil meters are not intended for high-precision measurements, the designer can use relaxed-accuracy resistors. Bypassing the instrument supply with decoupling capacitors is necessary to avoid stray pickup from the electrical-noise environment.

About the INA19x current-shunt monitor

The INA193 is just one member of a family of current-shunt monitors. The INA194 and INA195 are members that have the same pinout but provide different gains of 50 V/V and 100 V/V, respectively. Three other current-shunt monitors, the INA196, INA197, and INA198, are functionally identical but come in a different pinout.

The INA19x family uses a new, unique internal circuit topology that provides a common-mode range extending from –16 V to +80 V while operating from a single power supply. The common-mode rejection in a classic instrumentation amplifier approach is limited by the requirement for accurate resistor matching. By converting the induced input voltage to a current, the INA19x provides common-mode rejection that is no longer a function of closely matched resistor values, providing the enhanced performance necessary for such a wide common-mode range.

The simplified diagram in Figure 2 shows the basic circuit function. When the common-mode voltage is positive, amplifier A2 is active. The differential input voltage, $V_{IN+} - V_{IN-}$ applied across R_S, creates the voltage potentials v_N and v_P at A2's inputs:

$$v_N = V_{IN+} - I_S R_S \text{ and } v_P = V_{IN+}.$$

To make $v_P = v_N$, A2 must drive the transistor so that its collector current, I_C, causes a voltage drop across the 5-kΩ resistor that equals the differential input voltage:

$$v_P = v_N$$
$$V_{IN+} - I_C \times 5\ \text{k}\Omega = V_{IN+} - I_S R_S$$
$$I_C \times 5\ \text{k}\Omega = I_S R_S$$

Figure 2. INA19x simplified circuit diagram

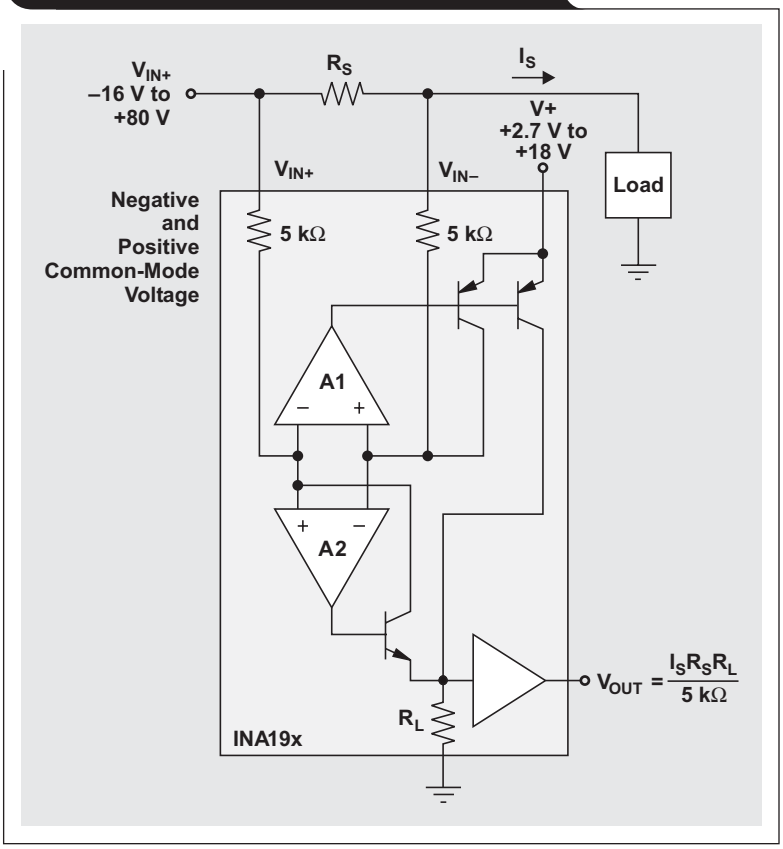
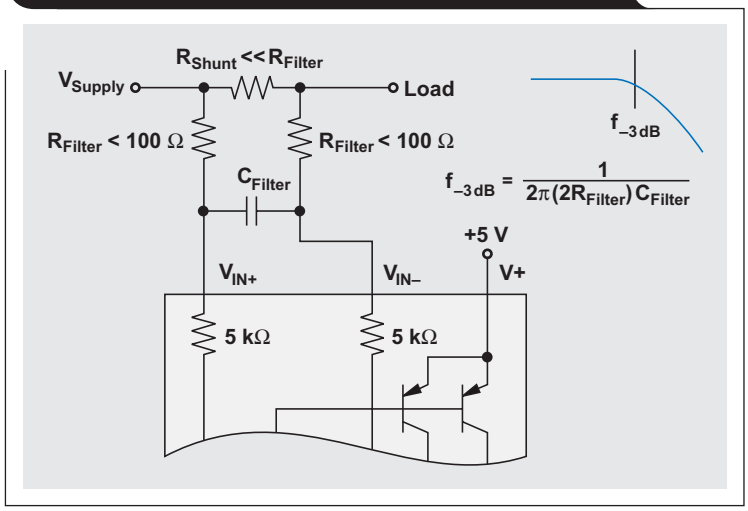


Figure 3. Input filter (gain error = –1.5% to –2.2%)



Expressing I_C through the ratio of output voltage to load resistor,

$$I_C = \frac{V_{OUT}}{R_L},$$

defines the output voltage as

$$V_{OUT} = \frac{I_S R_S R_L}{5\ k\Omega}.$$

When the common-mode voltage is negative, amplifier A1 is active. The differential input voltage, $V_{IN+} – V_{IN–}$ dropped across R_S, is converted to a current through a 5-kΩ resistor. A1 then drives a precision current mirror whose output through R_L provides the signal voltage to the output buffer amplifier. Patent-pending circuit architecture ensures smooth device operation, even during the transition period when both amplifiers A1 and A2 are active.

The input pins, V_{IN+} and $V_{IN–}$, should be connected as closely as possible to the shunt resistor to minimize any resistance in series with the shunt resistance. Power-supply bypass capacitors are required for stability. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Bypass capacitors should be connected close to the device pins.

The input circuitry of the INA19x can accurately measure beyond its power-supply voltage, V+. For example, the V+ power supply can be 5 V, whereas the load power-supply voltage is up to +80 V. The output voltage range of the OUT terminal, however, is limited by the voltages on the power-supply pin.

The output of the INA19x is accurate within the output-voltage-swing range set by the power-supply pin, V+. This is best illustrated by the INA195 or INA198 (both of which use a gain of 100), where a 100-mV full-scale input from the shunt resistor requires an output voltage swing of +10 V and a power-supply voltage sufficient to achieve +10 V on the output.

An obvious and straightforward location for filtering is at the output of the INA19x series; however, this location negates the advantage of the internal buffer's low output impedance. The only other option for filtering is at the input pins of the INA19x, which is complicated by the internal input impedance of 5 kΩ + 30% (see Figure 3). Using the lowest possible resistor values minimizes both the initial shift in gain and the effects of tolerance. The effect on initial gain is given by

$$\text{Gain Error \%} = 100 - \left(100 \times \frac{5\ k\Omega}{5\ k\Omega + R_{Filter}}\right).$$

Total effect on gain error can be calculated by replacing the 5-kΩ term with 5 kΩ – 30% (or 3.5 kΩ) or 5 kΩ + 30% (or 6.5 kΩ). The tolerance extremes of R_{Filter} can also be inserted into the equation. If a pair of 100-Ω 1% resistors is used on the inputs, the initial gain error will be 1.96%. Worst-case tolerance conditions will always occur at the lower excursion of the internal 5-kΩ (3.5-kΩ) resistor, and at the higher excursion of R_{Filter} – 3% in this case.

Note that the specified accuracy of the INA19x must then be combined in addition to these tolerances. While this discussion has handled accuracy worst-case conditions by combining the extremes of the resistor values, it is appropriate to use geometric mean or root-sum-square calculations to total the effects of accuracy variations.

Related Web sites

amplifier.ti.com
www.ti.com/sc/device/*partnumber*
Replace *partnumber* with INA193, INA194, INA195, INA196, INA197, INA198, or OPA344

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