Maximize power density with three-level buck-switching chargers

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Introduction

Modern portable electronic devices require a high-capacity Lithium-ion battery to power popular features such as high-definition cameras, edge-to-edge high-resolution touchscreens and high-speed data connections. As a result, charging power sources like USB Type-C® have increased their output power capabilities to support faster battery charging for high-capacity batteries.

Traditional synchronous buck-based battery chargers cannot take full advantage of high input power because of their maximum efficiency limitations. The challenge for portable electronics designers is how to fit a high-efficiency battery charging solution in a small footprint that fully utilizes high input power to achieve fast and cool charging.

A three-level converter topology that includes added capacitive storage elements and power switches can increase the equivalent switching frequency, f_{SW}, and generate a lower voltage across the inductor, which enables the use of a smaller inductor. This improves total system efficiency, with lower power losses and cooler operating temperatures in a smaller footprint when compared to traditional synchronous buck converters. This article presents an analysis of the three-level buck topology and provides an operation and power-loss comparison between synchronous buck and three-level buck battery chargers, including variances in charging current between the three- and two-level buck topologies.

Traditional buck topology

The synchronous two-level (2L), step-down (buck) switching topology has been around for decades. A traditional buck switching converter consists of two metal-oxide silicon field-effect transistors (MOSFETs or FETs), one inductor, an input capacitor in parallel with the input source and an output capacitor, as shown in Figure 1.

The switch gate-drive signals are complementary, running at duty cycles D and 1 – D. The node between the switches, V_{SW}, alternates between V_{IN} and 0 V; hence the term "two-level converter." When Q_1 is on and Q_2 is off, the inductor is charging and is providing current to the output. When Q_2 is on and Q_1 is off, the inductor discharges to provide current to the output. This produces a fixed duty-cycle square waveform that when filtered by the inductor and output capacitor provides an output voltage.

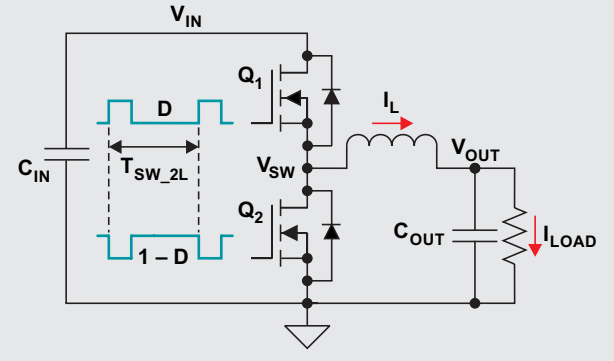
Assuming ideal FETs and continuous inductor current, the steady-state duty cycle is $D = V_{OUT}/V_{IN}$. The f_{SW} determines the inductor's inductance, based on $V = L \times di/dt$ and rearranged as Equation 1:

$$L = (V_{IN} - V_{OUT}) \times f_{SW} \times V_{OUT}/V_{IN}/(I_{LOAD} \times K) \quad (1)$$

where K is the inductor current ripple as a percentage of output current, chosen to be 20% to 40%.

For battery charging applications with wide input-voltage ranges, existing semiconductor processes and inductor technology limit f_{SW} to 1 to 2 MHz. Higher switching frequencies cause transistor switching losses and inductor second-order AC losses to dominate converter losses. Therefore, when trying to increase converter efficiency and reduce heat dissipation, the common solution is to increase inductor footprint size for a lower DC resistance (DCR).

Figure 1. Two-level (2L) buck switches and gate drive



Three-level buck operation

The three-level (3L) buck converter illustrated in Figure 2 is a combination of a switched flying capacitor, C_{FLY}, and a switched inductor circuit, with two additional FETs, Q_3 and Q_4.

The gate-driving scheme is similar to that of a traditional two-phase buck converter. A complementary signal drives the outer FETs, Q_1 and Q_2, with duty cycle $D = V_{OUT}/V_{IN}$, just like the two-level (2L) buck converter. A second complementary signal of equal duty cycle drives the inner FETs, Q_3 and Q_4, but is phase-shifted from the outer FET's signal by 180 degrees. By keeping C_{FLY} balanced at $V_{IN}/2$, the V_{SW} switch node alternates between V_{IN}, $V_{IN}/2$ and ground; hence the term "three-level."

Figure 3 shows a complete switching cycle when the duty cycle is less than 0.5 (that is, when the input voltage is more than twice the output voltage). Figure 4 on the next page shows the complete switching cycle when the duty cycle is greater than 0.5.

At D = 0.5 (50%), Q_1 and Q_4 are on for half of the period; Q_3 and Q_2 are on for the other half. This results in V_{SW} remaining at $V_{IN}/2$, which by definition is equal to V_{OUT}. There is no voltage across the inductor, so the ripple current goes to zero. Because the FETs are driven 180° out of phase, the switching frequency, f_{SW_3L}, at the V_{SW} node is double that of a comparable 2L converter, f_{SW_2L}. Each FET only turns on once during the 2L period, therefore $T_{SW\_2L} = 2 \times T_{SW\_3L}$.

Figure 2. Three-level (3L) buck switches and gate drive

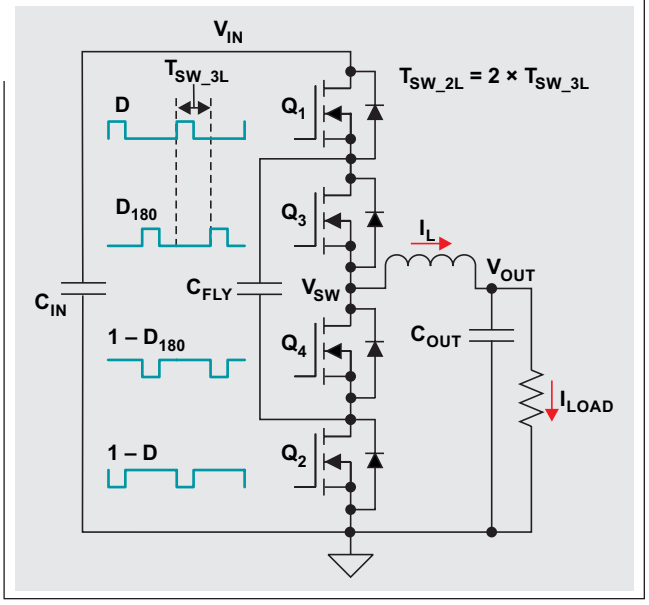


Figure 3. Three-level (3L) converter operation with D less than 0.5

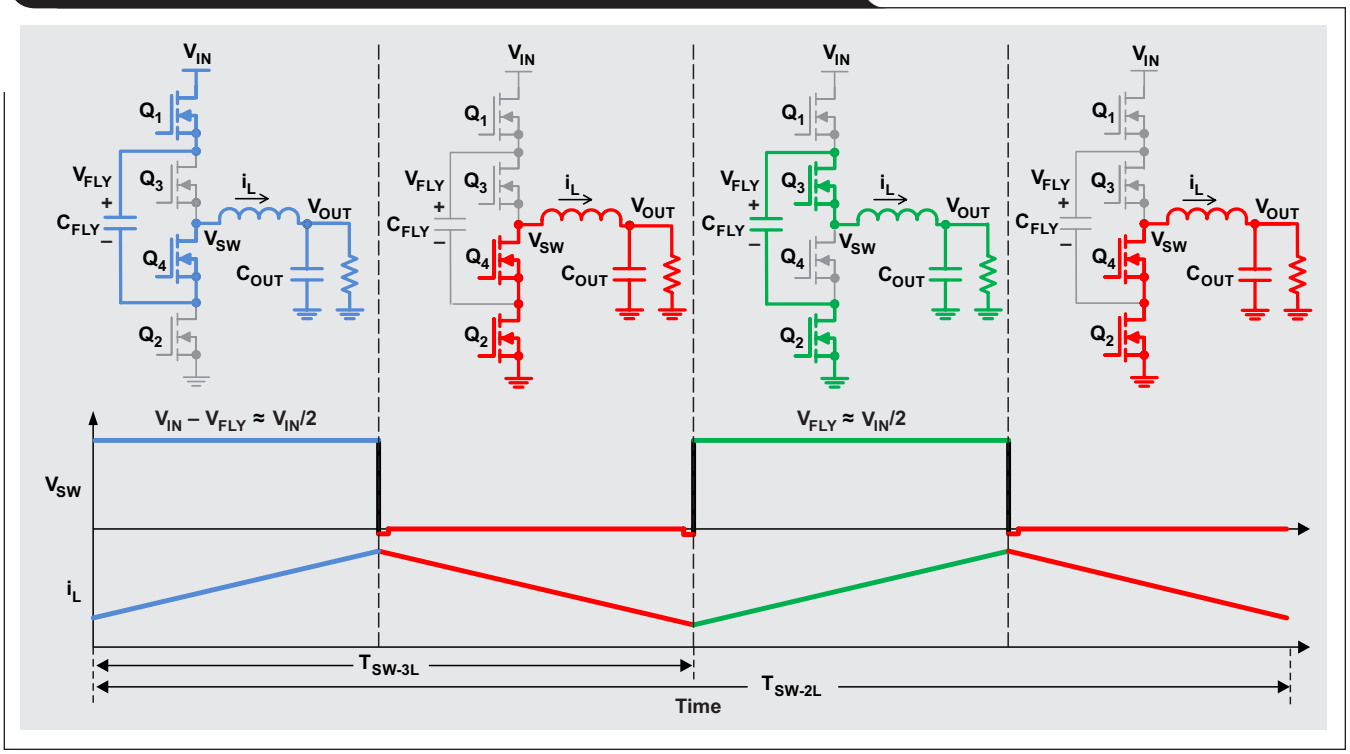
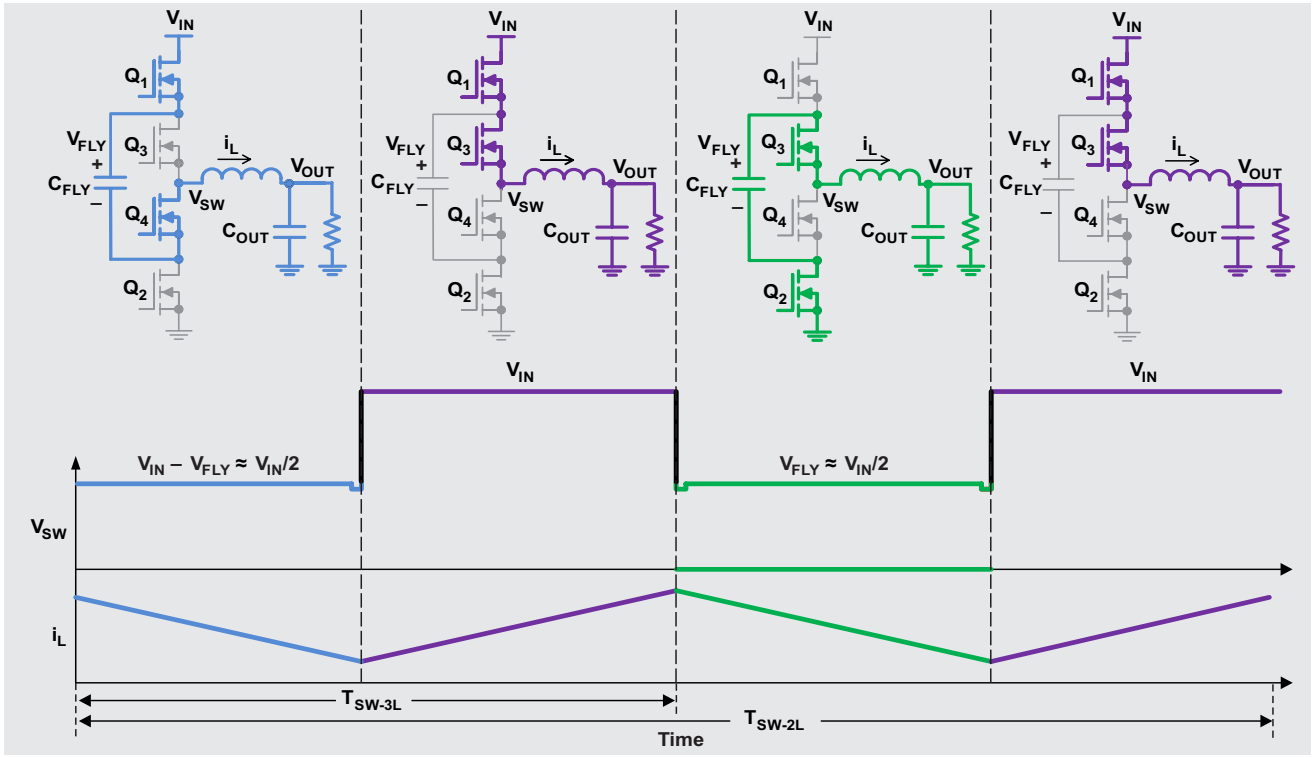


Figure 4. Three-level (3L) converter operation with D greater than 0.5



Three-level (3L) buck on-chip losses

Table 1 compares the 2L buck converter on-chip losses, $P_{ON\text{-}CHIP}$, to those in the 3L buck converter. On-chip losses include conduction losses from the switches' resistances, P_{COND}; switching charge losses, P_{OSS} and P_{GATE}; reverse recovery losses, P_{QRR}; current-voltage losses during gate turn-on and turn-off, P_{IV}; and loss across the body diodes during the dead time when both switches are off, P_{DT}. Assuming C_{FLY} is balanced at $V_{IN}/2$, the 3L buck-converter FETs only need to block half the voltage as compared to the 2L buck converter FETs.

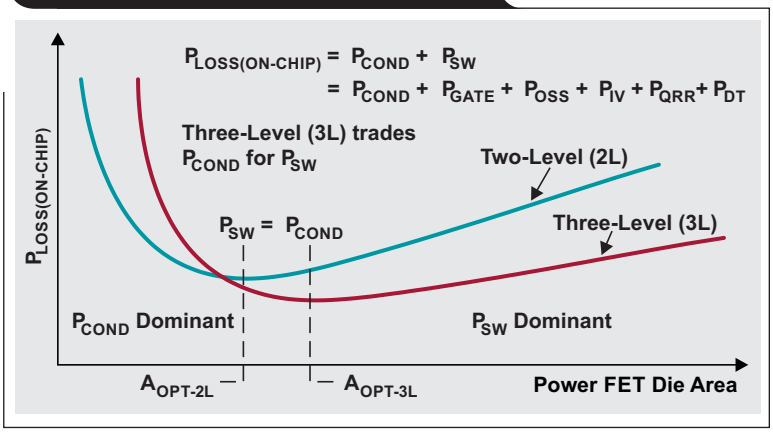
Making the above assumptions about the 2L and 3L losses enables a theoretical comparison of the on-chip power losses between the two topologies as shown in Table 1. The following bullets are highlights from this theoretical comparison:

- The f_{SW} and inductor current ripple are the same for both topologies, which means that the 3L inductance value, L_{3L}, is one-fourth that of the 2L, L_{2L}. This is explained more thoroughly in the next section.
- The area allocated for the 2L high-side (HS) FET is equal to the sum of the area for the 3L HS FETs (i.e., $A_{Q1\text{-}2L} = A_{Q1\text{-}3L} + A_{Q3\text{-}3L}$). With the 3L FETs at one-half the 2L FET's voltage rating, the FET resistances are equal (i.e., $R_{Q1\text{-}2L} = R_{Q1\text{-}3L} = R_{Q3\text{-}3L}$). The same applies to the low-side FETs. This results in the 3L total FET resistance being twice that of the 2L buck for a fixed area.
- If the 3L FETs are at one-half the voltage of the 2L FET but the 3L FETs are driven with the same transient voltages, dv/dt, at V_{SW}, the turn-on and turn-off times are cut in half. This results in P_{IV} being reduced by one-half.
- Using the same area, the total stored charge remains the same, meaning $Q_{OSS(Q1)\text{-}2L} = Q_{OSS(Q1)\text{-}3L} + Q_{OSS(Q3)\text{-}3L}$ and it is the same for $Q_{OSS(Q2)\text{-}2L}$. The total stored charge is actually less because the 3L FETs are at one-half the voltage, but this can be ignored in a simple analysis.

Table 1. Equations for comparing estimated power-loss

	Two-Level (2L) Buck	Three-Level (3L) Buck	P_{3L}/P_{2L}
P_{COND}	$I_{RMS2} \times [D \times R_{Q1} + (1 - D) \times R_{Q2}]$	$I_{RMS}^2 \times [D \times (R_{Q1} + R_{Q3}) + (1 - D) \times (R_{Q2} + R_{Q4})]$	2
P_{IV}	$V_{IN} \times [I_{L(MAX)} \times t_{off(Q1\text{-}2)} + I_{L(MIN)} \times t_{on(Q2\text{-}1)}]/2 \times f_{SW}$	$V_{IN}/2 \times [I_{L(MAX)} \times (t_{off(Q1\text{-}2)} + t_{off(Q3\text{-}4)}) + I_{L(MIN)} \times (t_{on(Q2\text{-}1)} + t_{on(Q4\text{-}3)})]/2 \times f_{SW}$	1/2
P_{DT}	$V_{FWD} \times [I_{L(MAX)} \times t_{DT(Q1\text{-}2)} + I_{L(MIN)} \times t_{DT(Q2\text{-}1)}] \times f_{SW}$	$V_{FWD} \times [I_{L(MAX)} \times (t_{DT(Q1\text{-}2)} + t_{DT(Q3\text{-}4)}) + I_{L(MIN)} \times (t_{DT(Q2\text{-}1)} + t_{DT(Q4\text{-}3)})] \times f_{SW}$	2
P_{OSS}	$V_{IN} \times f_{SW} \times (Q_{OSS(Q1)} + Q_{OSS(Q2)})/2$	$V_{IN}/2 \times f_{SW} \times (Q_{OSS(Q1)} + Q_{OSS(Q3)} + Q_{OSS(Q2)} + Q_{OSS(Q4)})/2$	1/2
P_{GATE}	$V_{IN} \times f_{SW} \times (Q_{G(Q1)} + Q_{G(Q2)})$	$V_{IN} \times f_{SW} \times (Q_{G(Q1)} + Q_{G(Q3)} + Q_{G(Q2)} + Q_{G(Q4)})$	1
P_{QRR}	$V_{IN} \times f_{SW} \times Q_{Qrr(Q2)}$	$V_{IN}/2 \times f_{SW} \times (Q_{Qrr(Q2)} + Q_{Qrr(Q4)})$	1

Figure 5. On-chip losses vs. die area



As shown in the far-right column of Table 1, for the same die area, the 3L topology conduction and dead-time losses double. But because the 3L FETs see one-half the input voltage compared to the 2L buck, P_{OSS} and P_{IV} losses are halved. An increase in FET area makes it possible to lower conduction losses until switching losses begin to dominate, as shown in Figure 5.

The optimal FET areas, A_{OPT-2L} and A_{OPT-3L}, occur where switching losses equal conduction losses.

Three-level (3L) buck off-chip components and their losses

Off-chip losses include those across the equivalent series resistance (ESR) in the input, output and flying capacitors, as well as the inductor. Choosing ceramic capacitors with very low (<20 mΩ) ESR renders their losses almost negligible. Input and output capacitors for the 3L converter are also sized based on acceptable input ripple current and output voltage ripple, just as they are for a 2L converter.

Sizing C_{FLY} for acceptable ripple voltage and current is critical for 3L operation. In fact, keeping C_{FLY} balanced at $V_{IN}/2$ during transients, startup, at light load and D = 100% is not trivial and requires some additional, proprietary circuitry not shown in Figure 2. Figure 6 shows an example waveform for ΔI_{FLY} relative to normalized ΔI_L.

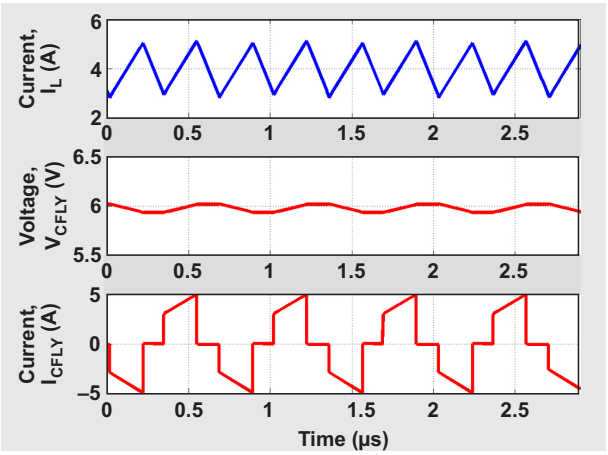
Equations 2 and 3 are for C_{FLY} ripple voltage and current:

$$\Delta V_{C(FLY)} = I_{LOAD} \times (0.5 - |D - 0.5|)/(C_{FLY} \times f_{SW}) \quad (2)$$

$$\Delta I_{C(FLY)-RMS} = [2 \times (0.5 - |D - 0.5|) \times (I_{LOAD}^2 \times + \Delta I_L^2/12)]^{0.5} \quad (3)$$

C_{FLY} ripple voltage peaks at D = 0.5 and increases directly with load current. After factoring in ceramic capacitor derating from DC bias and temperature, C_{FLY} must withstand half the input voltage. Note that at D = 0.5, $I_{C(FLY)}$ sees the full load current. C_{FLY} capacitance is sized to keep $\Delta V_{C(FLY)}$ less than 10% of $V_{IN}/2$ in order to ensure loop stability. To ensure long capacitor life, the capacitor package size and RMS current rating must be large enough to handle the associated temperature rise.

Figure 6. C_{FLY} ripple voltage and current relative to inductor ripple current

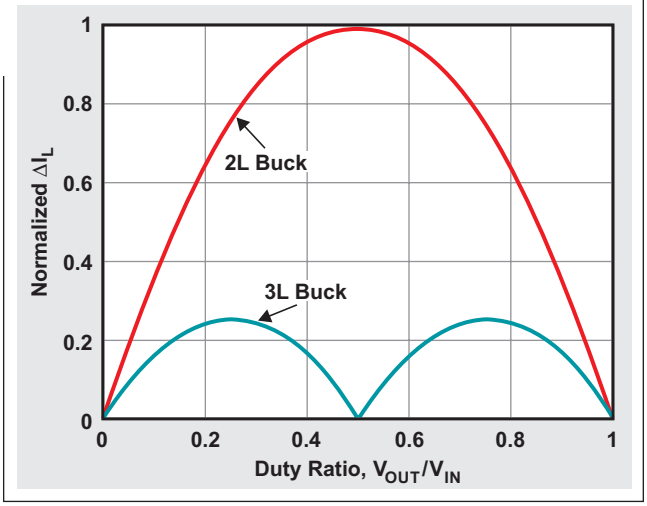


Inductor losses consist of DCR losses, P_{DCR}, and core losses, P_{CORE}. The DCR losses increase with inductance value, which is a function of f_{SW}.

The 180-degree phase-shifted gate drive for Q_3 and Q_4 effectively doubles the converter's switching frequency at V_{SW}. Additionally, by keeping C_{FLY} balanced at $V_{IN}/2$, the three-level converter reduces the volt-seconds across the

inductor by half. The combination results in a one-quarter reduction in inductor ripple given the same inductor and f_{SW}. The reduction in inductor ripple current compared to the 2L converter switching at the same frequency over duty cycle is apparent in Figure 7.

Figure 7. Duty cycle comparison of 2L and 3L converters



In a 3L converter, Equation 4 derives the inductance value:

$$L = V_{IN}/2 \times (|D - 0.5| - (D - 0.5)^2)/(K \times I_{LOAD} \times f_{SW}) \quad (4)$$

and Equation 5 calculates the inductor DCR losses:

$$P_{DCR} = I_{L(RMS)}^2 \times R_{DCR} = (I_{LOAD}^2 + \Delta I_L^2/12) \times R_{DCR} \quad (5)$$

Equation 5 confirms that inductor current ripple has little effect on P_{DCR}. Like the 2L buck converter, the 3L converter requires an inductor with lower DCR for higher efficiency. As explained above, the topology inherently provides a one-quarter reduction in inductor ripple current. If the application can accept the inductor ripple current and resulting output voltage ripple from a comparable 2L converter operating at the same switching frequency, an inductor with one-quarter the inductance value could be used, which is available in a package with a much smaller footprint.

Assuming that inductor DCR scales proportionally with the inductance value, the inductor losses for the 3L converter, P_{DCR-3L}, are one-fourth that of the 2L converter, $P_{DCR-2L}/4$. The smaller package yields a smaller total solution size, while the lower DCR yields higher efficiency. Therefore, for the same thermal budget, these benefits enable the 3L converter to provide a higher output current in a smaller area (that is, a higher power density) compared to a 2L buck solution.

Comparing 3L and 2L buck charging solutions

TI's latest 3L, single-cell buck charger, the BQ25910, operates at f_{SW} = 750 kHz and is capable of providing 5 A of battery charge current. Comparatively, TI's BQ25898 4-A 2L charger comes in a similar chip-scale package, with an older silicon process technology, but operates at an f_{SW} = 1.5 MHz. The BQ25898 uses a 1-µH inductor while the BQ25910 uses a 470-nH inductor—which is only one-half and not the potential one-fourth reduction in inductance that the 3L topology enables.

Table 2 compares component areas for the two chargers, using inductors with similar current ratings and reasonable DCR. The table also excludes routing and ignores common components for both chargers such as the input capacitor, PMID-pin capacitor and linear-regulator capacitor.

Table 2. Component area comparison

Converter	PCB Area (mm^2)						
	IC	Inductor	C_{FLY}	C_{BAT}	C_{AUX}	Total	% Difference
BQ25898 (2L)	7.0	17.6	0.0	1.3	0.0	25.9	—
BQ25910 (3L)	5.9	5.5	2.6	—	0.5	16.5	–36.3

Even with the additional capacitors, the BQ25910's smaller footprint but similar DCR inductor and lack of battery FET results in a 36% reduction in printed circuit-board (PCB) area.

Figure 8 shows the power losses for the BQ25910, modeled using the equations in Table 1 and actual silicon process data. Also shown are the losses for the BQ25898. Note how the inductor DCR losses dominate the total losses for both chargers.

Figure 8. BQ25910 vs. BQ25898 modeled power losses

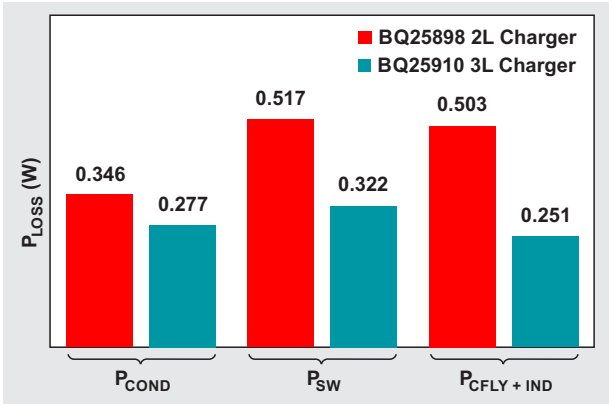


Figure 9a shows a plot of the BQ25910 and BQ25898 measured efficiency at a 9-V input voltage and a 3.8-V battery voltage. Figure 9b compares the losses of the two converters. At a 3-A charge current, the BQ25898 efficiency is 89.3%. From Figure 8, the BQ25910's P_{LOSS} is 0.850 W from a total output power of 3 A × 3.8 V = 11.4 W, resulting in 93.1% efficiency, which is very close to the measured 93.2%.

At a 9-V input voltage, 3.8-V battery voltage and 3-A charge current, the 3L BQ25910 has a 3.9% efficiency improvement and 36% loss reduction. For a loss budget of 1.5 W, the BQ25898 can provide 3.2 A of charge current, while the BQ25910 can provide 4.2 A of charge current (a 31% increase) in a 36% smaller solution size.

Conclusion

Consumers want their personal electronics, with their ever-increasing battery capacity, to charge as quickly as possible. Achieving more than 90% efficiency for 3-A and higher charging currents from a 9-V or higher adapter in a small footprint remains difficult with traditional 2L buck switching chargers. Battery charging solutions are needed that fit in the smallest footprint while providing the optimal charging current, not only for improved battery safety and lifetime, but also for acceptable charging time and device temperature. The 3L buck switching chargers offer improved efficiency while reducing total solution size for compact design requirements.

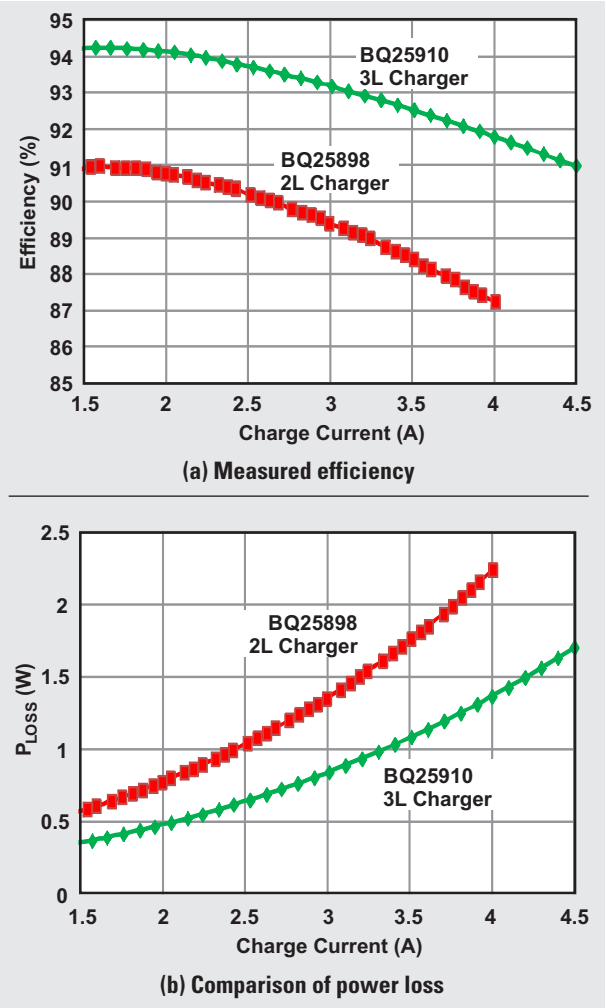
Related Web sites

Product information:
BQ25898
BQ25910

Three-Level Buck Charger video
(scroll down for videos)

Alvaro Aguilar, "How to increase charging current while shrinking overall solution size for portable electronics," TI E2E™ support forums, March 1, 2018

Figure 9. BQ25910 and BQ25898 measured efficiency and power losses



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