# How to prevent transformer saturation in push-pull converters

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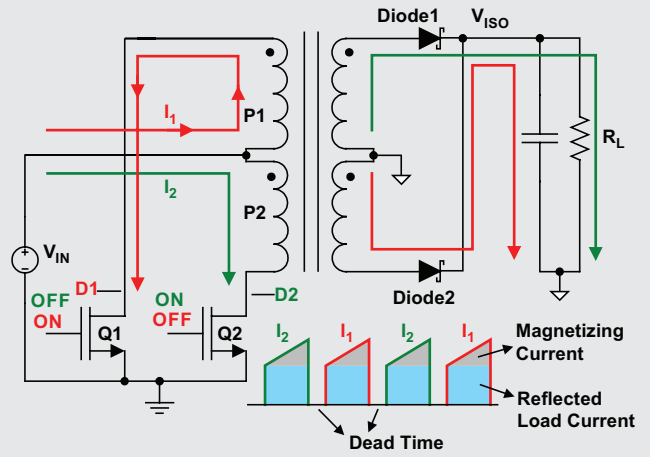
## Introduction

The push-pull converter has emerged as a popular topology to create isolated power supplies in the 1-W to 10-W range. This topology is pairable with digital isolators, isolated amplifiers, isolated analog-to-digital converters, isolated interfaces such as isolated Controller Area Network and isolated RS-485, and isolated gate drivers. See Figure 1.

The popularity of the push-pull converter stems from its simplicity of operation, low electromagnetic emissions, low peak currents, high efficiency, high immunity and low system cost.[1] It is possible to design an isolated power rail with a push-pull topology using just a few discrete components: two power switches, a center-tapped transformer and rectifier diodes. Because it is a feed-forward topology, an optocoupler-based feedback is not needed, and thus, there are no loop stability concerns.

Although the push-pull converter has many advantages, one major concern is the possibility of transformer saturation. This converter relies on good matching between the two phases of operation to avoid flux buildup in the transformer core. Transformer saturation can lead to an exponential increase in primary current, resulting in input supply collapse or even damage to the converter. This article describes the likely scenarios that can cause transformer saturation in push-pull converters, and also parameters that can mitigate or prevent transformer saturation.

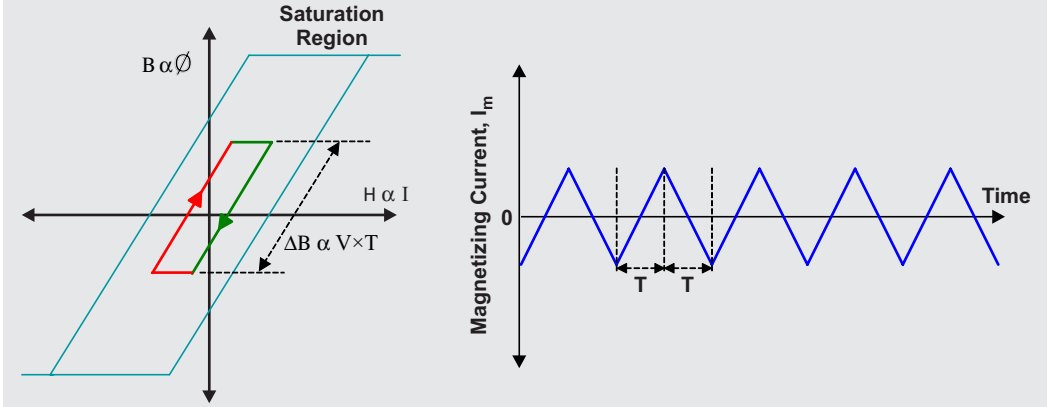
**Figure 1. A push-pull converter**




## The basic operation of a push-pull converter

In the push-pull converter shown in Figure 1, field-effect transistors (FETs) Q1 and Q2 are designed to be equal in drive strength and turned on for the same time (T) in alternate cycles. The two primary windings are wound such that the flux created by Q1 turning on is exactly equal and opposite to the flux created by Q2 turning on. The flux buildup in each phase (ΔB) is proportional to the voltage applied across the transformer primary (V) and the T for which the voltage is applied. With all components fully matched, the flux in the transformer core operates in two quadrants around zero, as shown in Figure 2. Because of exact flux cancellation in the two phases, the converter operates in a steady state, with no continuous flux buildup. The magnetizing current ($I_m$) correspondingly swings in a triangular wave around zero.

**Figure 2. Flux in the transformer and $I_m$**



## The effects of mismatches

If there is a mismatch between the two phases of operation—for example, if the voltage applied is different or if the time duration is different—the flux buildup in the transformer in one cycle is not fully canceled in the other cycle. This leaves a slight residual flux after one full period of operation that will slowly build up over time, eventually walking the transformer into the saturation region. See Figure 3. The $I_m$ builds up either in the positive or negative region based on the polarity of the mismatch. In the saturation region, the current through the transformer primary winding can increase drastically, potentially causing catastrophic damage to the transformer and driver transistors.

## Compensating for mismatches

A practical push-pull converter always has mismatches. Even the smallest mismatch can cause significant flux buildup over time. Does this mean that a push-pull converter will always saturate? No.

Negative feedback from Q1 and Q2 on-resistance ($R_{ON}$), current limiting, and $I_m$ transfer to the load during dead time can all help prevent transformer saturation. The use of these techniques and their effects are described next.

### Negative feedback from FET $R_{ON}$

As shown in Figure 3, in the presence of flux imbalance, the $I_m$ in one phase is higher than the other. The phase that has the higher current flowing sees a higher drop through the power FET, and thus a lower voltage is applied across the transformer in that phase. Less flux builds up in that phase, which reduces $I_m$. If the mismatch in the converter is small, this negative feedback is enough to keep the converter in a stable equilibrium.

However, depending on the values of FET $R_{ON}$ and $I_m$, this negative feedback may not be able to compensate for converter mismatches. For example, if the input voltage ($V_{IN}$) is 5 V, the peak $I_m$ is 100 mA and the FET $R_{ON}$ is 1 Ω, then the maximum negative feedback the FET $R_{ON}$ can provide is 100 mA × 1 Ω = 100 mV over 5 V, which is 2%. That is, the FET $R_{ON}$ can compensate for up to 2% of mismatches (caused by, for example, an on-time mismatch between the two phases). This 2% compensation is sufficient to prevent saturation in most cases. However, if the FET $R_{ON}$ is only 0.25 Ω, then the negative feedback can only compensate for 0.5% of mismatches, which may not be sufficient to always prevent saturation.

This approximate analysis is useful to get a sense of the extent of mismatches for which negative feedback from FET resistance can compensate. For high-power converters where the FET $R_{ON}$ is designed to be low in order to reduce conduction losses, negative feedback from FET resistance may not be enough to prevent transformer saturation.

### Current limiting

Another technique to prevent saturation is cycle-by-cycle current limiting, which monitors the current through the FETs for each cycle. If the current exceeds a safe limit (usually set at two to three times the operating current range), the cycle terminates. While current limiting can be a reliable safety net, this method can cause higher overall $I^2R$ power losses, since the peak currents in the converter are allowed to rise to a higher value than required. The impact on efficiency is higher at light loads, where the absence of load current means that $I_m$ must increase to much higher values to hit the current limit. Figure 4 shows the effect of current limiting on $I_m$, which cannot exceed the set current limit.

**Figure 3. Magnetic flux buildup and the rise of $I_m$ caused by a mismatch**

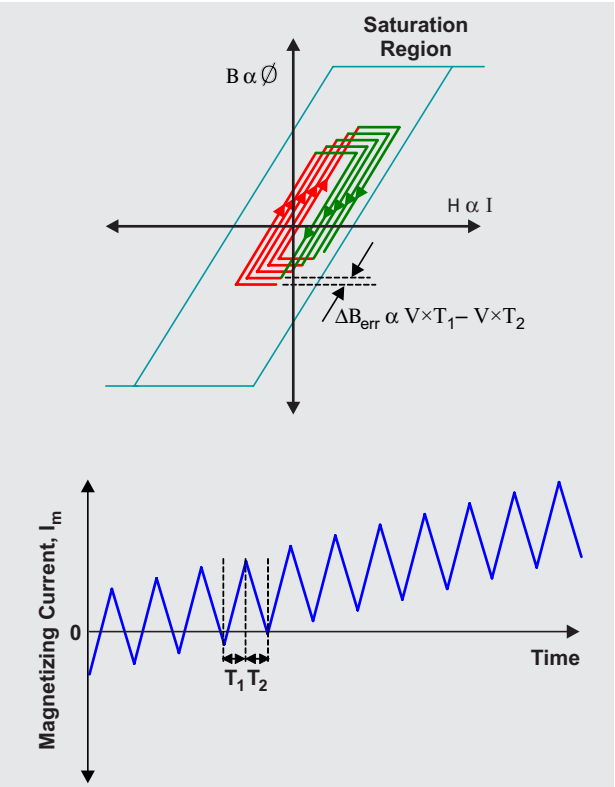
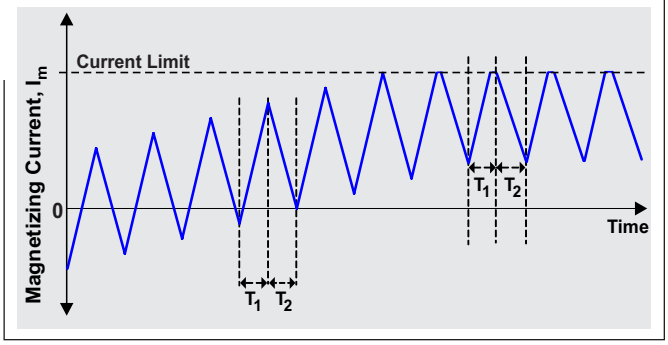



**Figure 4. Current limiting prevents $I_m$ from building up to unsafe levels**



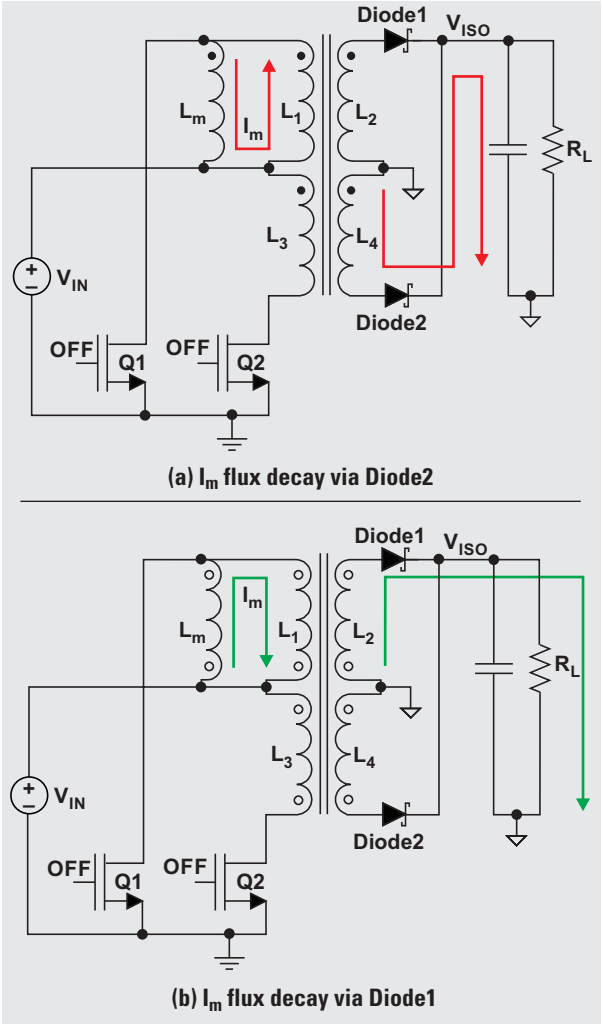
## Effect of dead time on transformer saturation in a push-pull converter

To prevent shoot-through currents, push-pull converters always have a certain dead time between the two phases. During dead time, FETs Q1 and Q2 are both off. The favorable effects of dead time in preventing transformer saturation are described below.

In Figure 5, the magnetizing inductance is modeled as $L_m$. Current through $L_m$ is $I_m$. Since FETs Q1 and Q2 are both off during dead time, the $I_m$ raises the drain voltages of either Q1 or Q2 such that either Diode1 or Diode2 is forward-biased. The current path depends on the polarity of $I_m$ at the beginning of the dead time. The secondary-side voltage appears across the core of the transformer, thereby decaying the core flux. In other words, $I_m$ has a way to decay through secondary-side diodes Diode1 or Diode2 during dead time. The current flow through the secondary diodes stops when $I_m$ (and thus the core flux) reaches zero.

If the total dead time as a percentage of on-time T is greater than the percentage mismatch in the flux between the two phases, then the flux will always decay to zero during the dead time. The push-pull converter now operates in a single quadrant, as shown in Figure 6. If in the steady state, the slightly higher flux developed in one phase ($\Delta B_1$) compared to the other phase ($\Delta B_2$) causes a net positive $I_m$ at the end of the full cycle, then this positive $I_m$ decays through the secondary diode during the dead time ($\Delta B_3$ and $\Delta B_4$) until the flux and $I_m$ drop to zero. As shown in Figure 6, $I_m$ does not build up indefinitely and reaches a steady state where it remains positive. Similarly, if the mismatch causes a net negative $I_m$ at the end of two phases, $I_m$ will reach a steady state with a net negative $I_m$.

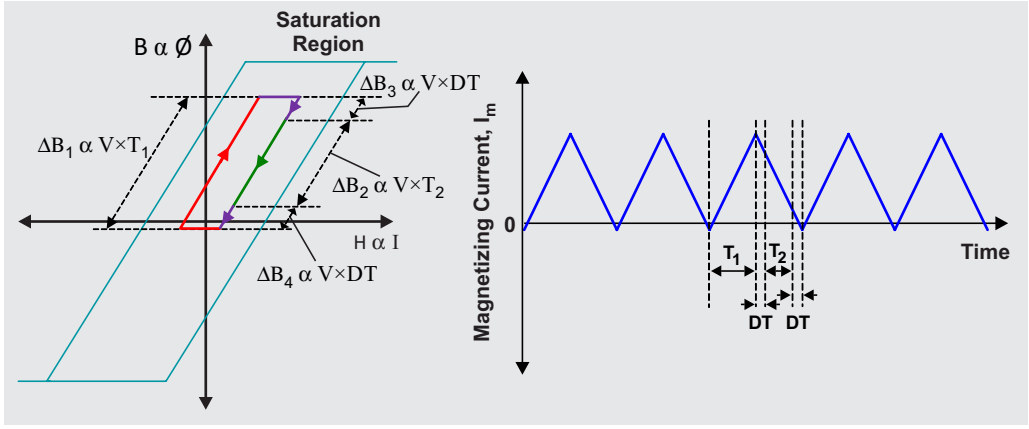
**Figure 5. Decay of $I_m$ through diodes**




## Silicon measurement results

We tested the impact of dead time on the SN6505B push-pull converter by intentionally adding a timing mismatch between the two phases through test modes. Without a mismatch, the on-time of each phase was 625 ns. Adding a mismatch to skew the two on-times ($T_1$ and $T_2$) all the way to 540 ns and 710 ns amounted to a total mismatch of 170 ns. The power-converter efficiency and overshoots on the switching node were then observed to get an indication of transformer saturation. A sudden increase in $I_m$ will show up as an inflection point for power-converter efficiency and overshoots.

**Figure 6. Flux and $I_m$ remain stable in spite of a mismatch, decaying to zero during dead time (DT)**



The total built-in dead time per clock period for the SN6505B is 160 ns, or 80 ns of dead time after each on-time. Figure 7 shows the converter efficiency vs. the load current as the mismatch between phases increases from 90 ns to 170 ns. Figure 8 plots the switching nodes (drains of Q1 and Q2) for three mismatch values: 150 ns, 160 ns and 170 ns. As these two figures indicate, the efficiency curves of the converter as well as overshoot on the switching nodes show an inflection point when the mismatch is around 150 ns to 160 ns, which is close to the total dead time in the SN6505B and $I_m$. These measurement results support the analysis in the previous section, and prove that mismatches up to the dead time as a percentage of the on-time do not saturate the push-pull converter.

The results also show that the SN6505B is able to remain stable, not saturating even for 10% to 12% of an intentionally added mismatch. This percentage is a much

**Figure 7. Efficiency vs. load current for different values of on-times $T_1$ and $T_2$**

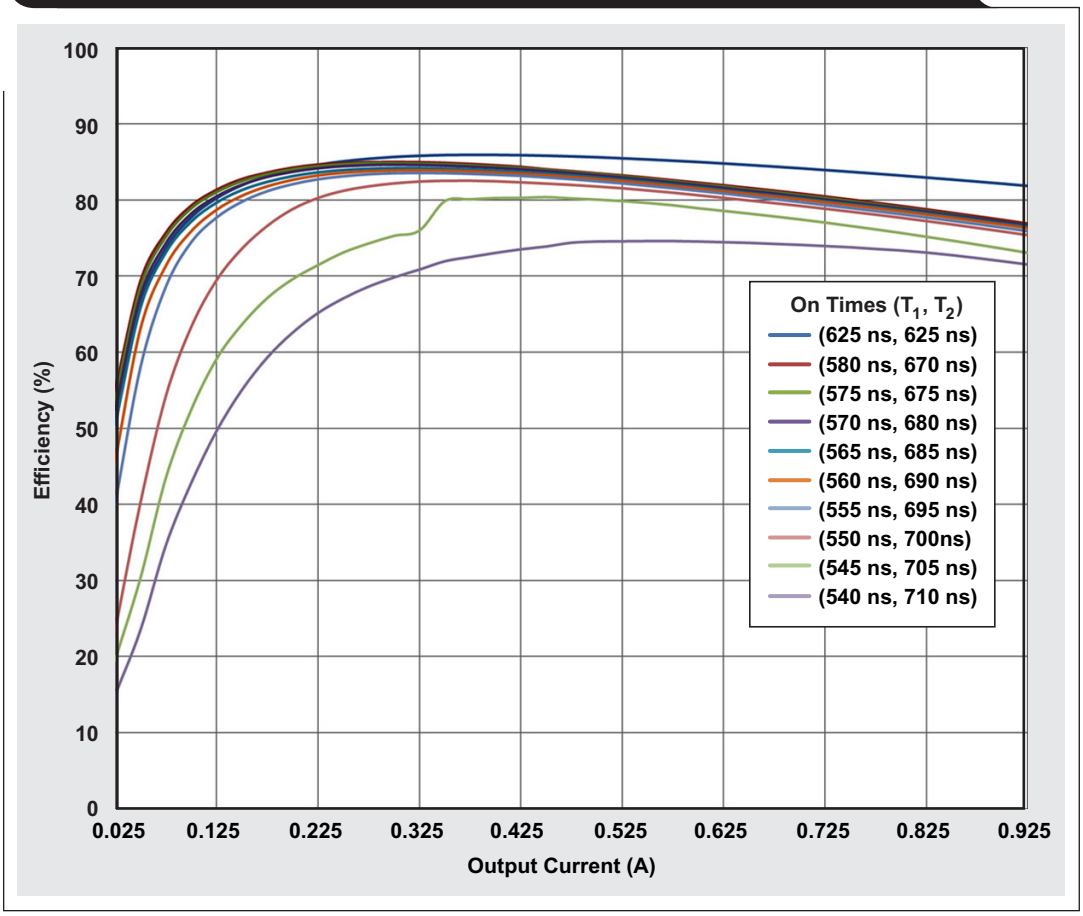
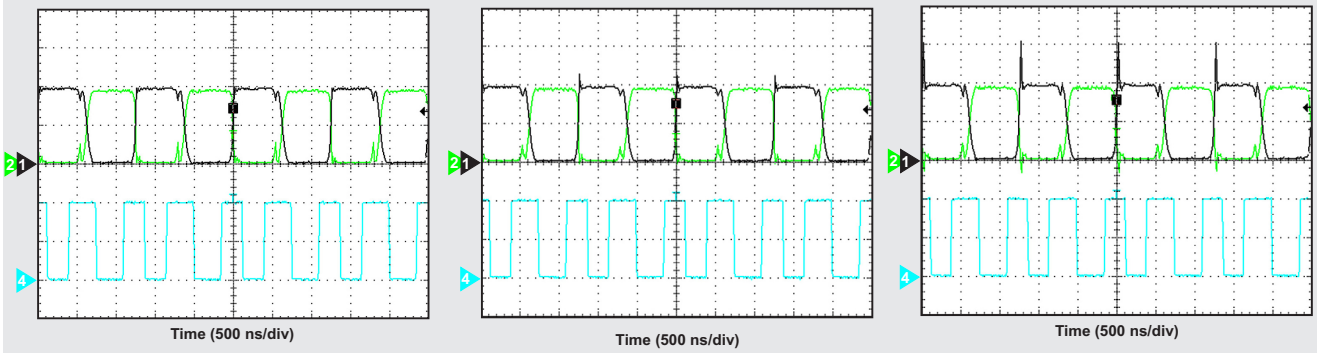



**Figure 8. Switch-node overshoot for different values of on-times $T_1$ and $T_2$**



higher mismatch than what is usually present in push-pull converters (2% to 3%). For further protection, the SN6505B also features a built-in current limit.

## Conclusion

Flux decay through the secondary diodes during dead time is very effective in preventing saturation. As long as the mismatches are lower than the dead time, in percentage terms, it is possible to prevent transformer saturation. Isolated power supplies designed with the SN6505B do not saturate, thus remaining stable in the presence of large mismatches.

## Reference

1. Anant Kamath, “Push-pull converter simplifies isolated power supply design in HEV/EV systems,” Analog Design Journal (SLYT790B), 1Q 2020.

## Related Web sites

Product information:
**SN6505B**

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