

AD-02 High Performance ADC's Require Dynamic Testing



Literature Number: SNAA017

High-Performance ADCs Require Dynamic Testing

Joseph D. Giacomini

August 1992

DESIGNERS MUST GO BEYOND TRADITIONAL TEST TECHNIQUES WHEN EVALUATING FAST, HIGH- RESOLUTION ADCs.

This is the first of two articles focusing on the issues involved in the design and test of high-performance analog-to-digital converters. Here, required external support hardware and its limitations will be covered. Also discussed are the specifics of distortion testing. The second article will cover tests for intermodulation, aperture jitter, and ac and time-domain considerations.

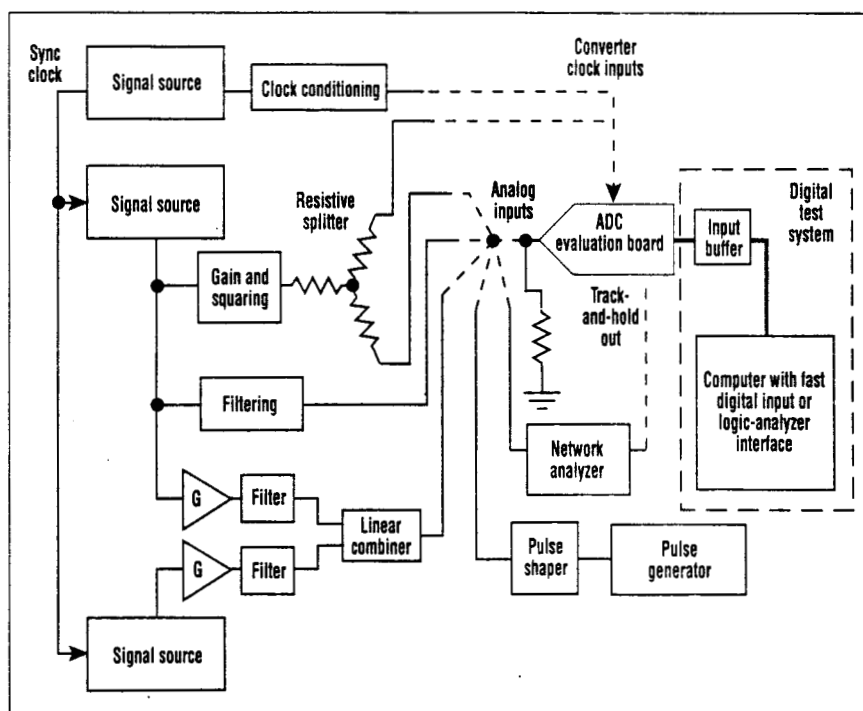
To optimize system performance, designers using high-performance analog-to-digital converters (ADCs) must thoroughly understand ADC test techniques and their limitations. At conversion speeds above 10 Msamples/s and resolutions beyond 10 bits, many traditional evaluation techniques no longer work. Difficulties arise when trying to exercise the ADC in a way that closely approximates the application. The evaluation phase should consider board layout and signal-conditioning issues to eliminate or reduce the risks associated with combining analog and digital circuitry in one system. This requires a test system that's flexible, accurate, and insensitive to variations in the parameters of support circuitry.

One traditional ADC characterization test places the device into a dc

servo loop, where each threshold is individually measured. This test supplies accurate and repeatable data on the dc transfer function, and is still quite useful for high-resolution, low-speed converters. But subtle interactions between the converter and the board alter the overall system performance as operating frequencies increase.

One solution is to test the circuit while applying high-frequency signals. For simple frequency-domain applications, single-tone testing may be adequate. However, many systems have multiple tones present simultaneously, which means that intermodulation becomes an issue. In other systems, integral linearity is less of an issue but differential code-to-code errors, slew rate, and sampling jitter are important.

Another traditional test method is to add a digital-to-analog converter (DAC) after the ADC to reconstruct the original waveform. If this is the way the ADC will be used in the application, typically with some digital



1. A COMPLEX TEST SETUP IS NEEDED to complete the majority of an ADC's evaluation. In practice, however, most applications can get by with only a portion of the components shown here.

JOSEPH D. GIACOMINI

Comlinear Corp., 4800 Wheaton Dr., Fort Collins, CO 80525; (303) 225-7509.

processing between conversions, the work required to obtain accurate results may be worthwhile. However, this technique is too inflexible and inaccurate for most applications.

The obvious alternative is a computer-driven test system that removes the errors created during waveform reconstruction. In describing the technique, this article discusses the hardware and software needed for the digital test system, and the hardware for the remainder of the setup, including signal sources, clock-conditioning circuits, filters, and support circuitry (Fig. 1).

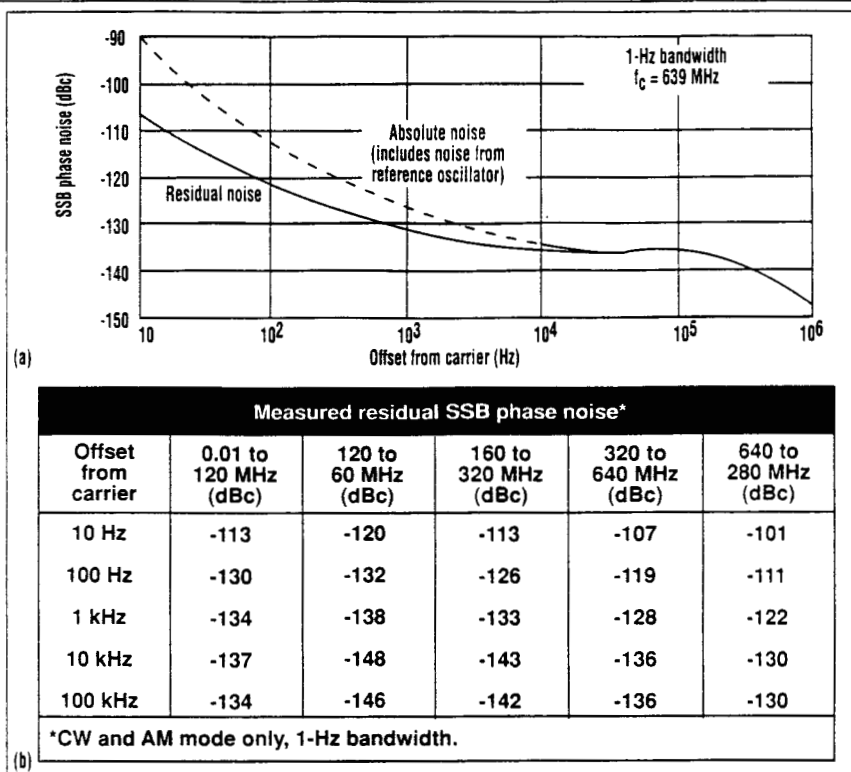
The number one consideration for the digital test system is flexibility. The system's fast edge rates and long cables create transmission-line and crosstalk problems. These effects can produce current spikes of 0.5 to 1.0 A in the digital power-supply lines of the device under test (DUT). Another problem is digital noise from the computer feeding back into the ADC's ground and supply lines. Consequently, the input buffer must isolate the ADC evaluation board from the cable leading to the computer.

ENSURING FLEXIBILITY

Digital line drivers placed close to the converter's output lines supply good isolation. Even better is a technique used in logic-analyzer pods, in which comparators latch the data and drive the cable. Rather than build the required custom interface circuitry, the designer can use a logic analyzer to collect high-speed data. The computer can read the data from the analyzer over a conventional serial link. The comparators' flexibility is very valuable during ADC evaluation and board development. With a simple threshold adjustment, any logic level can be examined. With the comparators' high input impedance, designers can probe circuit boards, which is very useful in hardware/software integration.

In summary, the input buffer should:

- create minimal loading on ADC output lines,
- enable the user to program thresholds from -2.5 to +5.0 V,



2. ALTHOUGH A SYNTHESIZER'S PHASE stability is specified in terms of single-sideband phase noise, as shown in this example for the HP 8662A (a), designers can use a linear approximation of the noise power between decades to estimate the total rms noise power (b).

- have an external clock input,
- include gating or triggering features (optional),
- have minimal setup and hold times (less than 1 ns preferred), and
- permit data rates up to 50 MHz (preferred).

Of course, the buffer memory itself must be wide enough to accommodate the system's data width. In addition, memory depth should be at least 2^w , where w is the data width. That is, 12-bit data requires a memory of at least 4096 words deep. The computer should have a minimum of 1 Mbyte of RAM, a floating-point processor, and an instrument controller card.

Beyond the obvious data-collection aspects, the system's software must be easy to use and to modify. It should contain I/O plotting/printing and disk-interface routines, as well as instrument control capabilities. Ideally, the software would incorporate every conceivable test function, selectable by the touch of a button. In practice, there will always be

some specialized test needed during the initial component evaluation phase or during later design integration phases. However, to speed development, the software should include a minimal set of routines:

- data acquisition,
- forward and inverse fast Fourier transforms (IFFTs),
- windowing,
- spectral analysis,
- histograms for integral and differential nonlinearity graphs (INL and DNL) graphs, and
- data viewing.

The data-acquisition function is fairly straightforward. Parameters required include the threshold voltage, number of bits, record length, and triggering information.

Which fast Fourier transform is used is unimportant, as long as its length is adjustable and it converts in either direction between the time and frequency domains. Short FFTs are useful for debugging systems, but long records are essential to

sizer offers the most flexibility. As for specifications, low phase noise is the first concern. The residual phase noise between the reference clock and the analog output signal must be low. The absolute phase noise in both signals is almost completely eliminated by the sampling process. Broadband noise is less of an issue because it can be filtered.

An easy way to understand the effect of residual phase noise, called jitter, is to consider the case where the clock and analog frequencies are the same. In the worst-case situation, the ADC samples the analog signal at its zero crossing. In the ideal case, the converter output is always the same nominal value. If a phase error exists between the sampling clock and the input sine wave, the sample value will be slightly above or below the nominal value.

For instance, consider a 5-MHz sine-wave input with an amplitude of 2 V pk-pk and a phase error of 0.01° (a sampling-time error of roughly 5 ps). The magnitude of the voltage error would be 175 μ V, which is 1.4 times the quantization level of a 14-bit converter. As the signal's slew rate decreases, so does the error. For a sine wave ($\delta V/\delta t$), the slew rate is:

$$S_r = V_p \omega [\cos(\omega t)] \quad (3)$$

where V_p is the peak amplitude of the sine-wave input signal and ω is the input signal's radian frequency.

The total sampled noise is the integral of the slew rate multiplied by the timing jitter over one cycle of the input waveform. Because the phase noise isn't correlated to the input signal, the result simplifies to:

$$e_n = S_r|_{rms} \times \delta t_j \\ = (0.707 V_p \omega) \times \delta t_j \quad (4)$$

where e_n is the rms noise energy in volts, and t_j is the timing jitter. This figure is the rms slew rate of a sine wave ($\delta V/\delta t$) multiplied by the rms jitter (δt).

The SNR in dBc based on jitter is only:

$$SNR_j = 20 \times \log(V_{in rms}/e_n) \\ = -20 \times \log(\omega \times \delta T) \quad (5)$$

where $V_{in rms}$ is the rms value of the analog input signal.

If the jitter is 5.55 ps rms, SNR_j is 75.2 dBc. This is unacceptable because the ideal SNRs for 12- and 14-bit converters are 74 dB and 86 dB, respectively. Also, ADC track-and-hold circuits currently achieve about 1 to 2 ps rms of jitter. In practice, the SNR for either a 12- or 14-bit converter is limited to about 70 dB, but SNR_j continues to grow with increased analog frequency.

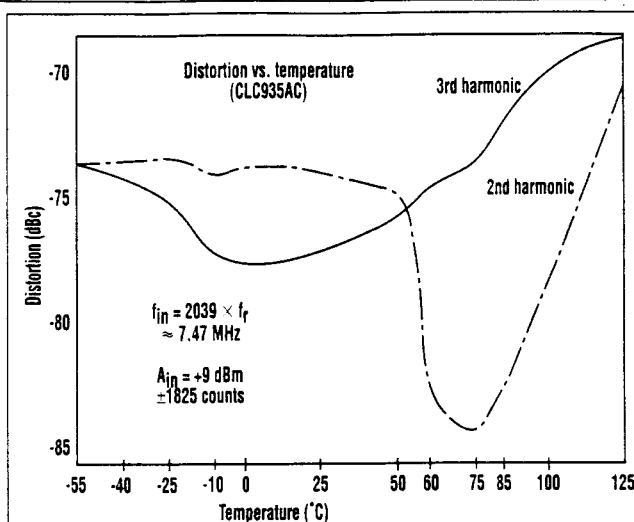
Unfortunately, a synthesizer's phase stability is specified in terms of single-sideband (SSB) phase noise, not rms timing jitter. However, specification data from the HP 8662A synthesizer manual shows that designers can use a linear approximation of the noise power between decades to estimate the total rms noise power (Fig. 2).

The noise power can then be related to jitter using Equation 4. To integrate the noise, the designer needs an equation that provides a linear slope on a log-log scale. In addition, the power must be converted from decibels to a power ratio. Equation 6, which is setup for piecewise approximation between various frequency points, performs the conversions:

$$e_n(f_1 \text{ to } f_2) = \\ 10^{(nf_1/10)} \int_{f_1}^{f_2} \left(\frac{f}{f_1}\right)^{m/10} df \quad (6) \\ = 10^{(nf_1/10)} \times f_1^{(-m/10)} \times \frac{1}{(m/10)+1} \times \\ \left[f_2^{(m/10+1)} - f_1^{(m/10+1)} \right]$$

where m is the slope in decibels/decade, and n_{f1} is the noise value in decibels for the lower frequency limit.

The HP 8662A data offer a good example (the 0.01- to 120-MHz figures are used). For the first decade, 10 to 100 Hz, Equation 6 gives the



4. A SERIES OF SINGLE-TONE distortion measurements were made to illustrate the effects of temperature on the converter's performance.

instrument's power sideband to power signal ratio:

$$e_n(10 \text{ to } 100) = \\ 10^{1.7} \times 10^{-11.3} \times \frac{-1}{0.7} \times (100^{-0.7} - 10^{-0.7}) \\ = 5.73e^{-11} V_{rms} \quad (6a)$$

The complete results are:

$$\begin{aligned} \text{Decade 1} &= 5.73e^{-11} \\ \text{Decade 2} &= 4.97e^{-11} \\ \text{Decade 3} &= 2.281e^{-10} \\ \text{Decade 4} &= 3.437e^{-9} \end{aligned}$$

The ratio SSB power, P_{ssb} , is $3.77e^{-9}$. The total effective phase power produced by the combination of the upper and lower sidebands, P_{rph} , is $4 \times P_{ssb} = 15.08e^{-9}$. The P_{rph} calculation accounts for the fact that complementary sideband terms which are evenly spaced around the carrier add in-phase to double the total phase error produced by either one separately.² The factor of four corrects for the error due to the single-sided integration. It's important to note that the largest contribution comes from the frequency range between 10 kHz and 100 kHz (high-order term).

The power ratio can then be converted to a voltage by:

$$V_n = \sqrt{P_r} \times V_{in rms} \quad (7)$$

Finally, the radian carrier frequency, ω_c , is used in Equation 4 to

solve for jitter:

$$\partial t_j = \frac{V_n}{\omega_c V_{in \text{ rms}}} \quad (8)$$

At 5 MHz and 2 V pk-pk, the jitter is 3.91 ps rms. This figure may seem unacceptable because ADCs can have lower jitter values. However, bandpass filters can remove some of the higher-order noise components, and the finite record length used in spectral analysis reduces the low-order sidebands. A low-order sideband term produces slow variations in the relative phase between the clock and input signals.

For example, when a 4096-point data record is taken at 10 Msamples/s, the total time is only 409.6 μ s. A close-in term will produce only a fraction of its possible carrier phase shift in this amount of time.

The second feature needed in the sources is the ability to lock the reference clock to an external source. This ability eliminates the jitter that would be produced by the absolute phase noise present in each generator. Locking to an external clock also makes possible commensurate sampling, which offers greater freedom in choosing frequencies and improves the accuracy of the results because windowing isn't required.

Unfortunately, most low-noise synthesizers perform poorly in other areas. Unfiltered harmonic distortion is typically in the -30-dBc range. Such instruments might also produce unwanted spurious tones, and may have no provisions for offset control and somewhat coarse amplitude control. In addition, frequency resolution must be considered carefully. For 12-bit systems, resolution should be at least 0.1 Hz because an error in signal frequency prohibits the use of commensurate sampling.

A few sources that work well in ADC evaluation are the Hewlett-Packard HP 8643A and HP 8662A and the Fluke 6080A and 6160B.

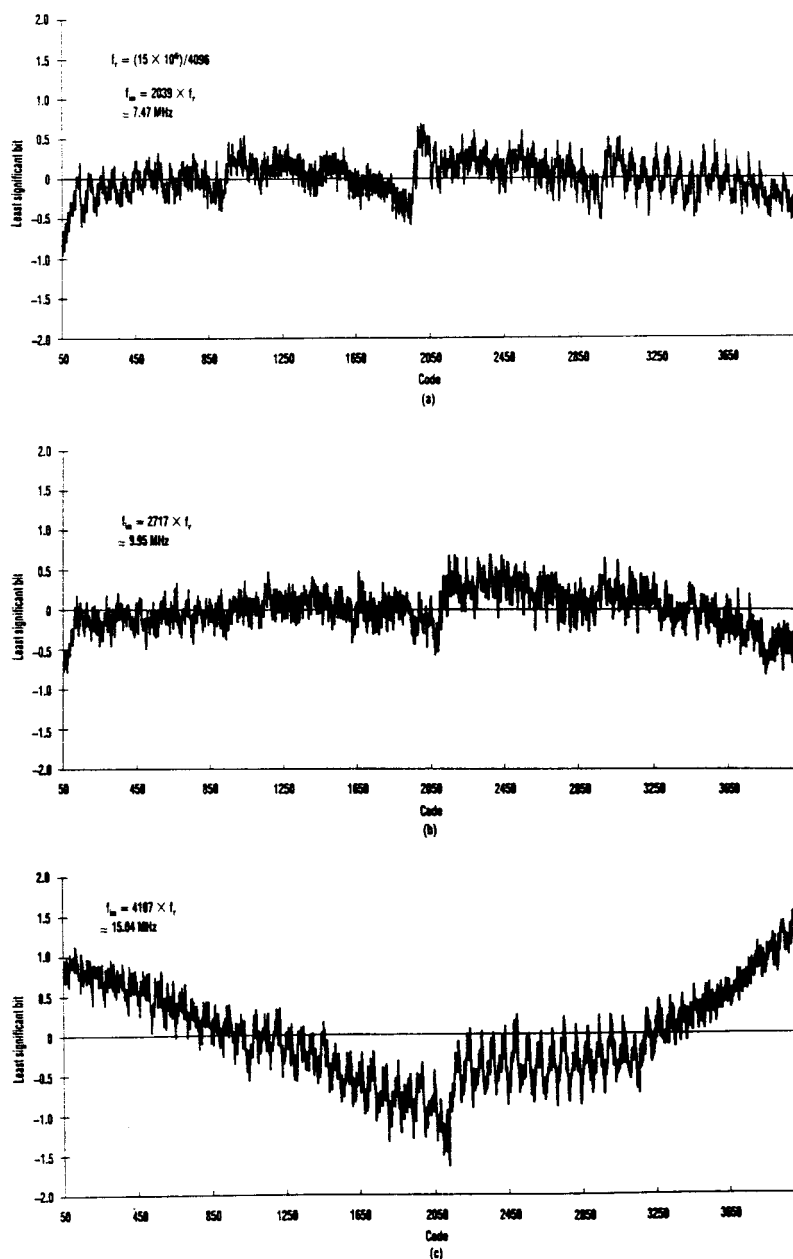
Another area of the test setup that requires attention is the clock-conditioning circuit. Improper conditioning can cause aperture jitter and distortion. Typically, clock signals start out as sine waves, with poor edge rates and the wrong amplitudes for driving ADC clock ports. A simple

conditioning circuit can perform the squaring and amplitude adjustment, but careful routing and grounding is needed to eliminate interference from other circuits (Fig. 3a).

Also troublesome is the noise produced in the test setup's digital output circuitry. In addition, power supplies will contain harmonics created by preamplifiers and analog and dig-

ital circuits in the converter. Consequently, poor power-supply routing or decoupling can produce input-related harmonic noise that modulates the clock switching time and causes distortion.

If the clock conditioning circuit is used on an ADC board, the circuit should be placed close to the converter control pins. The ground connec-



5. THESE PLOTS SHOW HOW integral nonlinearity (INL) graphs can provide information that's hard to glean from spectral plots. In this example, the INL graph for a CLC935 is plotted at 7.47 MHz (a), 9.95 MHz (b), and 15.04 MHz (c). The INL plot goes through a reversal somewhere between 10 and 15 MHz.

tions should be in close proximity to the converter's digital ground, but the supplies must be routed in a star configuration back to the main-power-supply capacitors.

The conditioning circuit can be built with an ECL gate, an ECL-to-TTL gate, or a comparator. No matter which type of component is used, other devices in the package must be wired into the off state, because operating other sections of the device will introduce noise into the clock channel. Results were measured for test jigs that used a copper-clad board with point-to-point wiring (Fig. 3b).

FILTERING IS NEEDED

As noted earlier, the analog output of low-noise sources must be filtered to remove harmonics and broadband noise. The best choice is a high-order passive bandpass filter. Low-pass filters work fairly well, but the broadband and phase-noise components that make it through will degrade the SNR. Regardless of type, the filter order must be high enough to reduce the second harmonic to at least 20 dB below the DUT's expected performance. Insertion loss should be no more than 3 dB, or problems will arise during multi-tone testing, where coupling losses are high.

Distortion in the filters is another potential problem. All connections to the DUT must be properly terminated to reduce reflections, maintain amplitude control, and improve noise immunity. The termination resistors cause substantial currents to flow through the filter's inductive elements. If the inductors start to saturate, they will produce distortion components.

The last electrical concern for the test engineer is the choice of power supplies. During component evaluation, an analog supply must be used to determine the ADC's optimum performance. If the final design calls for a switching supply, it should also be used independently to determine its effects on the system. Supply noise is discussed later on.

The final issue to address is temperature. The high resolution and speed of today's leading-edge converters push power consumption

into the multiwatt range. Some devices may have to be cooled just to keep them within their specified operating range.

Temperature affects reliability as well as repeatability. Ideally, an ADC would be unfazed by temperature, but even the best designs show some variations over temperature. In repetitive tests done to verify the effect of changes to the circuit or system, the part should be brought to the same temperature each time. To illustrate this point, the single-tone distortion versus temperature was measured for a CLC935 (Fig. 4). Tight temperature control and averaging were used to ensure accuracy.

In most cases, a consistent source of cooling air and about five minutes of thermal settling time are all that's needed. A fan rated at 75 cfm and a simple shroud suffices for most converters. For example, a CLC935 in its evaluation board settled out to a final value of 49°C five minutes after power-up in an ambient environment of 23°C. This setup has proved to be very reliable for evaluating design modifications.

Because of the large variety of ADC applications, distortion must be measured in a number of ways. Single-tone spectral analysis provides much information, but integral and differential nonlinearity plots are more useful for imaging and pulse-response work. Applications such as radar required multi-tone testing.

Static dc tests are of little use for either DNL or INL curves. When at or near dc, problems involving track-and-hold acquisition time, power-supply noise rejection, amplifier distortion, and dynamic quantization errors don't show up. What remains are the low-frequency distortion of the analog chain, quantizer device matching, and trim accuracy. Tests at dc can't even supply the upper limit of device performance because different distortion mechanisms can cancel each other as the input frequency is increased.

A CLC935 sampling at 15 Msamples/s offers a good example of INL variations with frequency. For each frequency, the test averaged 250 records of 4096 sample points each. The INL plot reversed itself between the 10- and 15-MHz inputs. Thus, at

some point between these frequencies, the INL curve flattens out and distortion is very low (Fig. 5).

The example histograms were made with unlocked sources and input frequencies chosen to be an odd multiple of the resolution frequency, f_r . These conditions ensure that each sample value in a record represents a unique location on the sine wave.³ A problem could occur because each record contains the same set of unique points. In practice, however, broadband noise and phase jitter will dither the sample values. Running the sources in an unlocked mode further ensures random code coverage.

SINGLE-TONE TESTING

In single-tone testing the sources should be locked, and the analog input signal should go through a bandpass filter. These conditions eliminate harmonics and reduce the various noise sources. If noise is a major concern, the clock signal could be run through a bandpass filter prior to the squaring circuit to remove the broadband noise component.

At this point, a hypothetical situation may best illustrate the ADC testing procedure: The input signals are properly conditioned, the analog input is carefully routed to the DUT input, a termination resistor is placed close to the device, the power supplies are correctly set, the supply leads are relatively short, and the DUT has settled to a reasonable temperature. The first data record is taken, processed by an FFT, and examined using an analysis routine. The results look good, but the noise is 1 dB higher than expected.

At least several possibilities exist:

- the part is bad,
- a filter is defective,
- the source's phase noise isn't within specs, or
- one of the cables is bad.

This scenario assumes that you know the exact expected performance of the particular part being tested. In reality, only the data-sheet spec limits or nominal values may be available. The part's actual SNR could easily be 2 dB better than the limit at 25°C. In any case, if the part is running near or slightly lower than the spec limit, it's time to reassess

assumptions. Check the following:

- Are the clock and analog signals actually locked? Set them to the same frequency and use a scope that's triggered by one signal while you look at the other. Examine the cabling and clock control switches.
- What is the clock signal's amplitude? For a squaring circuit that uses a simple gate, the level should be at least 10 dBm (2 V pk-pk).
- Are the clock and analog frequencies set exactly to the calculated values? In the example, a window wasn't applied to the data, so an error of only 0.5 Hz can lower the SNR from 66.5 dB to 65.5 dB.
- Do the data-acquisition pods latch their inputs at the correct time? Although this problem usually causes gross errors, it's possible that the least significant bit has more delay than the other bits.

The last test to be discussed in this article is for spurious-free dynamic range. The converter's optimal distortion performance is seldom achieved at full-scale input voltage levels. As a result, this test is the same as a single-tone test except that the analog input signal is swept over a range of amplitudes, typically from full-scale (0 dBfs) to -50 dBfs in 1-dB increments.

At each amplitude, the distortion is measured and the worst frequency component sets the value for the dynamic range. The largest component, or spur, is usually a low-order harmonic, but it could be any frequency other than dc or the input frequency. As with single-tone testing, this test should be done over a range of input frequencies.

References:

1. Harris, Fredric J., "On the use of windows for harmonic analysis with the discrete Fourier transform," Proceedings of the IEEE, Vol. 66, No. 1, January 1978.
2. Hewlett-Packard, *Understanding and Measuring Phase Noise in the Frequency Domain*, Application note 207, 1976.
3. Asta, D., *Recent Dynamic Range Characterization of Analog-to-Digital Converters for Spectral Analysis Applications*, Lincoln

Laboratory, Massachusetts Institute of Technology, Lexington, Massachusetts. Project Report AST-14, July 9, 1991.

Joseph D. Giacomini, a designer of fast, low-distortion amplifiers and track-and-hold circuits for data-conversion components at Comlin-

ear Corp., received his BSEE from the University of Minnesota in Minneapolis.

How VALUABLE?	CIRCLE
HIGHLY	541
MODERATELY	542
SLIGHTLY	543

Programmable Linear Phase Filters for A/D Prefiltering Applications

848DOW Series Combines Constant Delay of a Bessel Filter With The Sharp Attenuation of a Butterworth Filter.

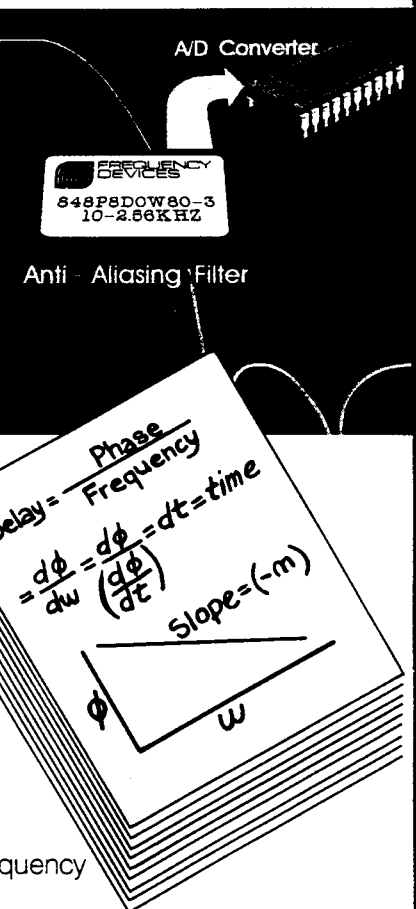
Features:

- 8 pole, 6 zero linear phase lowpass filters
- Digitally programmable corner frequency
- 8 bit (256:1) tuning ratio
- Internally latched control lines to store frequency selection data
- Linear phase response to minimize phase distortion
- Sharp roll-off for anti-aliasing
- Plug in, ready to use, fully finished, filter module
- Five frequency ranges to 51.2kHz

Other Filter Products available:

- Elliptic • Programmable • Fixed Frequency
- Instrumentation • Custom Designs

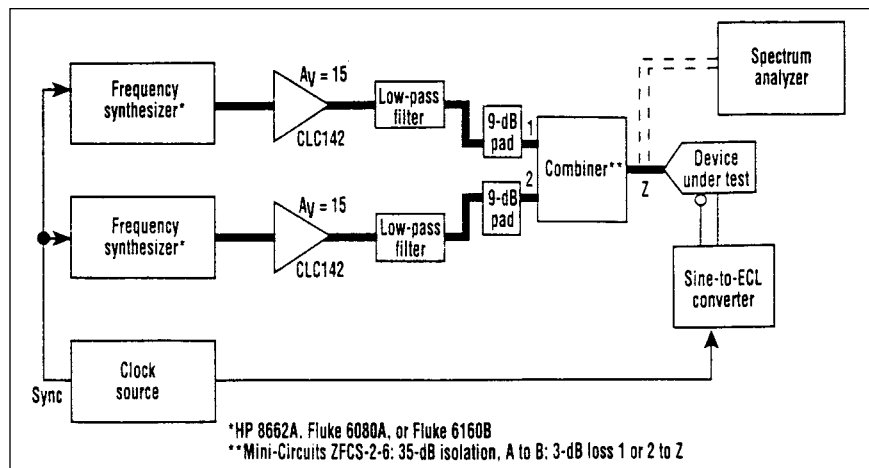
For more information, please call us at
508-374-0761.



FREQUENCY DEVICES

25 Locust Street
Haverhill, MA 01832
(508) 374-0761

CIRCLE 108 FOR U.S. RESPONSE
CIRCLE 109 FOR RESPONSE OUTSIDE THE U.S.



1. TO ASSESS AN ADC'S intermodulation distortion, a relatively complex test setup is needed. The setup must supply a very clean, dual-tone signal.

INTERMODULATION OF MULTIPLE TONES IS THE FACTOR THAT LIMITS ADC PERFORMANCE IN MOST APPLICATIONS.

MOST ADC SYSTEMS REQUIRE INTERMODULATION TESTING

This is the second of two articles focusing on the design and test of high-performance analog-to-digital converters (ADCs). The first article covered the fundamentals of ADC testing and the limitations of test setups. Included were the basic requirements for the digital test system, signal sources, clock conditioning circuits, and filters. Also discussed were the details of single-tone distortion tests. This article describes more advanced test topics and solutions for various problems encountered in ADC testing.

Single-tone linearity tests measure the cumulative distortion mechanisms of an ADC. These tests (ELECTRONIC DESIGN, August 6, p. 55) offer a good basis for comparing converters. In most systems, however, multiple frequencies are present. When multiple tones pass through a nonlinear element, intermodulation products are generated. This intermodulation determines the system's usable dynamic range. System performance is thus controlled by the number of the nonlinearities and their order of occurrence.

A simple dual-tone example illustrates how intermod products

JOSEPH D. GIACOMINI

Comlinear Corp., 4800 Wheaton Dr., Fort Collins, CO 80525; (303) 225-7509.

ELECTRONIC DESIGN **57**
 AUGUST 20, 1992

MULTITONE
ADC TESTING

are created. The example uses a second-order transfer function of:

$$Y(t) = a_1 X(t) + a_2 [X(t)]^2$$

and a two-frequency input of:

$$X(t) = b_1 \cos \omega_1 t + b_2 \cos \omega_2 t$$

where $X(t)$ is the input term; $Y(t)$ is the output term; a_1 and a_2 are the linear and squared gain terms, respectively; and b_1 and b_2 are the amplitudes of the ω_1 and ω_2 terms.

The result is:

$$Y(t) = a_1 b_1 \cos(\omega_1 t) + a_1 b_2 \cos(\omega_2 t) + a_2 b_1^2 \cos^2(\omega_1 t) + a_2 b_2^2 \cos^2(\omega_2 t) + a_2 b_1 b_2 \cos(\omega_1 t) \cos(\omega_2 t)$$

This can be broken down into a linear term:

$$a_1 b_1 \cos \omega_1 t + a_1 b_2 \cos \omega_2 t,$$

a dc error term:

$$(a_2 / 2)(b_1^2 + b_2^2)$$

harmonic terms:

$$(a_2 / 2)[b_1^2 \cos(2\omega_1 t) + b_2^2 \cos(2\omega_2 t)]$$

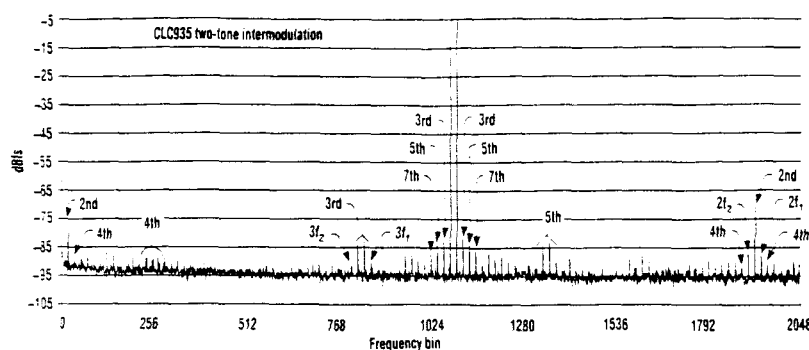
and intermodulation terms:

$$(a_2 b_1 b_2 / 2) \{ \cos[(\omega_1 + \omega_2)t] + \cos[(\omega_1 - \omega_2)t] \}$$

The intermod products in this example are second-order terms. The term's order is determined by the sum of the order of the harmonics needed to create the spurious frequency. A third-order term is created when the second harmonic of one tone interacts with the fundamental of the other.

Table 1 shows a list of second-through fifth-order product terms for a dual-tone system. Using two example frequencies, the table indicates the bin locations for a 4096-point fast Fourier transform. Any term that exceeds the Nyquist frequency, equivalent to bin 2048, is folded into its appropriate bin. The list of possible combinations is limited by the number and order of the system's nonlinearities. Although a substantial number of higher-order terms exist, the largest terms are usually below the sixth order.

To evaluate intermodulation, the test setup must supply the device under test (DUT) with a very clean dual-



2. THESE SAMPLE TEST RESULTS show the intermodulation distortion products for a CLC935. The evaluation used the test setup in Figure 1 and the frequencies in Table 1. To reduce the noise floor, the spectral measurements were averaged.

frequency signal (Fig. 1). The amplifiers in the setup provide gain and, more importantly, buffer each frequency synthesizer from variations caused by the other source. Otherwise, each synthesizer's amplitude-control loop might try to adjust the signal level to correct for the error current produced by the other unit's signal. The resulting signal-level modulation would produce intermod products similar to those caused by a nonlinear output impedance.

The attenuation placed between the amplifiers and the combiner improves isolation between the amplifier outputs, preventing one output from generating error currents in the other. Nonlinearities in the amplifiers' outputs would otherwise create intermod products.

The combiner itself has finite isolation. So to eliminate the possibility of creating intermod products in the coupler, low-pass filters remove individual distortion products in the signals before they're combined. Using one filter after the coupler would compound the problem by reducing the isolation provided by the coupler, because it requires a matched impedance on its output. The filter's input impedance is close to the desired value at low frequencies but becomes much worse near the stopband frequency. As with all tests, the setup requires high-quality coaxial cables properly terminated at the DUT.

Four slightly different test setups were evaluated. The configuration in Figure 1 delivered the best overall results (Table 2). By placing a band-

pass filter in each signal path and a low-pass filter after the coupler, the results would improve slightly. The bandpass filters would remove the second-order difference term, and the low-pass device would eliminate the third-harmonic distortion terms. A quick test was done with the addition of a low-pass filter after the combiner. The test showed that the third-harmonic terms were reduced to the level of case 3, and the intermod products that were checked showed little change.

A CLC935 was evaluated using the test circuit of Figure 1 and the test frequencies listed in Table 1. To reduce the noise floor, spectral averaging was employed (Fig. 2).

A test related to intermodulation is noise-power ratio. In this test, the input to the DUT is a spectrally flat noise signal that's passed through a narrow band-reject filter. Converter intermodulation creates spurious components that land in the input signal's notched region. The level of this noise regrowth is important in frequency-multiplexed communication systems.

Some new applications for high-resolution converters require a wide large-signal bandwidth (LSBW). These uses include direct intermediate-frequency (IF) sampling, direct video sampling, and precision pulse measurement. In the case of IF sampling, the information bandwidth may be on the order of 10 MHz centered at 70 MHz. Sampling the IF signal will cause information to be folded back into the Nyquist band in a

MULTITONE
ADC TESTING

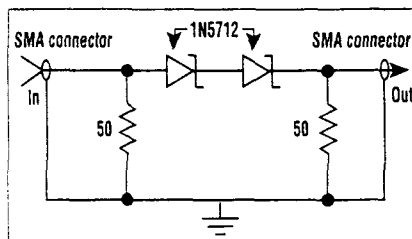
predictable manner. As long as sampling frequencies are chosen properly and the information bandwidth is less than the Nyquist bandwidth, the information will be preserved.

When there's direct video sampling, the information resides in the baseband region. The sample rate must be high enough to accommodate the largest signal components without folding them back to lower frequencies. For pulse measurement, the effective time resolution can be increased by repetitive sampling, but a wide bandwidth is needed to provide any meaningful information. The limit to repetitive sampling's effectiveness was evident in some of the early digital oscilloscopes: Time resolution was in the picosecond range, but the bandwidth of the scope's input circuitry was less than 100 MHz. When high slew-rate pulses were examined, they all looked the same because the scope was acting as a filter.

Even though a wide LSBW is a necessity, limiting the bandwidth helps reduce noise. But in the area of noise, it's the small-signal performance that's critical, because the amplitude of broadband noise is relatively low. It's important to note that a wide small-signal bandwidth (SSBW) works to ensure fast, accurate settling to step inputs.

In both the large- and small-signal cases, the critical point is at the sampling node or nodes. If a track-and-hold circuit is used, the point of interest is the hold-capacitor node. In flash converters, it's the sum of the comparator nodes that must be quantified. When a track-and-hold is present, the bandwidth can be measured by placing the converter in the track mode and measuring the track-and-hold output. This value includes the response of the hold amplifier, which buffers the hold-capacitor node. The measured bandwidth is a composite of the two responses.

An alternative method is to measure the response using the output data from the converter, which is the only way to evaluate a flash converter. To do so, the designer must take a record for each test frequency. The amplitude can be measured directly from the time data or from a frequency spectrum. Spectral informa-



3. TO IMPROVE the settling performance of the pulse generator used in the ADC test, the instrument's output can be run through a simple pulse-shaper circuit. With the orientation shown, a positive level sets the starting amplitude.

tion is better because the fundamental's amplitude is easy to identify. To minimize the number of tests, the selected frequencies should provide an even spacing on a log scale.

When measuring LSBW, the amplitude should be set to 1 dB below full scale (-1 dBfs). This signal is sufficiently large, and yet it allows room for small values of peaking that could occur over frequency. For SSBW tests, the exact amplitude is less critical. The level should be low

enough so that slew rate isn't a limiting factor, yet large enough for noise not to become a problem. The test setup is the same as the single-tone test setup described in the first article except that no filter is needed.

Imaging and pulse-measurement applications also require various time-domain tests. For instance, if two adjacent pixels in an image record are at opposite ends of the converter's input range, a step-response measurement is critical. In a radar system, the input may be overdriven, and poor recovery means lost information. Other situations may require very flat long-term settling. Most applications can be covered by a few basic tests: slew rate, short-term settling, long-term settling, and overvoltage recovery.

Slew-rate measurements are easy to make using a repetitive sampling technique: A high slew-rate square wave is sampled at a rate slightly lower than the square wave's frequency. Each successive sample occurs at a point on the wave that's slightly later than the previous sam-

TABLE 1: DUAL-TONE INTERMODULATION PRODUCT TERMS

$f_1 = 15 \text{ MHz}/4096$ $f_1 = 1079 \times f_r \approx 3.951 \text{ MHz}$ $f_2 = 1097 \times f_r \approx 4.017 \text{ MHz}$			
Frequency term	Actual bin	Folded bin	Approximate actual frequency
$2f_1$	2158	1938	7.90 MHz
$3f_1$	3237	859	11.85 MHz
$2f_2$	2194	1902	8.03 MHz
$3f_2$	3291	805	12.05 MHz
Second-order:			
$f_1 + f_2$	2176	1920	7.97 MHz
$f_1 - f_2$ or $f_2 - f_1$	± 18	± 18	65.9 kHz
Third-order:			
$2f_1 - f_2$	1061	—	3.89 MHz
$2f_1 + f_2$	3255	841	11.92 MHz
$2f_2 - f_1$	1115	—	4.08 MHz
$2f_2 + f_1$	3273	823	11.99 MHz
Fourth-order:			
$2f_1 - 2f_2$ or $2f_2 - 2f_1$	± 36	—	131.8 kHz
$2f_1 - 2f_2$	4352	256	15.94 MHz
$3f_1 - f_2$	2140	1956	7.84 MHz
$3f_1 + f_2$	4334	238	15.87 MHz
$3f_2 - f_1$	2212	1884	8.10 MHz
$3f_2 + f_1$	4370	274	16.00 MHz
Fifth-order:			
$3f_1 + 2f_2$	5431	1335	19.89 MHz
$3f_1 - 2f_2$	1043	—	3.82 MHz
$3f_2 + 2f_1$	5449	1353	19.95 MHz
$3f_2 - 2f_1$	1133	—	4.15 MHz
$4f_1 + f_2$	5413	1317	19.82 MHz
$4f_1 - f_2$	3219	877	11.79 MHz
$4f_2 + f_1$	5467	1371	20.02 MHz
$4f_2 - f_1$	3309	787	12.12 MHz

MULTITONE
ADC TESTING

ple. As a result, the sample record traces the shape of the input signal with a time resolution equal to the difference in the periods of the convert and analog signals. The output data displays the net slew rate, SR_{net} , produced by the converter with a finite-slew-rate input signal. The input signal's slew rate must be measured and used to compute the correct slew rate of the converter being tested.

For a desired 10-ps resolution with a fixed ADC sample rate of 15 MHz, the analog input-signal frequency should be 15.00225 MHz. To get this kind of resolution, two synthesizers must be locked together to generate the initial test frequencies. The convert signal can be squared-up using a logic gate or comparator. The analog signal requires more slew improvement than a simple circuit can provide, but a pulse generator with a slew rate twice as fast as the DUT supplies a suitably conditioned signal. Under these conditions, the net slew rate will be about 11% below the converter's actual slew rate.

For simplicity, the analog signal can be considered to be centered around 0 V. Once the signals are applied, the computer obtains a data record with the appropriate slewing edge. SR_{net} should be measured in a narrow region around zero, where the slewing is relatively constant.

The input signal's slew rate must be carefully measured using a fast oscilloscope. Because the input signal must be terminated at the DUT, a low-impedance divider probe is suitable. A good attenuation choice is divide-by-20, created by a 950- Ω resis-

tor in series with a properly terminated coaxial cable. This arrangement produces only a 1-k Ω resistive load in parallel with about 1 pF.

If this low-impedance probe is used, the speed-limiting factor will be the scope. For an accurate measurement, the scope's slew rate must be at least twice as fast as the signal being measured. The engineer can approximate the correction factor for the oscilloscope from its rise-time specification. The first step is to assume a simple exponential response for the step response:

$$Y(t) = V_o(1 - e^{-t/\tau})\mu(t)$$

where V_o is the input step voltage, τ is the time constant, and $\mu(t)$ is the step function.

Then for a specified rise time, τ_r , of 300 ps (10% to 90%):

$$\tau_r = t_2 - t_1$$

where

$$t_1 = -\tau \ln \left[1 - \frac{Y(t_1)}{V_o} \right]$$

and

$$t_2 = -\tau \ln \left[1 - \frac{Y(t_2)}{V_o} \right]$$

Solving for τ :

$$\tau = 0.455\tau_r = 136 \text{ ps.}$$

The slew rate at the 50% point is then:

$$\frac{\partial V}{\partial t} = \frac{\partial Y(t)}{\partial t} = V_o \left(\frac{1}{\tau} \right) e^{-(t/\tau)}$$

where $t = -\tau(\ln 0.5)$. Then:

$$\delta V / \delta t = V_o / 272 \text{ ps}$$

And the scope's slew rate is:

$$SR_{scope} = V_o(3676) \text{ V/s}$$

The correct SR can now be calculated with reasonable accuracy:

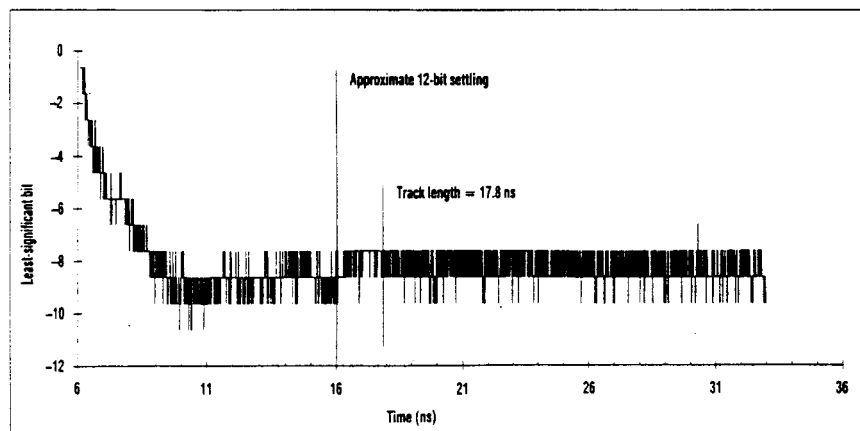
$$SR \approx \frac{1}{\sqrt{\left(\frac{1}{SR_{net}}\right)^2 - \left(\frac{1}{SR_{in}}\right)^2}} \quad (1)$$

where SR_{net} is the net slew rate of a system that's driven by a signal with a slew rate equal to SR_{in} . The engineer must first use Equation 1 to correct the measured slew rate of the analog input signal. Then the equation has to be applied using the corrected slew rate for the input signal, and the net slew rate obtained from the time record to compute the actual converter slew rate.

Although pulse generators work well in ADC slew-rate measurements, they don't have the fine settling characteristics needed for step-response tests. Most fast pulse generators are only specified for 8-bit settling. But settling performance can be greatly improved if the instrument's output is driven through a simple pulse shaper (Fig. 3). With the orientation shown, the initial level is set with the positive voltage and the final value is ground. The negative potential is set to ensure that the diodes aren't turned on by ringing in the input signal. If the input and output terminals are reversed, a positive-step signal can be generated.

The circuit's settling time depends on the time it takes the input signal to turn off the diodes, and on the discharge time of the diode capacitance through the output resistor. Any ringing on the input signal will couple through the reverse-bias diode capacitance to the output resistor. Attenuation will be fairly high, however, because the series capacitance of two diodes is very small.

For a reasonably clean input signal (less than 10% overshoot), this circuit will settle in less than 10 ns to 12 bits. The speed can be improved by using unprotected Schottky diodes. The 1N5712 devices employed in the circuit are hybrids that have a pn junction diode built in parallel with a Schottky barrier diode to improve



4. THIS SETTLING RESPONSE plot for a CLC935 displays a one-cycle step-input acquisition. The time scale starts at the point where the data starts to transition.

MULTITONE
ADC TESTING

the reverse breakdown. The current levels required for a 1-V step will start to turn on the protection diode. Unlike a Schottky diode, a pn diode will store charge, which greatly increases the effective capacitance.

Repetitive sampling is again used to obtain a trace of the converter's response. The time data actually maps the acquisition response of the converter. If the ADC includes a track-and-hold circuit, the waveform may present erroneous results. Once the analog and convert signals slip in phase to where the input is low when the track-and-hold goes into track, the same value will be obtained for each successive sample.

The problem arises if the track-and-hold can't fully settle to a step input in one track period. For a properly settled track-and-hold, the data asymptotically approaches some final value. The track-and-hold hasn't settled if the response includes a strong discontinuity roughly one track period after the signal starts to transition. To accurately perform this test, the track time must be increased. This can usually be accomplished by lowering the sample rate, but then the analog input frequency must be reduced accordingly.

Figure 4 shows the fine settling region for a CLC935 at its designed sample rate of 15 Msamples/s. The time scale is referenced to the point where the data starts to transition. The plot shows that the signal approached its final value at about 12 ns and appears to settle to 12 bits in 16 ns. Determining the 12-bit settling point is somewhat difficult because the step used in this test covers only half of the input range and the noise level is about 2 least significant bits (LSBs) pk-pk. With a half-scale step, settling must be measured to one-quarter of an LSB. To reduce the noise, several time records could be manually aligned and averaged.

The overvoltage recovery test is simple. Added recovery time shows up as a reduction of the low-level duty cycle. Therefore, the engineer merely increases the positive amplitude to achieve the desired overdrive condition and then measures the change in the duty cycle. The delay is the difference between the input signal's duty cycle and the duty cycle

TABLE 2: TEST SETUP IMD PERFORMANCE*

Frequency	Test Case			
	Figure 2 (No. 1)	No amps (No. 2)	One filter (No 3.)	Resistive splitter (No. 4)
$f_1 = 1079f_s \approx 3.95 \text{ MHz}$	+3 dBm	—	—	—
$2f_1 \approx 7.90 \text{ MHz}$ (bin 2158 into 1938)	-104 dBm	-104.4 dBm	-104 dBm	-106 dBm
$3f_1 \approx 11.85 \text{ MHz}$ (bin 3237 into 859)	-93 dBm	-93 dBm	-107 dBm	-87.8 dBm
$f_2 = 1097f_s \approx 4.02 \text{ MHz}$	+3 dBm	—	—	—
$2f_2 \approx 8.03 \text{ MHz}$ (bin 2194 into 1902)	-106 dBm	-101 dBm	-107 dBm	-104 dBm
$3f_2 \approx 12.05 \text{ MHz}$ (bin 3291 into 805)	-97 dBm	-96 dBm	-106 dBm	-91 dBm
$f_1 + f_2$ (bin 2176 into 1920)	-100 dBm	-96 dBm	-99 dBm	-97 dBm
$f_1 - f_2 = f_2 - f_1$ (bin 18)	-93 dBm	-98 dBm	-93 dBm	-95 dBm
$2f_1 - f_2$ (bin 1061)	Noise floor	-106 dBm	-83 dBm	-95 dBm
$2f_1 + f_2$ (bin 3255 into 841)	Noise floor	-105 dBm	-101 dBm	-102 dBm
$2f_2 - f_1$ (bin 1115)	Noise floor	-107 dBm	-83 dBm	-99 dBm
$2f_2 + f_1$ (bin 3273 into 823)	Noise floor	-107 dBm	-98 dBm	-107 dBm
Noise floor	-111 dBm	-109 dBm	-111 dBm	-110 dBm
Amplitude settings				
AF ₁	0 dBm	15.3 dBm	15.3 dBm	3.4 dBm
AF ₂	0.3 dBm	15.8 dBm	15.8 dBm	3.7 dBm

*Measured in low-distortion mode on an HP 3588A with high-resolution zoom; 10-dBm input, 0.088-Hz resolution bandwidth, four measurements averaged.

measured using the output data.

Aperture jitter is indirectly obtained by measuring the sampled noise and slew rate of an ADC, or a track-and-hold circuit, while it's sampling a rapidly slewing waveform. To ensure extremely low residual phase jitter, a common source generates the convert and analog signals (Fig. 5). The engineer adjusts the phase of the two signals by varying cable lengths in each signal path so that the analog signal is sampled at the midpoint of its transition. Consequently, any variation in the sample time causes a change in the sampled value. The deviation from the nominal value depends on the sampling circuits, slew rate, and timing jitter.

Therefore, the effective timing jitter can be calculated by:

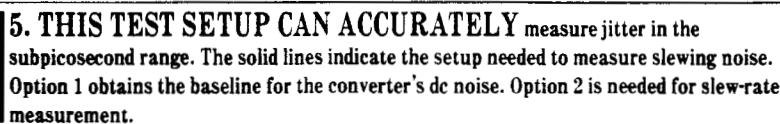
$$\tau_j = V_n / \text{SR} \quad (2)$$

where V_n is the noise voltage caused by jitter and SR is the slew rate.

Repetitive sampling is again used to measure the slew rate. In this case, the net slew rate is desired.

To obtain the noise voltage, the engineer can either compute the rms value for a sampled record or measure the output spectrum of the track-and-hold circuit, if its output is available. If a data-record calculation is used, the dc, or mean, value must first be removed. The noise value obtained during the slewing case contains an error term caused by the broadband noise combined with the converter's quantization noise. Thus, the noise must be computed for the slewing case and for a dc case in which only a termination resistor is connected to the analog input. The noise component caused solely by jitter, in V rms, can then be approximated by:

$$V_n = \sqrt{(V_{\text{slew}})^2 - (V_{\text{dc}})^2} \quad (3)$$



HOW VALUABLE?	CIRCLE
HIGHLY	534
MODERATELY	535
SLIGHTLY	536

Customer Design Applications Support

National Semiconductor is committed to design excellence. For sales, literature and technical support, call the National Semiconductor Customer Response Group at **1-800-272-9959** or fax **1-800-737-7018**.

Life Support Policy

National's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of National Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, a) are intended for surgical implant into the body, or b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



National Semiconductor Corporation

1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe

Fax: (+49) 0-180-530 85 86
E-mail: europe.support@nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Francais Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.

13th Floor, Straight Block
Ocean Centre, 5 Canton Road
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.

Tel: 81-043-299-2309
Fax: 81-043-299-2408

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Mobile Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Transportation and Automotive	www.ti.com/automotive
Video and Imaging	www.ti.com/video

TI E2E Community Home Page

e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2011, Texas Instruments Incorporated