DP83223,DP83840A,DP83858

Application Note 1087 Cascaded Unmanaged Repeater Applications

Literature Number: SNLA003

Cascaded Unmanaged Repeater Applications

National Semiconductor
Application Note 1087
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1.0 INTRODUCTION

The purpose of this application note is to provide guidelines and recommendations for designing a multi-port unmanaged stackable hub using National's 12-port DP83850 and 8-port DP83858 Repeater Interface Controller "100RIC™" chips. The simplicity of cascading multiple repeaters is demonstrated in this note. In this document, it is assumed that the system designer is already familiar with the interface between the 100RIC and the RJ45 connector. For further information, refer to Application Note AN-1069 100BASE-TX Unmanaged Repeater Design Recommendations.

2.0 OVERVIEW

Figure 1 depicts the constituent parts of a repeater box in an unmanaged configuration. For applications that require more than 12 ports, more boxes can be connected together through the Inter-Repeater bus to form a larger network in a simple and modular fashion *(Figure 2)*. A management module could also be placed in one of the repeater boxes for managing of the stack. (Discussion of the management module design is beyond the scope of this application note.)

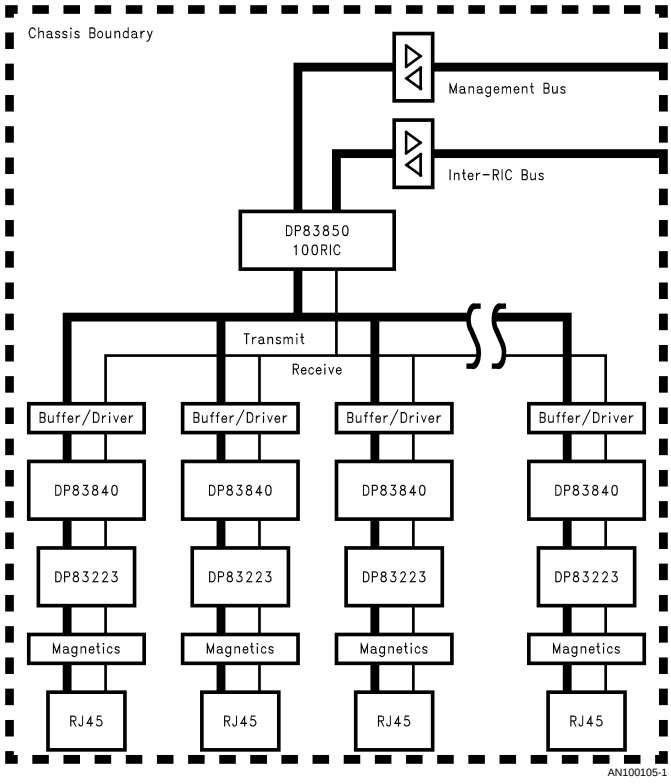

FIGURE 1. A 12-Port Repeater System

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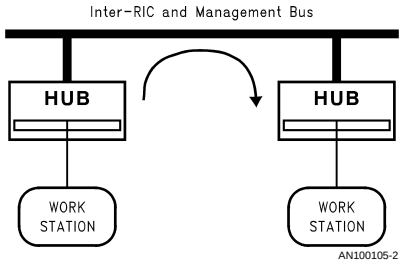


FIGURE 2. Cascading Multiple Repeater Units

3.0 METHODS OF INTER-CONNECTING REPEATERS

Fundamentally, repeaters can be connected by either or both of the following methods:

1. Through the inter-repeater link and/or
2. Through the ports.

Class I vs. Class II Repeaters

A logical repeater unit is a term that is used to describe a system where the repeaters are cascaded together through the inter-repeater link (Inter-RIC bus in the case of 100RIC). For example, when a packet is received by a port on 100RIC #1 from N1 *(Figure 3)*, the repeated packet to N2 and N3 leave both the 100RICs at approximately the same time, resulting in only one repeater delay between the received and transmitted packets.

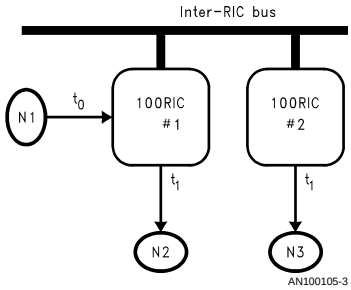


FIGURE 3. A Logical Repeater System

However, when the repeaters are connected to each other by their ports, then multiple repeater delays are introduced *(Figure 4)*. A packet sent by N1 to the 100RIC #1 is received at time t0 and then repeated to both N2 and the 100RIC #2 at time t1 (one repeater delay). However N3 receives the same packet at t2 as a result of the additional delay in the second repeater.

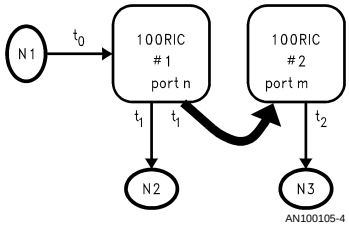


FIGURE 4. Class II Repeater

In 100 Mbps terminology, a system with two repeater delays is referred to as a Class II repeater.

Class I and Class II are defined by IEEE (section 27.1.1.3) as:

Class I: A type of repeater set specified such that in a maximum length segment topology, only one such repeater set may exist between any two DTEs within a single collision domain.

Class II: A type of repeater set specified such that in a maximum length segment topology, only two such repeater sets may exist between any two DTEs within a single collision domain.

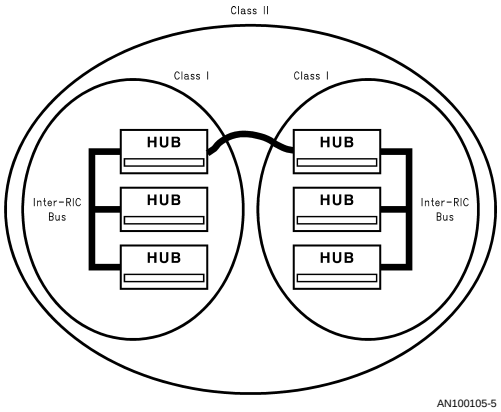


FIGURE 5. Stackable Repeaters in a Class II System

For the purpose of this applications note, the mechanism in which the repeaters are cascaded through the inter-RIC bus (Class I), is considered.

4.0 INTER-RIC BUS OPERATION

The Inter-Repeater Bus ("IR bus") provides all the necessary signals to make the whole stack a logical unit adhering to IEEE 802.3µ standard's repeater section.

The Ethernet data packets received by one 100RIC are transmitted to other 100RICs in the system through the IR bus. This bus therefore provides the means for:

a) receiving data from and transmitting data to the other 100RICs, and

b) determining whether more than one 100RIC are active at the same time (collision scenario), and if so, letting all the repeaters know of a collision occurrence somewhere in the network.

Before going into details, it is necessary to note that in this application note, ABT class devices are recommended for at least two reasons:

1. There may be applications where the boards are often removed and inserted while the backplane is still active. In such cases, the insertion and removal of a board creates glitches and voltage level changes on the backplane. To prevent these kind of problems, ABT is a suitable class.
2. When the devices that interface with the backplane power up or down, their connection to the bus will ideally maintain a high impedance state. The output enable circuitry associated with these devices controls the output state of the interface device during power up and down. This prevents intermittent low impedance loading or glitch generation commonly associated with conventional CMOS and Bipolar devices.

The following sections describe the necessary components (external to the RIC) for interfacing two or more repeaters.

4.1 Vector Identification

IR_VECT(4:0) and RID(4:0) work together to accomplish the tasks of Port N recognition and collision detection. (Port N is defined as the port which becomes the source of packet reception after idle.) Here is a brief explanation of these two sets of signals:

Repeater Identification Number (RID)

RID provides the unique vector for the IR_VECT[4:0] signals used in Inter Repeater bus arbitration. These bits are also used to uniquely identify each repeater for serial register accesses. The RID value is latched on the rising edge of the active low reset signal.

IInter Repeater Vector

When there is reception on a port the DP83850CVF drives a unique vector based on the RIDs onto these vector lines. The vector on the IR bus is compared with the Repeater ID (RID). The DP83850CVF will continue to drive the IR bus if both the vector and RID match.

RID (Repeater ID) is an input, and upon power up, the user selectable ID is available inside the repeater for sampling. The chip's unique ID (RID) is then compared to IR_VECT open collector signals.

Figure 6 shows the conditions that cause an open collector vector signal to be asserted on the backplane bus.

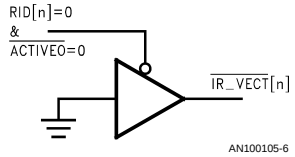


FIGURE 6. RID and $\overline{\text{IR_VECT}}$ Relationship

As indicated, if the RID[n]=1 (and therefore disabling the driver), and the repeater is receiving on a port, then the $\overline{\text{IR_VECT}}$[n] value would be 1 due to a pull-up on this pin. If RID[n]=0, then the driver is enabled and a zero is driven out on the $\overline{\text{IR_VECT}}$[n] signal.

Furthermore, as shown in *Figure 7*, if only one 100RIC is receiving packets on a local port, there is an equality between the ID and the vectors. However, when multiple 100RICs are driving their IDs into the vector bus, at least one of the 100RICs will detect the collision and assert the IR_COL_OUT signal which is detected by other 100RICs. When the collision signal is asserted, then all the repeaters will tri-state their Inter-RIC signals to prevent contention.

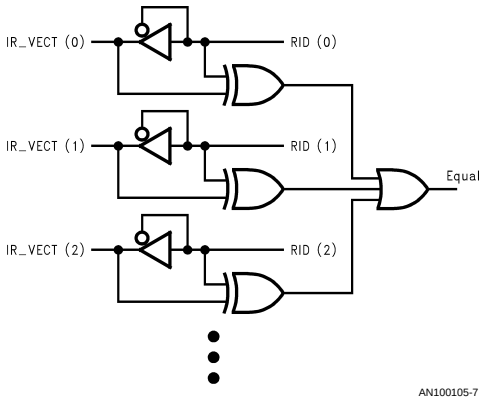


FIGURE 7. Conceptual $\overline{\text{IR_VECT}}$ Qualification

As an example, assume that two repeaters with RIDs equal to RID#1=00010 and RID#2=00011 are connected through the Inter-RIC bus. The following diagrams depict the values of $\overline{\text{IR_VECT}}$ signals over the backplane in this scenario.

Figure 8 represents a repeater with ID=00010 that receives a packet and drives its ID onto the backplane. Later another repeater with ID=00011 receives a packet. However the backplane ID stays as 00010. After the collision ends, since the repeater with ID=00010 is not active anymore, the backplane ID reverts to 00011 for the active duration of the second repeater.

Figure 9 shows two repeaters with IDs as in *Figure 8*, but in this example, the repeater with ID=00011 drives the backplane first.

As another example, assume that the two repeaters have RIDs equal to RID#1=00010 and RID#2=00001. The vector value seen on the backplane would be all zeros (00000) during the collision activity, as shown in *Figure 10*.

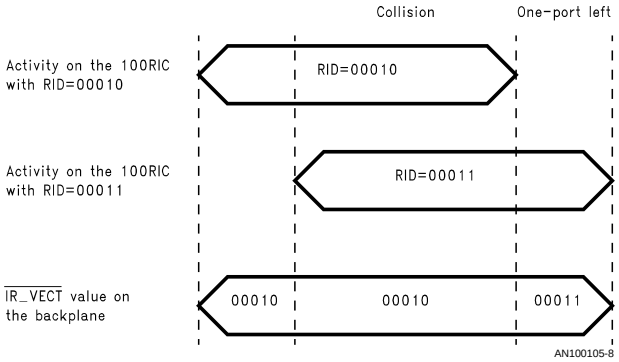


FIGURE 8.

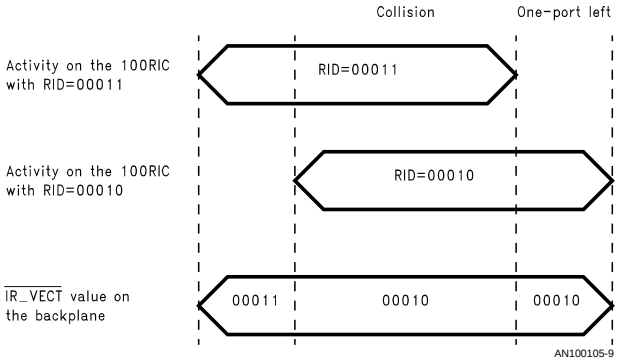


FIGURE 9.

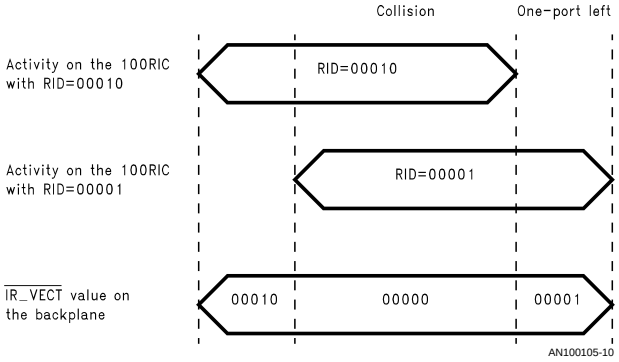


FIGURE 10.

4.1.1 Circuitry for the Inter-RIC Vector Identification

To make sure proper vector identification and collision detection is done, the scheme in *Figure 11* is recommended:

A receiving 100RIC asserts a set of signals, one of which is $\overline{\text{ACTIVEO}}$. This signal is followed by IR_VECT(4:0) signals driven out on the bus.

The 100RIC has to see its feedback vector within the $\overline{\text{ACTIVEO}}$ assertion. If this feedback is different than the 100RIC's ID, then the collision signal is asserted.

Figure 11 represents the mechanism of operation. For simplicity, consider only $\overline{\text{ACTIVEO}}$ and IR_VECT4 signals (the same operation applies to the rest of the IR_VECT signals).

When the network is idle ($\overline{\text{ACTIVEO}}$=1), then the IR_VECT4 sees the value that has been set by the RID4. For example, if RID4=1, then IR_VECT4=1, and if RID=0, then IR_VECT4=0. In this case, the buffers are disabled and IR_VECT4_BP=1.

When the 100RIC receives a packet on one of its ports, then ACTIVEO=0 which enables the ABT125 buffers and allows the IR_VECT4 to see/sample the IR_VECT4_BP value.

When the network is idle, the backplane value is always 1Fh (due to pull ups on IR_VECT_BP lines). The only time the backplane has a different value than 1Fh is when a 100RIC is active and its vectors are put on backplane through the enabled buffers. In this case, the 100RIC sees its own vector.

However, if two 100RICs drive their vectors on the bus, one of the 100RICs detects a change of vector value. Assume one 100RIC has IR_VECT0=1 and another 100RIC has IR_VECT0=0. The only RIC that sees a change of value in its vector is the one with IR_VECT=1, since its value changed from 1 to 0 (0 is driven by the other RIC).

After detection of an unexpected vector value, a collision signal is asserted to all the 100RICs connected to the Inter-RIC bus.

Another alternative to the circuit in *Figure 11* is to use RID(4:0) signals instead of IR_VECT(4:0) at the input of the 'F32 OR gates. In this case, the vector identification stays unchanged as described earlier.

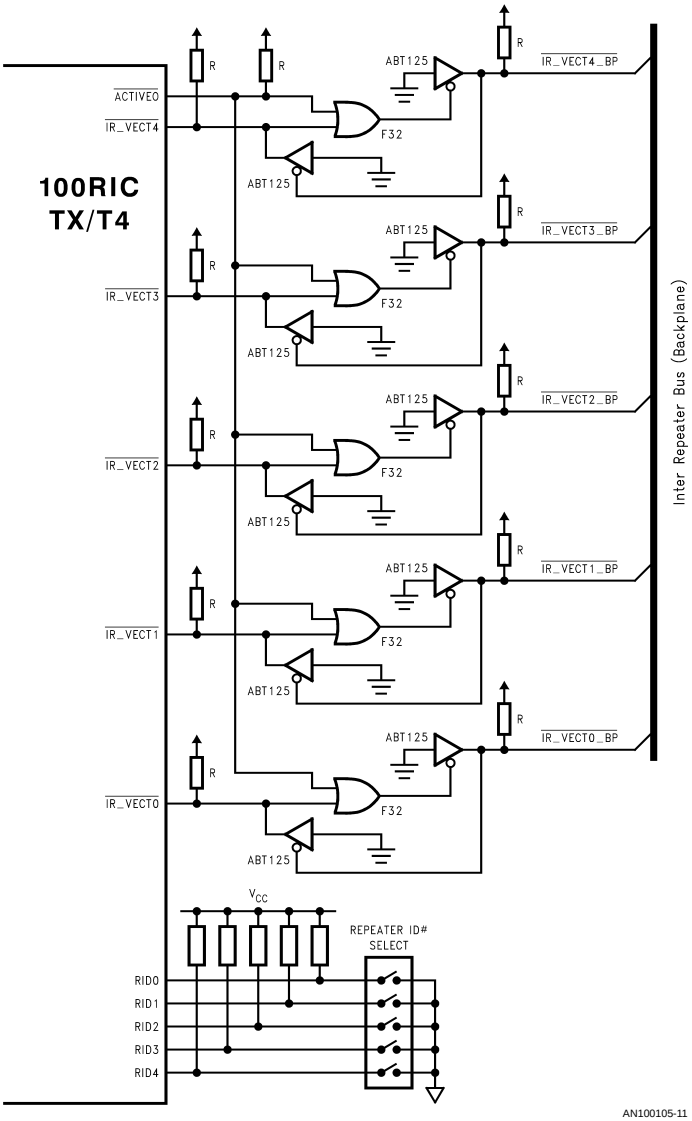


FIGURE 11. Circuitry for Vector Identification on the Inter-RIC Bus

4.2 Activity/Collision Detection and Notification

In a multi-RIC application, the repeater with Port N drives a signal which is sensed by the other repeaters, notifying them of a network activity. This is done through open-collector/active low IR_ACTIVE and ACTIVEO signals. In other words, the receiving RIC drives its ACTIVEO signal on the bus which in turn is sensed by the IR_ACTIVE signal of the other 100RICs (refer to *Figure 12*).

There are two ways a repeater can determine whether a collision has occurred. One is if more than one port become the source of reception, i.e., the presence of multiple CRS signals. The second one is if there are multiple vector IDs on the backplane. In either case the repeater experiencing the collision asserts the collision signal (IR_COL_OUT) which is sensed by all other repeaters through their IR_COL_IN signal (refer to *Figure 12*).

4.2.1 Circuitry for the Activity/Collision Detection and Notification

Figure 12 shows two examples of an equivalent circuit. In *Figure 12A* two different ICs (ABT125 and ABT244) are used whereas in *Figure 12B*, only ABT125 IC is used for both outgoing and incoming signals. It would be up to the system designer to choose either of these or any other option suitable for his/her design needs.

Note: Pull-up resistors are required on all Inter-RIC and backplane signals.

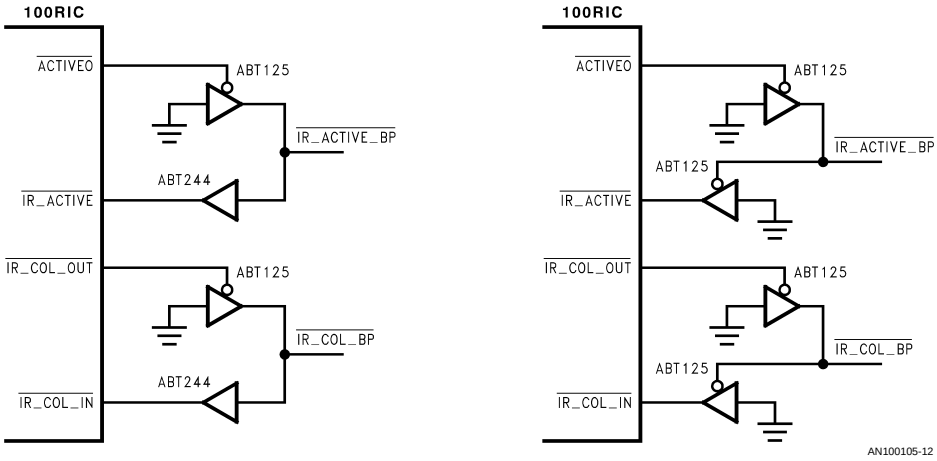


FIGURE 12. Options for Activity and Collision Detection on the Inter-RIC Bus

4.3 Data and Clock Connections over the Inter-RIC and Management Bus

When there is no activity on any of the repeater's ports, the direction of the IRD signals is from the backplane toward the 100RIC. This is so that the repeater can see activities from the backplane and therefore repeating that activity to its local ports. As soon as a 100RIC receives data on one of its ports however, the IRD signal lines for that repeater change direction (now from 100RIC to backplane) supplying the data to other repeaters connected to backplane. The circuitry in *Figure 13* shows the necessary components for proper cascading. It should be noted that this scheme of buffering needs to be done for each RIC in a cascaded architecture.

4.3.1 Circuitry for the Data and Clock Connections over the Inter-RIC and Management Bus

Figure 13 shows that the bi-directional buffer is enabled through the NOR of IRD_ODIR and ACTIVEO signals. On the other hand, *Figure 14* shows the elimination of the NOR gate and instead utilizing the IRBUS_EN signal for controlling the buffer. Again these two circuits accomplish the same objective.

Note that although *Figures 13, 14* do not show any signal termination, proper pull ups/downs are required.

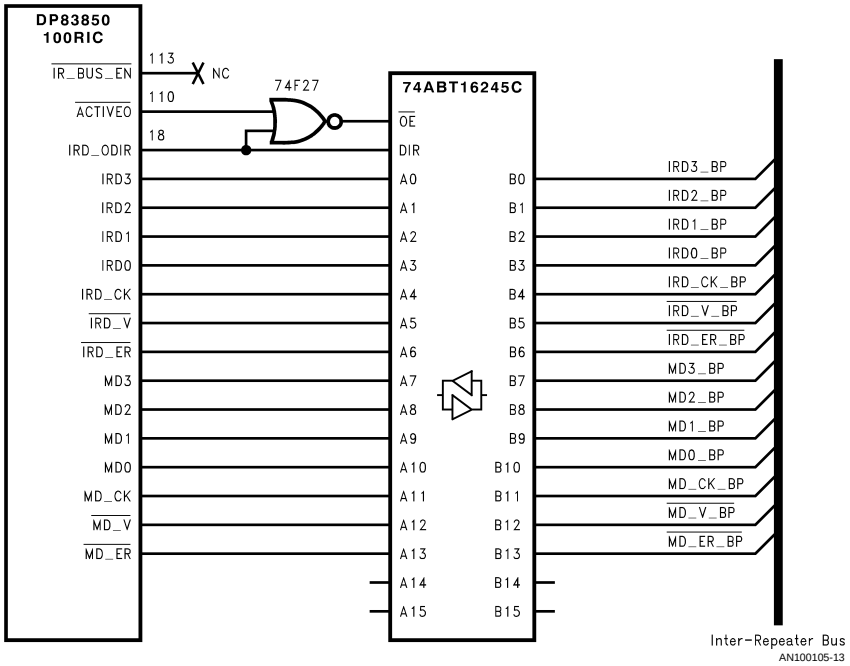


FIGURE 13. Inter-RIC Signal Buffering Using $\overline{\text{ACTIVEO}}$ and IRD_ODIR

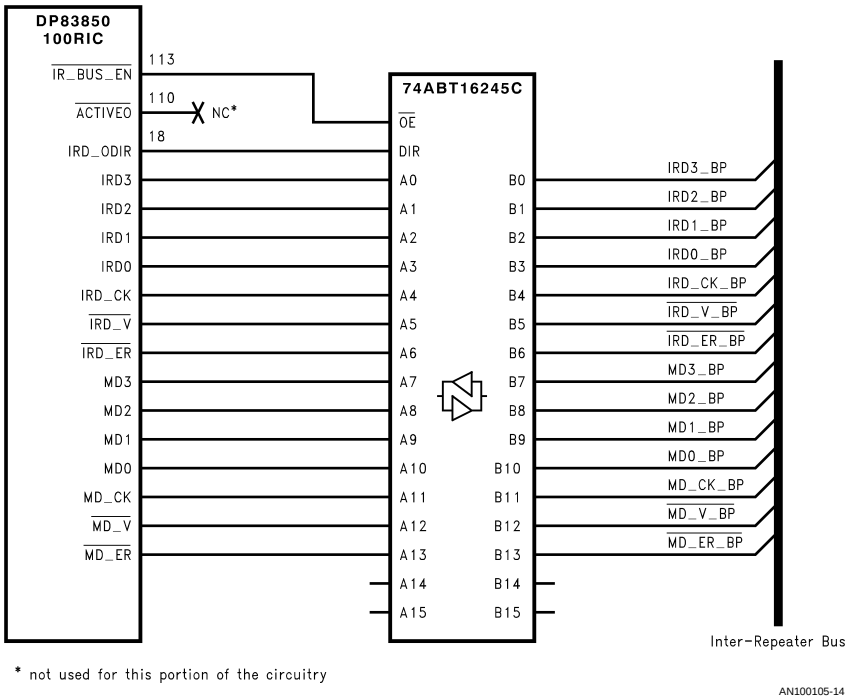


FIGURE 14. Inter-RIC Signal Buffering Using $\overline{\text{IR_BUS_EN}}$

5.0 OTHER RECOMMENDATIONS

1. As a reminder, each $\overline{IR_DV}$ and $\overline{M_DV}$ signal should be pulled high by a 4.7 kW resistor on the backplane/stack side.
2. If there are relatively large overshoot (due to reflection for example) on the Inter-RIC Clock (IRD_CLK) signal, the integrity of packets could be affected, leading to packet corruption. To prevent this adverse effect, a series resistor in the range of a few hundred ohms (typically 330W) can be placed on the IRD_CLK signal to dampen the overshoot effects.

6.0 STACK TIMING ANALYSIS

When the repeater is intended to be used in a stack configuration, signal delays and skews between the boxes in the stack should be taken into account. Specifically, proper set up and hold time should be maintained as a packet is received on a port and is transmitted over the IR Bus and is received by other repeaters. *Figure 16* shows the path that a packet traverses in a stack environment.

To determine whether data and clock have proper set up and hold time as the packet is received by the 100RIC (point F in *Figure 15*), some calculation is required. *Figure 16* shows the delays and skews imposed on the clock and data as they go through different devices:

This table starts off with the DP83840A's RX_CLK to RXD[4:0] minimum and maximum delays (10 ns and 30 ns respectively). These numbers are then used to calculate the worst case setup and hold times for the DP83840A device. From there on, the delay and skew through each device, as applicable, are taken into account to calculate the final setup and hold times as the packet traverses through different components. As seen in *Figure 16*, the data and clock are retimed after the latch, providing plenty margin as required by the other 100RICs in the stack (2 ns set up and hold time for the data to clock on the Inter-RIC bus).

Note that the calculation in *Figure 16*, allows for 3.0 ns skew for the backplane. This skew could be higher depending on the backplane architecture. As long as the Inter-RIC bus requirements are met, even with few nano-second increase of skew, the design should operate properly.

6.1 Usage of 74F174 Flip/Flop

To guarantee the latch operation, a 74LS174 "D Flip-Flop with clear" is recommended. The flip-flop's clear input should be the logical OR of all of the RXEs asserted by the 100RIC. A single PAL™/GAL™ could be implemented to provide this logic as shown in the following figure.

The reason for the OR of all RXEs is that during collisions, all RXEs are de-asserted by the 100RIC, forcing the flip-flop's output to become low. This in turn guarantees that the repeater does not enter an undefined state.

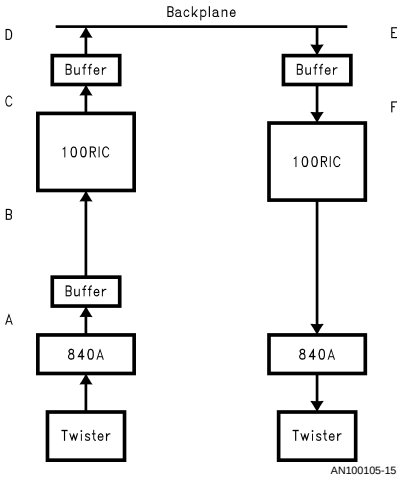
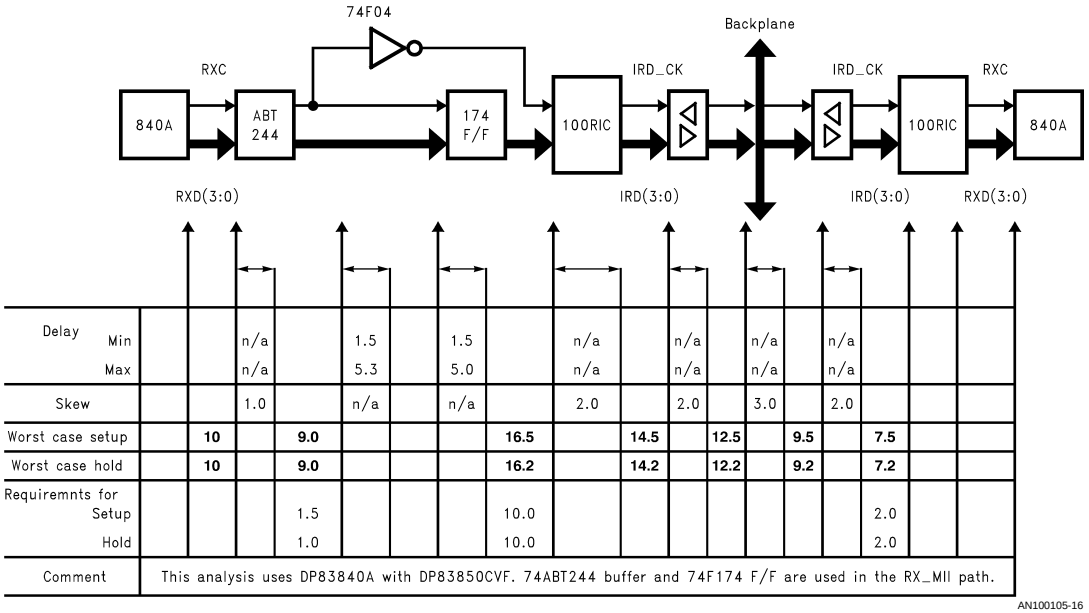


FIGURE 15. Data Path in a Stack Environment



Delay Min			n/a		1.5		1.5		n/a		n/a		n/a		n/a		
Max			n/a		5.3		5.0		n/a		n/a		n/a		n/a		
Skew			1.0		n/a		n/a		2.0		2.0		3.0		2.0		
Worst case setup		**10**		**9.0**				**16.5**		**14.5**		**12.5**		**9.5**		**7.5**	
Worst case hold		**10**		**9.0**				**16.2**		**14.2**		**12.2**		**9.2**		**7.2**	
Requiremnts for Setup				1.5				10.0								2.0	
Hold				1.0				10.0								2.0	
Comment	This analysis uses DP83840A with DP83850CVF. 74ABT244 buffer and 74F174 F/F are used in the RX_MII path.																

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FIGURE 16. Timing Analysis for the 100RIC Stackable Implementation

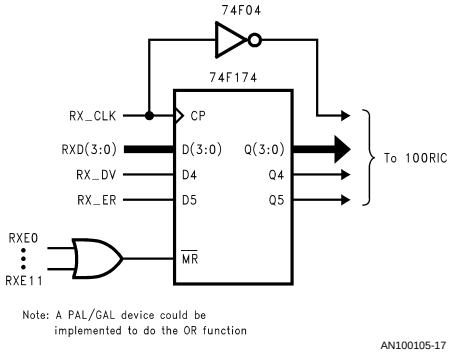

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FIGURE 17. 74F174 Implementation on the RX MII between 840A PHY and 100RIC

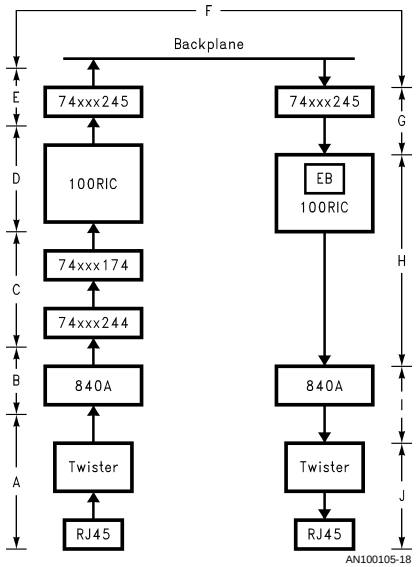

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FIGURE 18. Delay Paths in a Stackable System

7.0 BIT BUDGET ANALYSIS

With both the 74XXX541 buffer and the 74XXX174 flip-flop in the RX MII path (between the 840A and the 100RIC), a class II bit budget analysis is done according to the *Figure 18*. In this configuration, a packet traverses through two 100RICs and the cascade (backplane) bus.

All delays used in the following figure and tables are the actual components delays with the exception of the backplane delay. This delay could vary depending on the complexity and the type of components used for the cascade circuitry.

Two nano-seconds (2 ns) backplane delay is used for the calculation of the SOP and the SOJ.

7.1 Start Of Packet Delay (SOP)

The start of packet propagation delay (SOP) for a repeater is defined as the time delay between the start of the packet on an input port to the start of the same packet on its output ports.

Table 1 shows the total data delay through a normal and collision free scenario.

TABLE 1. Class II SOP Calculation

Point	Data Path	Delay (ns)
A	RJ45/TWISTER™ to 840A	5.5
B	840A Mil to 244	209.0
C	244 to 100RIC through 174 F/F	16.6 (3.6+11.0+2.0)
D	100RIC to 245	10 + 2.0 (skew)
E	245 to Backplane Connector	3.6 + 2.0 (skew)
F	Backplane to 245	3.0 (0.5m cable)
G	245 to 100RIC	3.6 + 2.0 (skew)
H	100RIC to 840A Mil	100.0 + 40.0 (EB + TX)
I	840A to TWISTER™	62.5
J	TWISTER™ to RJ45	6.5
	TOTAL	466.3 (46.63 BT)

Legend for *Table 1*

TWISTER™	DP83223
840A	DP83840A
100RIC	DP83850
174	74xxx174
244	74xxx244
245	74xxx245

7.2 Start Of Jam Delay (SOJ)

The start of collision jam propagation delay (SOJ) for a repeater is defined as the time delay between the start of the second packet on an input port to the start of the jam out on all its ports.

Table 2 shows the data delay when the network experiences a collision.

TABLE 2. Class II SOJ Calculation

Data Path	Delay (ns)
RX TWISTER™ to 840A RX	5.5
840A RX to 840A CRS Assertion	175.0
840A CRS to $\overline{\text{IR_COL_OUT}}$ + IRB Delay to 100RIC	80.8
Collision Synchronization of $\overline{\text{IR_COL_IN}}$	60.0
100RIC TX to 840A TX Mil	40.0
TX Delay through TWISTER™	24.0
TX Delay through TWISTER™	6.5
Total	391.8 (39.18 BT)

8.0 IR BUS SIGNAL CONNECTIONS FOR AN UNMANAGED SINGLE APPLICATION

Figure 19 represents the necessary Inter-RIC signal connections for a 12 port un-managed stand-alone architecture. As with any other design, all open collector signals are tied to V_{CC} through resistors.

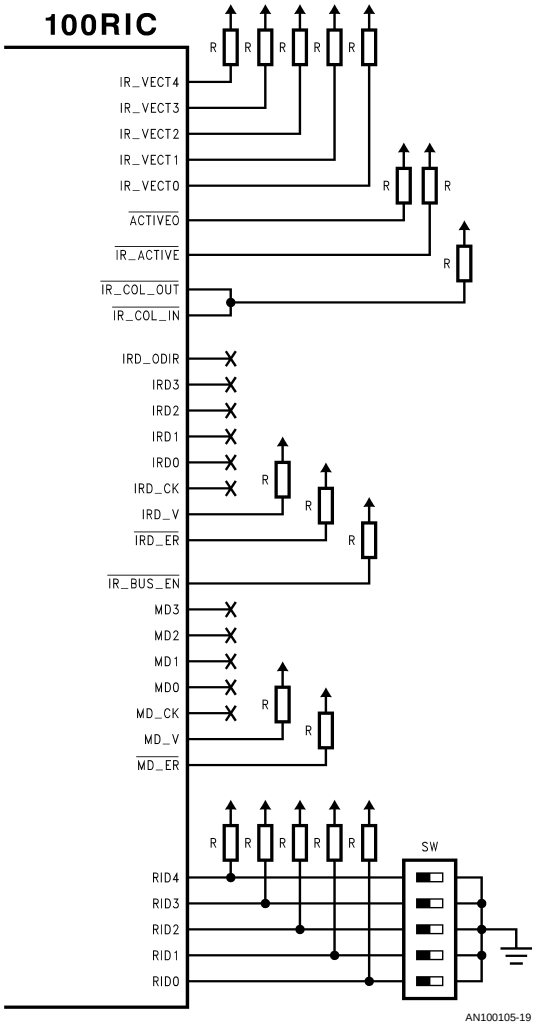

FIGURE 19. Inter-RIC Bus Signal Connections in an Unmanaged Single Repeater Application

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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