

OBSOLETE



Application Report
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AN-1347 PCB Layout Techniques for Adaptive Cable Equalizers

ABSTRACT

Without a doubt, when it comes to achieving good performance, the Texas Instruments CLC014 and CLC012 adaptive cable equalizers present the greatest challenges to digital video design engineers. Difficulties with these devices often arise because it is not fully appreciated that they are, in fact, high performance analog devices and not simple digital devices. More specifically, the CLC014 and CLC012 are high-gain, wide-band, analog, RF, AGC amplifier-filters. In order to obtain the best possible performance and avoid common difficulties, suitable care must be given to developing the circuit and PCB layout. This application report is a guide to proven effective techniques that, when used in a design, can eliminate troublesome behavior and provide the best possible circuit performance.

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1 Equalizer Difficulties and Their Causes

The gain-frequency plot in [Figure 1](#) indicates the maximum equalization response of the CLC014 and CLC012. The gain at 600MHz is about 43dB. This maximum gain is achieved when the cable length is a maximum. But the equalizer also operates at maximum gain and bandwidth when the input is not connected to a cable. No-signal is a minimum signal condition. In both cases, the equalizer gain is a maximum because the signal is a minimum. So, it should be easy to understand how even small amounts of unwanted interference signals, when amplified under these conditions, can greatly upset equalizer operation. Likewise, the need for a good PCB layout is clearly evident.

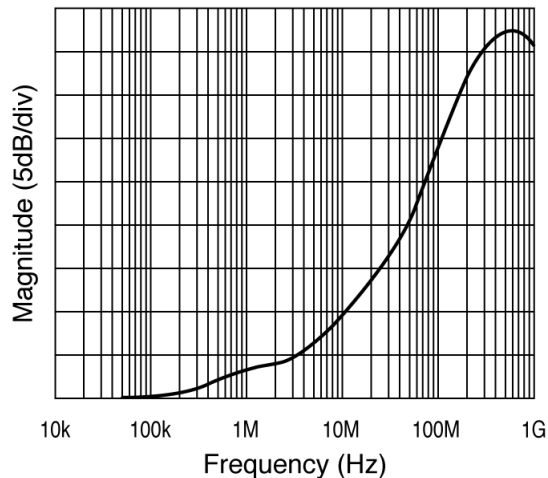


Figure 1. Maximum Equalization Response

Some of the most common problems with these equalizers that result from improper circuit and PCB layout are:

- Failure to equalize the maximum cable length for a given data rate
- Corrupted data when cable lengths are long but less than the maximum length
- Spurious or random output data when the input is not connected to a cable
- Carrier detect (or LOS) indication when no cable is connected

All of these symptoms can usually be traced to interference problems in the system enclosure and on the PCB. Among the most common sources of interference are:

- Reception of radiated EMI signals originating in the system enclosure or on the PCB
- Power supply or other noise coupling to the inputs by way of the input network component mounting pads
- Crosstalk between the input network and other nearby networks
- Coupling between the input and output circuits of the equalizer
- Crosstalk and noise coupling into the AEC circuit

2 Preventing PCB Problems

The most effective way to prevent these problems is to adopt circuit and PCB layout techniques like those used to combat ESD and EMI/RFI. These techniques boil down to three basic things:

- Isolation of the equalizer inputs, input networks and the AEC circuit from on-card, high level signals
- Shielding of input and AEC networks from external signal pickup
- Suppression or attenuation of unwanted interference signals

Figure 2 is the schematic diagram of the recommended equalizer circuit. A well drawn schematic is a useful guide to achieving a good layout. Of note here is the placement of the equalizer's output load network near the inputs of the device at the receiving end of the transmission lines. This load network does two things: It provides the proper DC levels for the outputs of the equalizer; and it terminates the transmission lines.

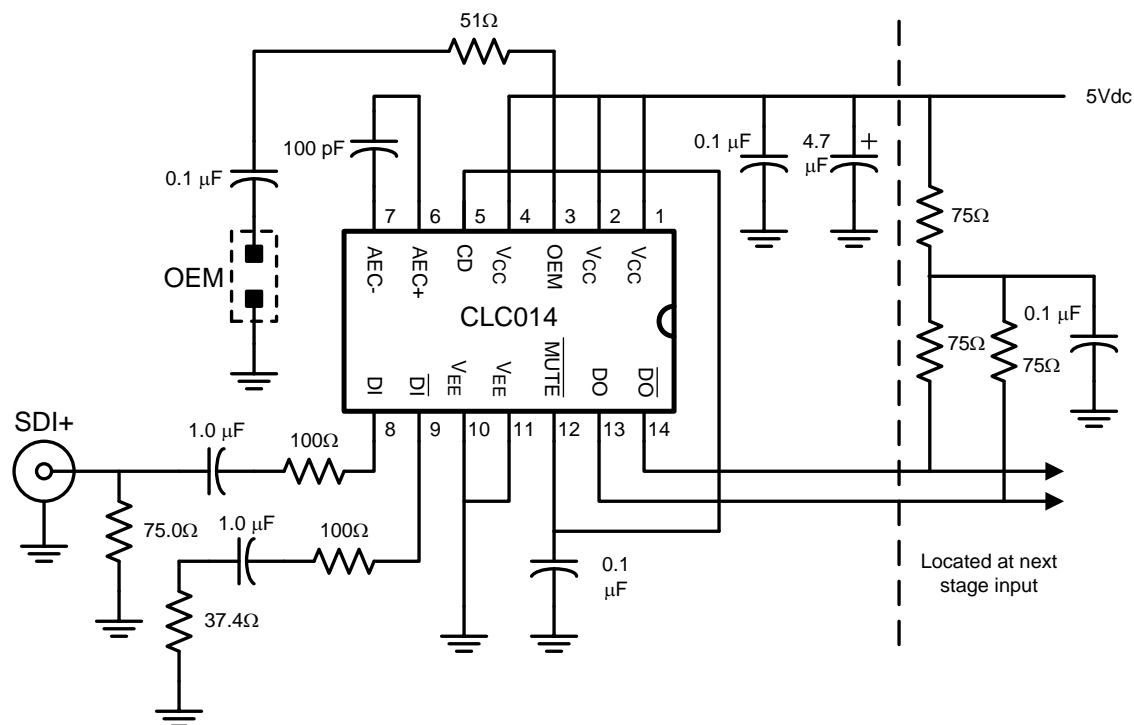


Figure 2. Typical Equalizer Circuit

At this point a word about the requirement for using multi-layer PCBs is in order. Devices such as the CLC012 and CLC014 are prime examples of devices requiring PCBs with four or more layers. Separate transmission line layers, usually microstrip, and inner layer power plane sandwiches are elements needed for these devices. It is almost impossible to achieve the needed isolation and shielding for high-gain, wide-band analog devices with double-sided PCB stackups. Power-ground layer pairs, or sandwiches, should be specified with thin dielectrics, 6mils or less, so that the intrinsic capacitance of the sandwich is as high as practical. Maximizing power supply layer capacitance provides very effective high frequency bypassing. It is possible to achieve 100pF/in² (15.7pF/cm²) or more with conventional PCB dielectric materials in sandwiches 10mils (0.25mm) and less in thickness. This capacitance can increase effective attenuation of the power supply decoupling by 20dB or more. Moreover, it costs nothing to include in the circuit.

Elements connecting to the power or ground layers such as bypass capacitors, termination resistors, collector load resistors, and V_{CC} and V_{EE} pins of ICs, should employ two vias for the pad-to-plane connection. Dual vias reduce interconnect inductance by up to half. In the case of bypass capacitors, this extends the effective operating frequency range of the component. Inductance in component connections to power and ground planes should be minimized wherever possible.

One very important rule that must never be violated when using the CLC012 or CLC014: Multiple V_{CC} or V_{EE} pins must not share a common via. The pins must be individually connected to the power or ground planes with separate vias.

Figure 3 shows the equalizer circuit in PCB layout form. This layout shows several things that should be done to isolate the input networks and the entire circuit from unwanted stray signal pickup. The dark-shaded area around the input networks and the AEC capacitor indicates where copper in the plane layers is removed. Removing this portion of the planes reduces the stray parallel-plate capacitance formed between the component mounting pads, the component bodies and the planes. If present, this capacitance can couple power supply noise into the inputs or the AEC feedback loop.

The technique of moating around a circuit achieves isolation. Moating is simply the removal of strips of copper in the inner plane (and surface plane) layers. The moats are represented by the dark-shaded strips enclosing the equalizer circuitry. Note that the moat is not continuous around the entire circuit. A copper area at the end of the equalizer farthest from the input connector is left. This copper connects the equalizer circuit to the remainder of the planes. The moats act to prevent currents from adjacent circuits from directly reaching the equalizer circuit. The long path length between the adjacent circuits and the equalizer input circuits increases signal attenuation in the planes serving the circuits. This low-pass filtering reduces or eliminates signals which would otherwise reach the equalizer inputs.

Frequently, a cable driver may be located adjacent to the equalizer to provide a signal loop-back function. The cable driver output signals are usually much larger than the signal being received by the equalizer. The large amplitude output signal can couple into the equalizer input causing data corruption or unwanted output. Isolation and shielding can be used to prevent the cable drive signal from interfering with the equalizer input.

Two things can be done to reduce effects from radiated RFI pickup:

1. the input can be ringed by a shield
2. the input circuit layout can be made symmetrical

A grounded shield ring is shown in Figure 3 that completely encloses the input circuits of the equalizer. Note that the ring is well grounded at several points including the V_{EE} power supply pin. (In this example, a positive V_{CC} is assumed). Also, the common mode cancellation afforded by the differential input of the equalizer can be used to improve interference suppression. RFI will be a common-mode signal if it is received equally by both inputs as is usually the case. A symmetrical input circuit layout with balanced termination impedances, similar to that shown, will tend to equalize RFI signals reaching both inputs. The common mode rejection of the input differential amplifier will thus cause the cancellation of most or all of the interference signal.

The clearance area around the input connector center pin should also be noted. Clearance around the center pin through the planes should be quite wide. This will reduce stray capacitance which can adversely affect input return loss. The exact dimensions and placement of the clearance will depend on the type of connector; but in general, the ring's radius should extend to the adjacent ground pin(s) of the connector. The minimum clearance around the via should be 30 to 40 mils.

Note that the AEC pins and capacitor are isolated from other circuitry. Doing so prevents unwanted signal interference with the integrator and filter control circuits of the equalizer.

Figure 4 shows how additional isolation and shielding may be obtained through the use of copper floods on the outer layers of the PCB. Similar layout recommendations as those for guard rings apply in this case. Void areas in the inner plane layers under the input networks and moating as shown in Figure 3 are also indicated. To be an effective shield, the copper floods must be connected to other inner layer ground planes at about 1-cm intervals.

Equalizer circuits using the PCB layout and noise control techniques described in this note perform better and experience far fewer difficulties than layouts not using them. Adoption of these techniques will not increase the cost of the PCB. Moreover, these techniques will improve product performance and reduce the number and cost of PCB redesigns to fix equalizer interference and performance problems. The major benefits are: fewer product development headaches and quicker product time-to-market.

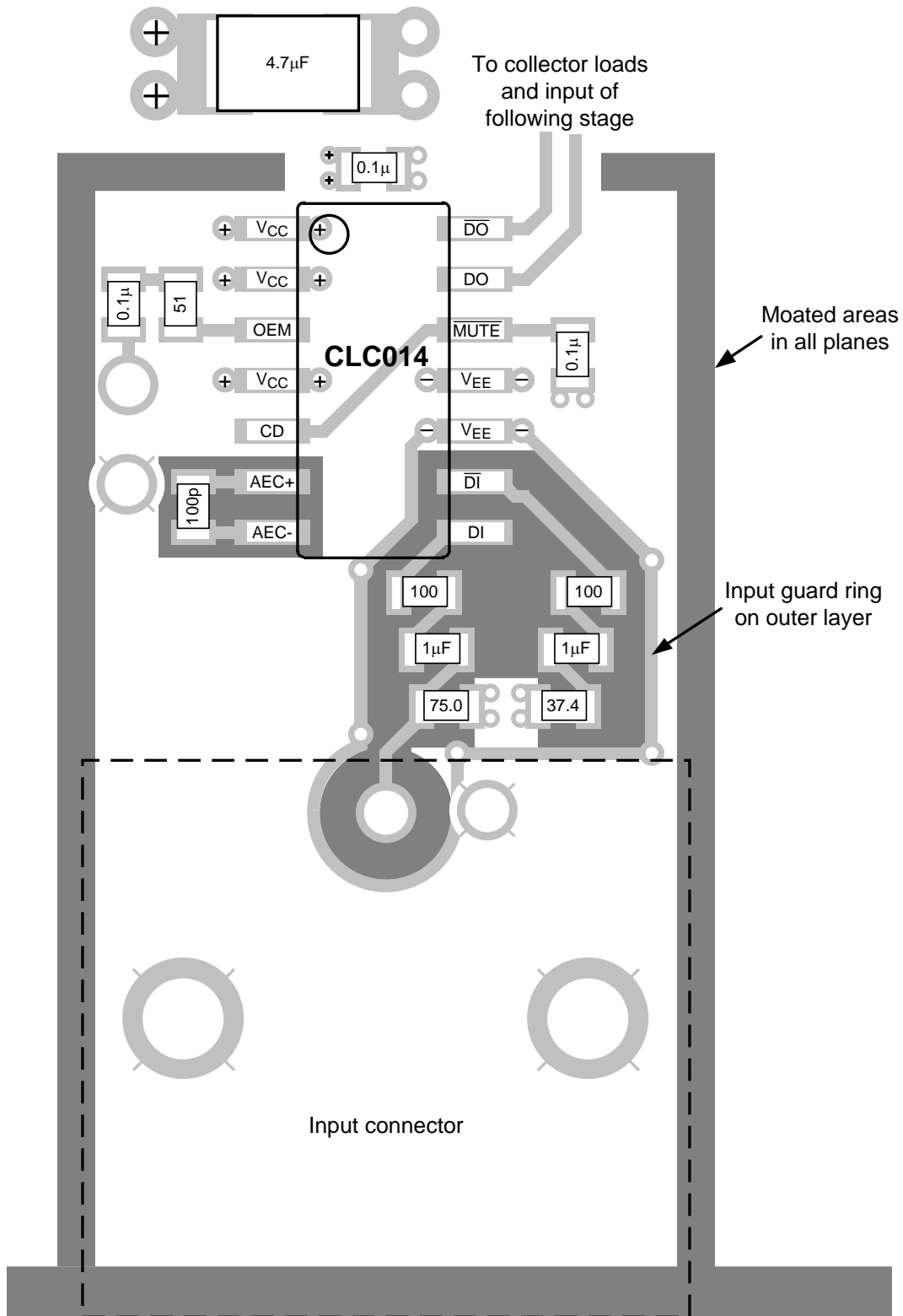


Figure 3. Isolating Critical Circuit Elements

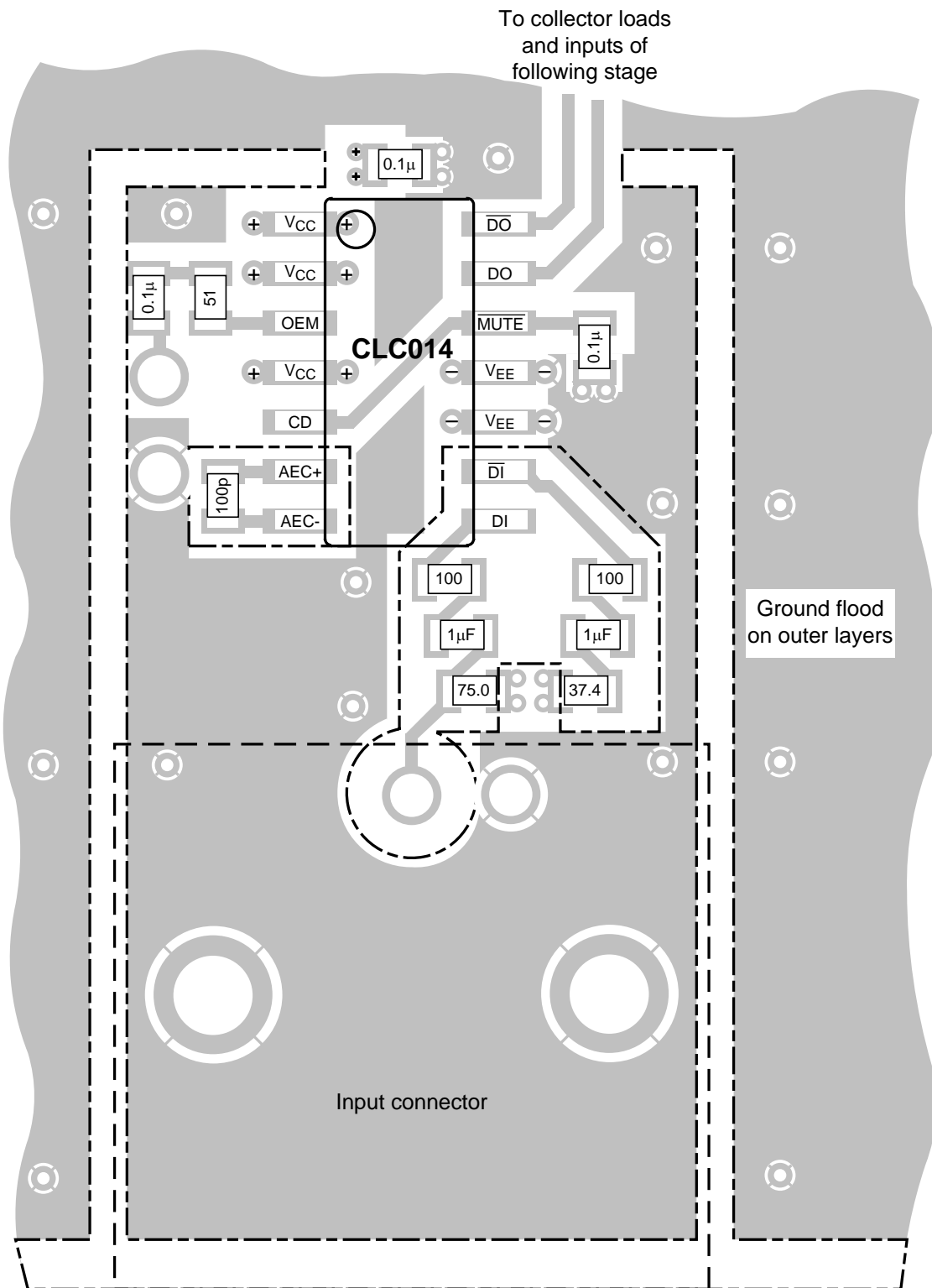


Figure 4. Shielding with Copper Floods

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