Handset Architecture with Integrated Framestore/SourceDriver IC

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42.2: Handset Architecture with Integrated Framestore/Source Driver IC

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Abstract

The application of TFT displays for handset applications requires new display system architectures in order to achieve desired power targets and to enable handset features such as integrated cameras. There are significant benefits to embedding a framestore into the source driver chip of a handset display system. This paper explores these benefits with respect to typical handset usage models, power consumption, memory architecture, camera/video functions, and other advanced techniques for display power optimization. In particular, both the system power consumption and the source driver interface bandwidth requirement will be greatly reduced. These and other benefits are discussed, and the architecture of a TFT handset display system incorporating such an embedded framestore is described.

1. Introduction

Due to the high refresh rates required by the display module within a handset, the power and data bandwidth requirements of the interface between the baseband processor and the TFT-LCD display module are relatively high. These will be significantly reduced if a framestore is embedded into the display module.

If this embedded framestore is integrated into the source driver IC of the display module, there will be yet additional benefits that will minimize system power and cost: further reduction in power dissipation, opportunities to optimize the memory architecture, and improved integration of other imaging and video functions within the system. The architecture of a two-chip TFT-LCD chipset that includes such an integrated framestore will be presented.

A detailed method for analyzing the power consumption of the display system has been developed, and will be used to demonstrate the system power reduction that is achieved by the two-chip architecture.

2. Background

Among other things, an imaging-enabled mobile phone handset contains a baseband processor and/or a graphics controller that generates image data, a video or still camera that generates additional image data, and a TFT-LCD system to display the image data. A typical display system contains 176x220 ~ 176x240 RGB pixels and can display 18-bit color (6-bits each for red, green, and blue channels). Figure 1 shows a 176x240 display system that does not integrate the framestore with the source drivers. This system uses three ICs and has the disadvantage of requiring data transfer between the controller IC and the source driver IC at the high-bandwidth display refresh rate.

Figure 2 shows an improved architecture that contains just two ICs. The timing controller, source drivers and the framestore are integrated into one of these chips, while the gate drivers, a common electrode driver (V_{COM}) and the DC-DC conversion circuitry are integrated into the second chip.

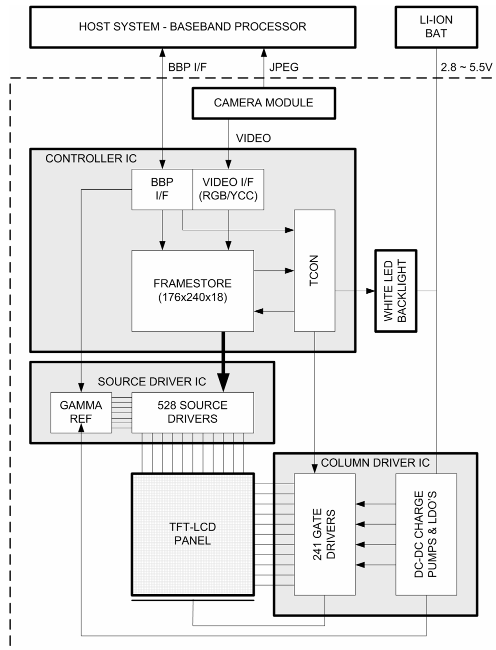

Figure 1: Three-Chip System

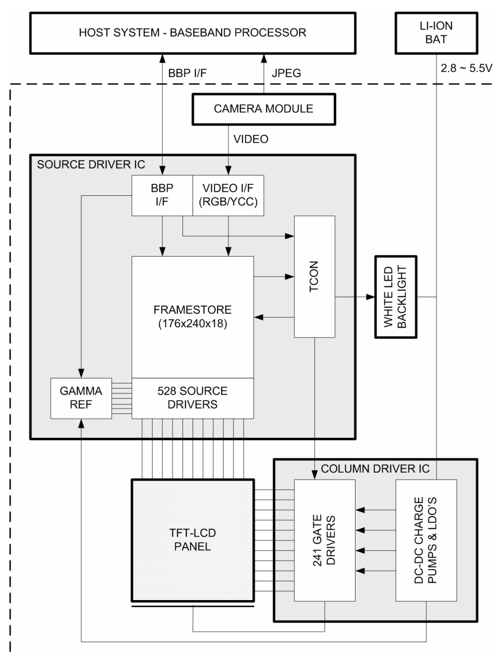

Figure 2: Two-Chip System

2.1 Chipset

The chipset shown in Figure 2 has been developed for 18-bit color 176x240 TFT-LCD display systems. This chipset may be used for lower resolutions such as 176x220. One chip contains the DC-DC converters required to produce all of the system's required DC voltages directly from a single-cell Li-ion battery. It also contains all of the gate drivers and associated logic, and a driver for the LCD panel's common electrode. The second chip contains a timing controller, 528 source drivers (6-bits each, for 18-bit color), a programmable gamma reference voltage generator, and a 176x240x18-bit framestore. This chip directly interfaces to the host system via an 8/16 bit parallel interface or via an SPI interface. It also contains a video interface for either 18-bit RGB or 8/16 bit YCC 4:2:2 data. [1] The second chip was implemented on a 0.35um CMOS process, with a die size of 1.98mm x 24.96mm.

3. Advantages of Integrated Framestore

3.1 Interface Power Reduction

To avoid flickering in the display, display refresh rates of 60-100 frames/sec. are required. If the display module does not include a framestore, significant interface power and processing bandwidth will be required from the baseband or application processor, even when the display data is static or slowly changing. This is so because the baseband or application processor must continuously generate and send data to the display module at the frame refresh rate. A typical 60Hz display (176x220x18-bit) requires a data rate of 2.32 Mword/s over an 18-bit interface. Assuming that half of the data lines are toggling (on average), an interface voltage level of 2.5V, and an interface capacitance of 20pf, the average power ($CV^2F/2$) required by the interface is:

$$20\text{pf} \times (2.5\text{V})^2 \times (2.32\text{MHz} \div 2) \times 18 \times 50\% = 1.31\text{mW} \quad (1)$$

This power consumption may not be obvious to the display module designer because it is provided by the baseband or application processor rather than by the display module.

If a framestore is included in the display module as in Figure 1, the baseband processor no longer must transfer data at the display refresh rate. In standby mode (i.e. no active phone conversation), the image data is static or slowly changing, so that the average data rate over the baseband processor interface approaches zero. Thus, during standby mode the power consumption of this interface also approaches zero. Since standby mode can represent >95% of the handset operation, battery life will be significantly improved in handset applications.

Even if video data is being displayed, the power consumption of the baseband processor interface is still significantly reduced because the video frame rate is much less than the display refresh rate. For example, QCIF video (176×144×18-bit×15fps) has a bit-rate of 6.9Mbit/s. This requires an average interface power of:

$$20\text{pf} \times (2.5\text{V})^2 \times 6.9\text{Mb/s} \div 2 \times 50\% = 0.22\text{mW} \quad (2)$$

This is a savings in power consumption of 1.09mW. Even if the logic voltage levels are reduced to 1.8V, this power savings is 0.57mW, which is still significant.

Furthermore, if the Display Controller, framestore and source drivers are integrated into one IC as in Figure 2, the power consumption of the interface between the source drivers and the framestore will be reduced because this interface is internal to the IC. This is in addition to the reduced power consumption of the baseband processor interface.

3.2 Memory Architecture Requirements

The required memory cycle time of an embedded framestore is modest, because the framestore can be easily designed to read an entire line of data in one operation. A 176x220 display operating at a 60Hz frame rate requires 220x60 = 13,200 line reads/sec. To burst-write a QCIF frame (176x144) into the framestore within 15msec, 176x144/0.015 = 1,689,600 pixel writes/sec are required. Assuming that negligible bandwidth is required to update the graphics portion of each frame, a typical framestore thus requires a peak bandwidth of:

$$0.0132\text{M} + 1.6896\text{M} = 1.703\text{M operations/sec.} \quad (3)$$

This is easily achieved with any of the CMOS processes that are used for the fabrication of the source driver circuits. This modest speed requirement allows "simultaneous" loading of both graphics and video data into the framestore through small internal FIFOs.

The die size and cost of such a framestore can be competitive with those of an external framestore if the source driver is implemented with a fine-line geometry CMOS process that includes a dual gate oxide (DGO) option. A DGO process provides small geometries for the fabrication of the framestore, while also providing the higher voltage transistors that are required by the source drivers. Alternatively, a non-DGO process could be used by employing National Semiconductor's voltage doubling techniques for the source drive circuitry.

3.3 Video Architecture Optimization

When a framestore is integrated with the source drivers, video may pass directly into the framestore because the framestore decouples the video rate from the display refresh rate. Most CMOS imager camera modules used in handsets can provide cropped and/or sub-sampled streaming video, in either RGB or YCC 4:2:2 formats. Such camera modules may be directly connected to the input of the framestore. Thus, live video data never needs to be sent through the handset processor in order to display it. This greatly reduces the interface requirements between the camera module and the handset processor.

As video data is sent to the framestore, a small amount of logic easily converts YCC data back into 24-bit RGB data. Both spatial and temporal dithering may be easily included as part of this logic in order to convert this 24-bit RGB data into the bit-depth supported by the source drivers and the LCD panel.

3.4 Additional Techniques for Power Reduction

When active, the backlight is by far the largest consumer of power in a display system. A typical backlight contains 4 white LEDS, each with a forward voltage of 3.3V and a forward current of 10mA. Assuming an LED driver efficiency of 80%, the backlight consumes 165mW when operating at full brightness. By integrating the framestore with the source drivers, it becomes practical to continuously collect statistics directly from the framestore as the display is refreshed. These statistics may then be used to automatically control the backlight power, via a PWM output from the source driver chip.[2]

To simplify the source driver circuitry, TFT-LCD panels are usually driven using a "line-inversion" scheme[3], wherein the common electrode of the TFT-LCD panel is driven with a square wave at half the line rate. Most of the AC power dissipation in a TFT-LCD panel is due to the line-inversion rate charging and discharging of the source to gate line capacitances and of the source to common electrode capacitances.

When a framestore is integrated with the source drivers, it becomes easy to modify the inversion scheme, display bit-depth, and display refresh rate according to the required performance for different operating modes. For example, when a handset is in standby mode, it may only be necessary to use partial display at a reduced bit-depth (which reduces the source driver power), and to use frame-inversion rather than line-inversion. The AC power dissipation of a TFT-LCD panel may be easily reduced by a factor of twenty or more (to as little as 0.12mW) under such conditions. This is a very substantial savings because a handset is typically in standby mode over 95% of the time.

4. Power Estimation

A detailed spreadsheet has been developed for use in accurately estimating the system power consumption of this chipset. First, the gross power consumption is calculated as the sum of several components:

- The AC power ($CV^2F/2$) dissipated by the charging and discharging of the various LCD panel capacitances. This power is a function of the panel capacitances, the V_{COM} modulation amplitude, the LCD voltage range, the source driver supply voltage, the line inversion rate, the gate voltage amplitude, and the line refresh rate.
- The power dissipated by the toggling of logic nodes within the column driver IC.
- The power consumption of the analog circuitry (clock generation, bias generation, and gamma DAC buffers) in the column driver IC.
- The power consumption of the framestore memory in the column driver IC.
- The power consumption of the gate driver IC.

The total power consumption from the battery is then calculated by dividing the gross power consumption by the efficiency of the DC-DC charge-pump converters. This efficiency is a function of the battery voltage and the required DC voltages.

Using this chipset, for a typical 176x220 LCD panel the calculated total power consumption from the system battery is under 5mW when displaying an all-white image in 18-bit mode. This includes the efficiency losses incurred during DC-DC conversion. By decreasing the bit-depth to 12 bits, this power will be reduced to under 4mW.

5. Conclusions

Significant advantages are obtained by integrating a framestore into the column driver chip of a small-format AMLCD display system:

The bit-depth of the displayed data may be reduced without changing the stored image data, in order to reduce power consumption. The use of an integrated framestore also enables the use of other inversion schemes, which can drastically reduce the AC power dissipated by the LCD panel.

The integration of the framestore with the source drivers also facilitates the implementation of an automatic backlight intensity control that is based on the statistics of the displayed image.

6. References

[1] ITU Recommendation ITU-R BT.601

[2] Insun Hwang, SID 01 Digest, pp. 492-493 (2001)

[3] Christopher Ludden, "How to Design Module Electronics for Advanced TFT-LCDs," SID Seminar, June 1994.