

Image Processing Applied to Small Format Displays



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P-43: Image Processing Applied to Small Format Displays

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Abstract

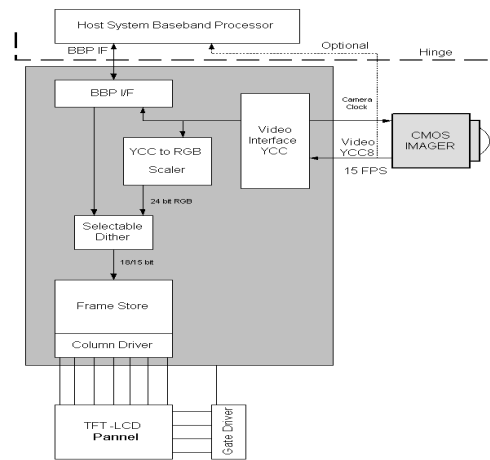
The application of TFT displays for handset applications requires new display system architectures to have on-chip image processing in order to accommodate a direct camera connection. Other image processing techniques like stochastic dithering are required to reduce the size of the on-chip frame buffer thus reducing power and silicon real estate utilization, while preserving high image quality. The purpose of this paper is to explore the applicability of certain key image processing techniques, which add value to display column drivers with respect to their typical usage. The benefits and caveats of these image processing methods with respect to power and system bandwidth are articulated and their hardware requirements are discussed.

1. Objective and Background

The handset market has recently seen the emergence of cell phones equipped with image sensors or cameras. To capture video from these CMOS imagers a video port with a YCC/RGB interface is available on Small Format Column drivers [1]. However, the small format column drivers are meant for QCIF, QCIF+ and QVGA TFT displays and hence video coming from Megapixel Imager needs to be resampled. This process of resampling is called Image Scaling. The incorporation of an Image Scaler on a column driver with a video port enables a direct camera connection, eliminating the need for an interface chip between the Imager and the column driver. This value added column driver is now in line with market trend while greatly reducing the cost of the camera interface circuitry. The direct connection between a column driver and a camera is shown in Figure 1. The paper discusses different image scaling techniques in terms of the hardware requirements, feasibility of integration with a column driver and the impact this integration has on system bandwidth, power and image quality.

The on-chip frame buffer on the column driver consumes most of silicon real estate for a column driver. The recent market trend is moving towards smaller pixel pitch for TFT displays which constrains the length of the silicon area for driver chips. Hence, it is imperative to develop a scheme to reduce the size of the column driver chips. Reducing the size of the on-chip frame buffer results in a silicon area savings for the column driver. One way of

achieving a smaller frame-buffer is to reduce the memory word-width or the pixel resolution in bits while still maintaining a high image quality. Using multitone to shape the quantization noise generated due to the reduction in pixel resolution preserves image quality. Thus, the use of multitone enables the reduction of the frame-buffer and consequently of the column driver without compromising the image quality. Different multitone strategies will be discussed in this paper with emphasis on hardware requirements, feasibility of integration as well as the impact on power, silicon real estate consumption and image quality.



2. Results

The pros and cons of three popular Image Resampling strategies as well as their applicability to small format column drivers is summarized in Table 1 below. Silicon Area Estimates are obtained in terms of gate counts by using synthesis tools like Synopsys. MATLAB routines were developed to capture the different scaling strategies. These MATLAB routines were used for qualitative evaluation of different image scaling strategies. The output scaled images obtained as a result of executing these routines were visually inspected for quality determination.

Scaling Strategy	Image Quality	Hardware Requirements and Approximate Gate Count	Bandwidth Impact	Power Impact
Nearest Neighbor	<ul style="list-style-type: none"> • Significant amount of aliasing manifesting itself as jaggedness in the output image. [1] • Ringing artifacts due to Gibbs phenomenon. 	<ul style="list-style-type: none"> • Counters/Adders for Interpolation Grid Generation. • Approximately 1100 gates needed. Integration with a column driver is feasible on a 500 nm process. Deep sub-micron process not needed. • Due to hardware simplicity, a good strategy for small format drivers like SQCIF, QCIF and QCIF+ where the prospect of a direct camera connection outweighs image quality concerns. 	Depends on the pixel resolution of the image sensor. To avoid jaggedness the scaler and the video datapath should be able to accept video at 15 fps. For a Megapixel(1280x 1024) sensor with YCC8 output this translates to bandwidth requirement of about 40 MHz.	Direct camera connection only used in the viewfinder mode, which is a low percentage usage condition. Hence, with an operating speed of 40 Mhz the overall battery consumption is low due to low usage.
Bilinear Interpolation (Seperable 2-Point Interpolation)	<ul style="list-style-type: none"> • Better than nearest neighbor in terms of aliasing. Although, aliasing artifacts are still present. [1] • Significant amount of passband attenuation leads to blurring artifacts. [1] 	<ul style="list-style-type: none"> • Two 2-Tap FIR filters one for the Column and one for the Row dimension. Convolution operation requires 2 multipliers and one adder per color channel. Two image lines need to be stored for column dimension convolution. • Integration with column driver only possible on a deep sub-micron process (< 0.25 um) for efficient silicon real estate utilization. • Due to some hardware complexity, this strategy is applicable for medium quality QCIF+ and QVGA small format column drivers. 	Depends on the pixel resolution of the image sensor. To avoid jaggedness the scaler and the video datapath should be able to accept video at 15 fps. For a Megapixel(1280x 1024) sensor with YCC8 output this translates to bandwidth requirement of about 40 MHz. Due to the arithmetic operations and memory read and writes required multi-stage pipelined datapath is required to get the required throughput of 15fps.	Direct camera connection only used in the viewfinder mode, which is a low percentage usage condition. Hence, with an operating speed of 40 Mhz the overall battery consumption is low due to low usage.

<p>Bicubic Interpolation (Seperable 4 Point Interpolation)</p>	<ul style="list-style-type: none"> • By choosing a suitable cubic interpolation polynomial for FIR filter coefficient generation artifacts due to aliasing and unnecessary blurring can be prevented [1]. High quality scaled images can be obtained with this method 	<ul style="list-style-type: none"> • Two 4-Tap FIR filters required, one for row and one for column dimension. Convolution operation requires 2 multipliers and one adder per color channel. Four image lines need to be stored for column dimension convolution. • Due to some hardware complexity, this strategy is applicable for High quality QCIF+ and QVGA small format column drivers. • Integration with column driver only feasible on a deep sub-micron process (< 0.18 um) for efficient silicon real estate utilization. 	<p>Depends on the pixel resolution of the image sensor. To avoid jaggedness the scaler and the video datapath should be able to accept video at 15 fps. For a Megapixel(1280x 1024) sensor with YCC8 output this translates to bandwidth requirement of about 40 MHz. Due to the arithmetic operations and memory read and writes required multi-stage pipelined datapath is required to get the required throughput of 15fps.</p>	<p>Direct camera connection only used in the viewfinder mode, which is a low percentage usage condition. Hence, with an operating speed of 40 Mhz the overall battery consumption is low due to low usage</p>
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Table 1

Certain key test images are used for testing and evaluating dithering techniques. Images with gradual and slow gradients suffer from contouring artifacts upon quantization and are ideal candidates for comparative assessment and evaluation of some dithering techniques.

The differentiating factor for these dithering techniques is the size of dither mask and the method used to generate the mask. Such images were used for qualitative evaluation of different dithering techniques and the results are tabulated below in Table 2.

Multitoning Strategy	Image Quality	Hardware Requirements	Power Impact	Silicon Real Estate Impact
<p>Ordered Dithering with a small 16x16 dither mask generated from noise shaping white noise</p>	<p>Depends on the size of the quantization step. For dithering images from 24-bits to 18-bits this table works well. However, for truncation beyond 18-bits the dithering results in granular noise being added to the image. The image also suffers from regular patterns, which are very noticeable to the eye.</p>	<p>Lookup Table for the dither mask and an adder for the dithering process</p>	<p>24-bit Quality is obtainable from an 18-bit Frame Buffer thus allowing almost 25 % reduction of memory silicon real estate. This amounts to a 25 % reduction in memory refresh power for a DRAM frame buffer</p>	<p>24-bit Quality is obtainable from an 18-bit Frame Buffer thus allowing almost 25 % reduction of memory silicon real estate.</p>

			architecture.	
Ordered Dithering with 256x256 dither mask with special high frequency characteristics	Image quality is reasonably good for dithering down to 15-bits from 24-bits. Using a bigger dither mask goes a long way in improving image quality and depending on the method used to generate the dither mask (refer [2]) high quality images can be obtained.	Lookup Table for the dither mask and an adder for the dithering process	24-bit Quality is obtainable from an 18-bit Frame Buffer thus allowing almost 38 % reduction of memory silicon real estate. This amounts to a 38 % reduction in memory refresh power for a DRAM frame buffer architecture.	24-bit Quality is obtainable from a 15-bit Frame Buffer thus allowing almost 38% reduction in memory silicon real estate. This allows for significant reduction in column driver chip length, which enables the column driver to support small TFT displays with a smaller pixel pitch.

Table 2

References

[1] Survey: Interpolation Methods in Medical Image Processing, Thomas M. Lehmann, Claudia Gonner, Klaus Spitzer, IEEE Transactions on Medical Imaging, Vol. 18, No. 11, November 1999

[2] Selected Papers on Digital Halftoning, Jan P. Allebach, SPIE Milestone Series, Volume MS 154

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