Package,Thermal,Characterization

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Introduction

Effective heat removal from the IC chip, through the package, to the adjacent environment is crucial to maintain an allowable device junction temperature. The latter directly affects the electrical circuit performance both at the component and system levels. Aside from thermal enhancement of individual packages by the IC manufacturers, proper printed circuit board (PCB) layout and cabinet design by the end users can also substantially reduce the overall package thermal resistance.

The fundamentals of various heat transfer modes can be found in any classic heat transfer textbook, and recent advances in heat transfer and fluid flow development can be referred from published technical papers. Thus, the intent of this application note is threefold:

1. provide practical aspects of package thermal resistance definition;
2. show how the data are generated; and,
3. discuss package mounting, board effect, and system effect on heat transfer.

This application note first covers the basics of package thermal characterization to help the end user in interpreting the package thermal data. Subsequently, the package mounting effects, board effects, and system effects on package heat transfer are outlined, along with some critical dimensions. The last section is a summary of major guidelines for the end user to obtain a better thermal design at the board and system levels.

Package Thermal Characterization

Thermal properties of electronic packages are characterized by θ_{JA} and θ_{JC}, which are widely used in the electronic industry. θ_{JA} can be defined as an overall package thermal resistance, which is the sum of package internal and external thermal resistance. It can be expressed as:

$$\theta_{JA} = \theta_{JC} + \theta_{CA} = (T_J - T_A)/P$$

where

θ_{JC}: $(T_J - T_C)/P$, junction-to-case conductive thermal resistance (˚C/W)

θ_{CA}: $(T_C - T_A)/P$, case-to-ambient convective thermal resistance (˚C/W)

P: I (Current) x V (voltage), Device heat dissipation (W)

T_J: Average device junction temperature (˚C)

T_A: Average ambient temperature (˚C)

T_C: Case temperature at a prescribed package surface (˚C).

θ_{JC} is dominated by the conductive thermal resistance within layers of packaging materials, and is highly dependent on the package configuration. If the heat flow is assumed to be perpendicular to each layer of the packaging material, θ_{JC} may be expressed as

$$\Sigma\ t_i/(k_i\ A_i)$$

where t, k, and A are the thickness, thermal conductivity, and heat transfer surface area of each packaging material layer, e.g., die attach material, lead frame, die coating, and encapsulant.

θ_{CA} is the external convective thermal resistance. It is greatly affected by adjacent ambient conditions, package boundary conditions, and conjugate heat transfer.

Figures 1, 2, 3 and *Figure 4* describe the package thermal experiments, TSP (Temperature Sensitive Parameter) diode calibration procedure, θ_{JC} and θ_{JA} deriving methods, as summarized by (1). Typically, T_A and T_C are physically measured by high precision thermocouple wires. T_J is an indirect measurement extracted from the TSP diode calibration curve. The average device power is calculated by the product of measured current flow and voltage across the power and ground pins of a given package. All measured values are recorded at the thermal equilibrium state of room temperature and 1 atm. conditions. Details on the measurements procedures can be found elsewhere (2), together with data generated with a thermal test chip (3).

Package Thermal Characterization (Continued)

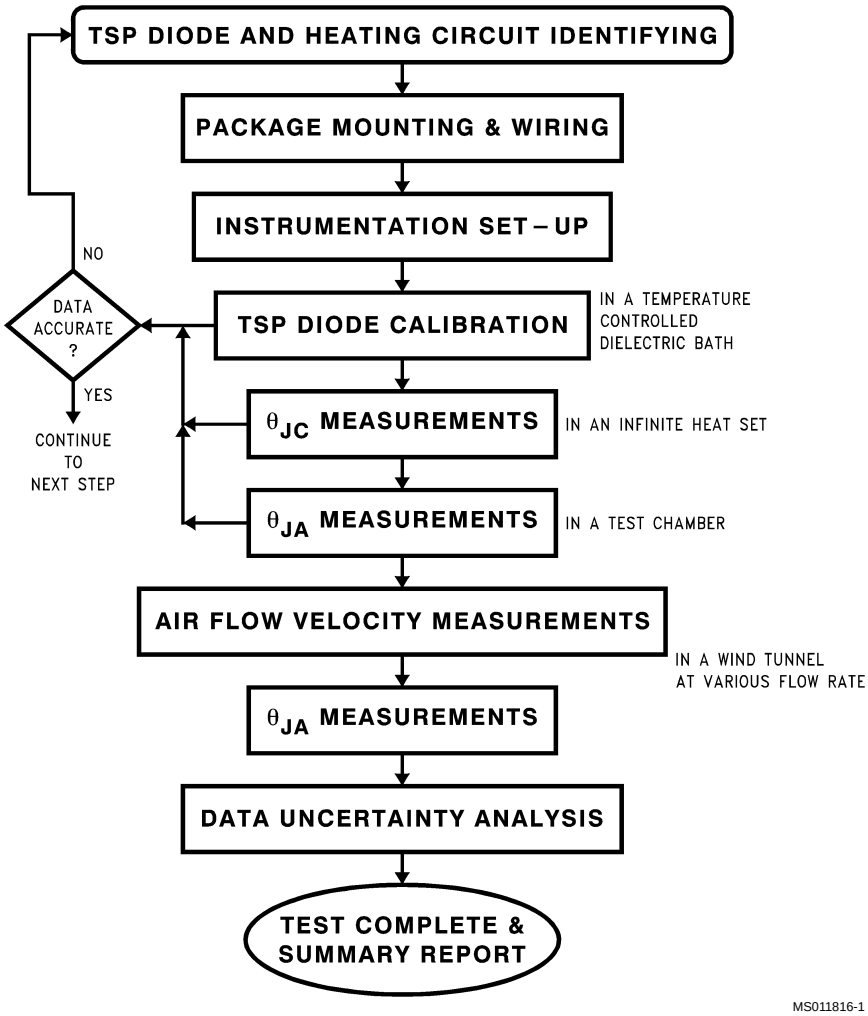

FIGURE 1. Package Thermal Experiments

Package Thermal Characterization (Continued)

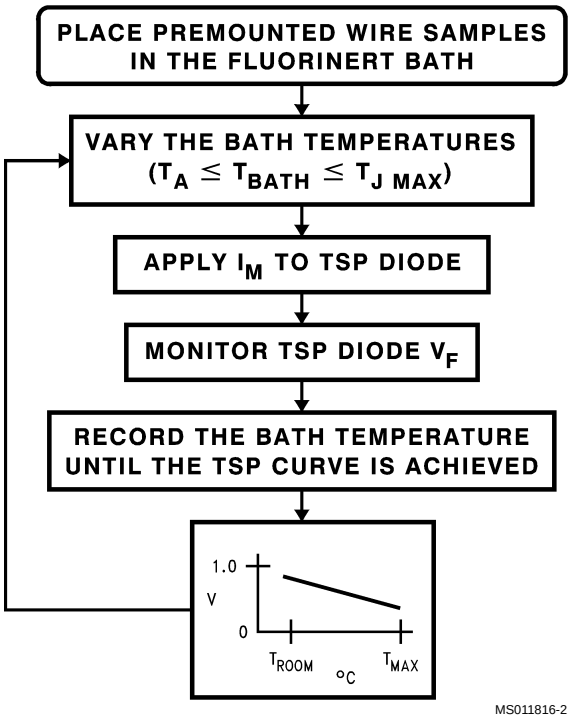

FIGURE 2. TSP Diode Calibration

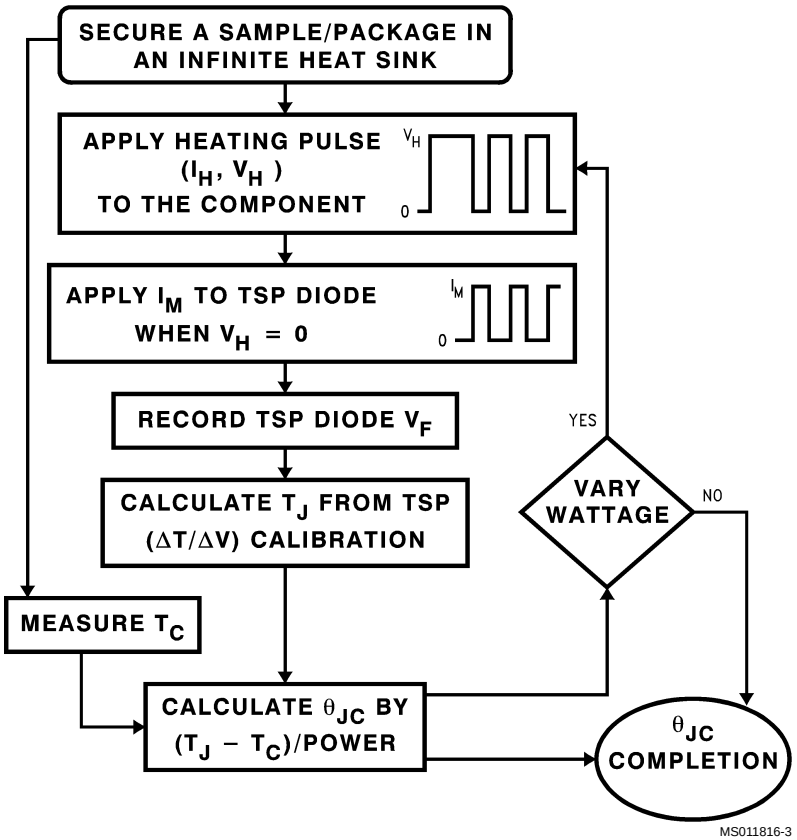

FIGURE 3. θ_{JC} Deriving Methods

Package Thermal Characterization (Continued)

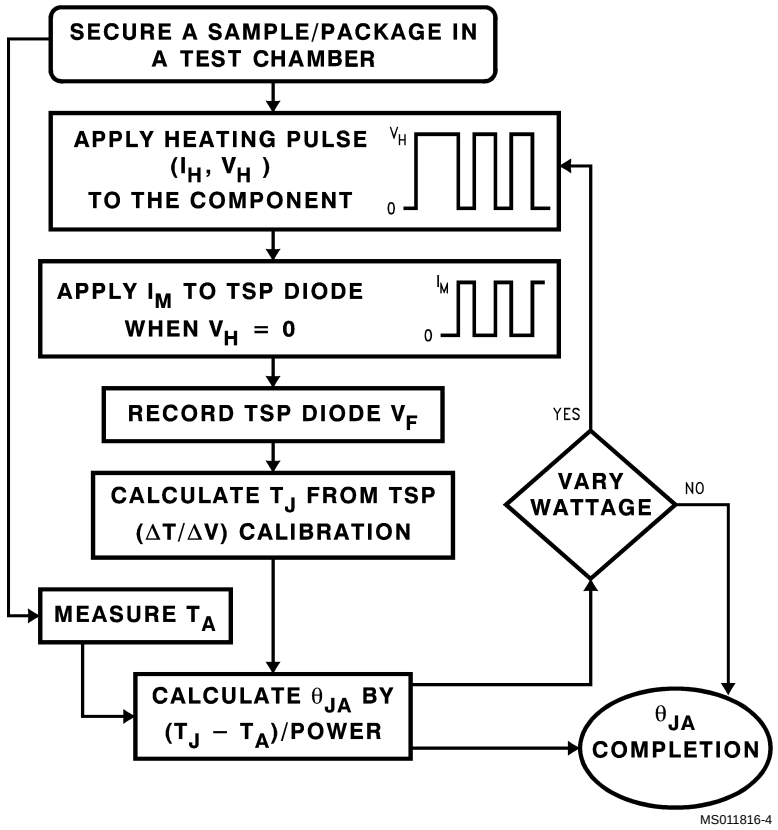

FIGURE 4. θ_{JA} Deriving Method

Tabular thermal data in this databook list the typical package thermal resistance data from each package family with different lead counts. θ_{JA} data are generated with packages mounted on National Semiconductor's standard FR-4 test boards, which conform to SEMI/JEDEC standards and are designed for certain package families. Typically, the overall thermal resistance decreases with an increase of the forced flow rate, when the flow becomes fully developed and the temperature profile does not fluctuate. At this stage, even with further increases in flow rate, the overall package thermal resistance stays relatively unaffected. As the die size increases for a given package, the overall package thermal resistance decreases due to a reduction in power density.

Thermal testing of the end user's board or system product may be made by a regional NSC Sales representative when your thermal loading condition is largely different from NSC standard test conditions. If the user has stringent thermal requirements for critical applications, the package thermal resistance can be reduced further with embedded heat spreaders or particular lead frame designs.

Package Mounting (Through Hole vs Surface Mount)

Package pin-to-board solder joints should be free of voids to minimize unwanted thermal resistances. Depending on the package style, there is an inherent thermal limitation on each package family. For instance, DIPs mounted on a PC board typically have a wider gap from board-to-package bottom than SOs. This differential results in a poor package thermal performance. Nevertheless, improvement can be obtained by providing an additional heat path to the board such as installing a metal rail underneath the package, or increasing the metal trace footprint area to enhance heat conduction from the ground pins. Care must be taken when an external fin or heat sink is mounted on a package, since drag may be generated in the flow field depending on the position of the package on the board.

Board Effect

A printed circuit board acts as a heat sink providing path(s) for individual packages to effectively transfer heat to the board and the adjacent environment. Thus, maximizing the area of the metal trace where the power and ground pin(s) of the package are located is important for effective heat transfer as pointed out by (4).

To enhance the "chimney effect", the pressure drop between the flow inlet and outlet, or across the entire flow field, should be maximized. This is achieved by reducing the friction in the flow with the proper layout of packages of different heights. Furthermore, high power devices may be placed near the leading edge or trailing edge of the board, so that a potential thermal runaway is no longer a concern.

The board should be attached closer to the cold plate wherever possible. The board should never be placed with the mounted packages facing down in the same direction as the gravitational force, so that convective currents can be available. If the board is facing up, the higher power devices may be positioned in the board center, in case all the locations along the board edges are occupied. As a rule of thumb, packages at the upper levels are always preheated by packages at the lower positions. This preheating effect has to be considered in any board level thermal analysis.

System Effect

Cabinet height-to-width/depth aspect ratio and board-to-board spacing, and adjacent package spacing can have significant effects on the overall system thermal performance. In addition to the ergonomics, the typical cabinet aspect ratio is close to 1. Certain large protruding packages from the board may induce drag in the flow, where the desired channel or cabinet pressure drop can be altered. When radiant heat transfer is no longer negligible, a polished aluminum cabinet interior close to mirror image may promote the system heat transfer. Thus, a basic understanding of natural, forced, and mixed convection, and combined conduction, convection, and radiation, and fluid flow would be useful for the facilitation of overall thermal design. Regular cleaning of the precipitated dust and contaminant on the package and board surfaces can maintain thermal stability of the system.

Summary

A thermal resistance approach by electrical analogy, so far, is the simplest method for analyzing the thermal behavior from the component level up to the system level. The following practical thermal guidelines may be useful in providing component and system reliability, which meet the best interests of both semiconductor manufacturers and end users:

1. Provide sufficient conduction paths from the package to the board or adapt a direct heat sink approach,
2. Enhance the convective heat transfer to the board or along the board in the cabinet by diverting flow to simulate jet impingement at the hot spot regions,
3. Place high power devices near the leading edge or trailing edge of the board when the board is oriented vertically. On the other hand, when the board is oriented horizontally, position the high power devices face up within the center,
4. Mounting of any heat sink on a package should also take into consideration the heat transfer effect on adjacent packages,
5. Strengthen the radiant heat with an increase of surface emissivity.

The overall thermal resistance of a package can be reduced significantly by addressing the comprehensive thermal management from the component level, to the board level, and up to the system level.

References

1. P. C. Lin, *"Thermal Characterization of Semiconductor Packages",* **Nordic Cooling of Electronics Conference,** Gothenberg, Sweden, November 18–19 (1992).
2. R. M. Mindock, *"Thermal Resistances of Joint Army Navy (JAN) Certified Microcircuit Packages",* **RADC-TR-86-97,** Rome Air Development Center, Air Force Systems Command, Griffiss AFB, NY (1986).
3. R. Pendse and B. J. Shanker, *"A Study of Thermal Performance of Packages Using A New Test Die",* **4th IEEE Semiconductor Thermal and Temperature Measurement Symp.,** pp. 50–54 (1988).
4. C. Simpson, *"The Fundamental of Thermal Design",* **Electronic Design,** pp. 95–100, September 26 (1991).

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