

Maximizing the Performance of GaN with Ideal Diode Mode



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ABSTRACT

Gallium Nitride (GaN) High Electron Mobility Transistor (HEMT) has significant advantages over traditional Si MOSFETs due to its lower gate charge and smaller output capacitance which lead to faster switching and lower losses. Also, the absence of body diode in GaN allows zero reverse recovery thus making it viable in high-frequency power converters. However, the reverse conduction voltage of GaN is high compared to Si MOSFET's body diode leading to slightly higher dead time losses due to the third quadrant freewheeling current. Targeting to reduce the third quadrant dead time losses, an ideal diode mode function is implemented in TI's new generation GaN devices. The ideal diode mode enables an adaptive dead time, and automatically realizes a fast synchronous FET operation with no external circuitry or control. Detailed explanation of the ideal diode mode feature and its benefits with experimental results will be presented in this application note.

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1 Introduction

1.1 GaN Application Background

GaN is an enabling technology for high-efficiency and high-power-density power converter designs. Owing to its superior material property, the junction capacitance of the lateral GaN device is much lower compared to vertical Si power MOSFETs, thus making GaN suitable for high-frequency operations. Meanwhile, utilizing the piezoelectric property, a two dimensional electron gas (2DEG) layer with high electron mobility is formed in between the aluminum gallium nitride (AlGaN) and GaN heterostructure interface. Hence, a low on-resistance is achieved. In addition, unlike the Si MOSFETs with p-n junction body diode, no body-diode exists in lateral GaN devices and consequently there is no reverse recovery loss associated with GaN device. Combining all the material property and structural benefits, GaN devices demonstrate a better figure of merit (i.e. lower specific on-resistance), and they have been applied to various hard-switching and soft-switching converters. For example, with insignificant hard-switching losses in GaN devices, the continuous conduction mode (CCM) totem-pole power factor correction (PFC) is enabled in the AC/DC stage leading to high-power density see [TIDM-1007](#). Also, owing to its low turn-off loss, the GaN devices are desirable for high-frequency soft-switching topologies like LLC and phase-shifted full-bridge (PSFB) converters in the DC/DC stage see [TIDA-010062](#) and [PMP20637](#).

Still, the reverse conduction voltage of traditional GaN devices is high and induces excessive reverse conduction losses during the dead time. To further improve the system's efficiency, this application note introduces the ideal diode mode in TI's new generation GaN devices targeting at reducing the dead time losses in GaN devices.

1.2 Dead Time Losses

Soft-switching and hard-switching topologies will have different dead time mechanisms, and they will be analyzed separately taking the Si MOSFET as example. For hard-switching topology, a buck converter is shown as an example. There are two instances of dead time during each switching cycle. [Figure 1-1](#) demonstrates the first instance of the dead time, where both FETs are off followed by the turn-on of the lower FET as demonstrated in [Figure 1-2](#). In [Figure 1-1](#), when both FETs are off, the inductor current will go through the body diode of the Si MOSFET, and there will be power loss due to the diode conduction. One point to note is that it takes some time for the inductor current to discharge the lower FET output capacitance for the body diode to conduct, and this time t_f needs to be subtracted from the dead time. Also the value of t_f will be dependent on the load current I_L . The loss in the lower FET due to the first dead time can be estimated in [Equation 1](#):

$$P_{dt1, Si} = V_{sd} \cdot I_L \cdot (t_{d1} - t_f) \cdot f_{sw} \quad (1)$$

- V_{sd} is the body diode forward voltage drop
- I_L is the inductor current during the dead time
- t_f is the rising time for upper FET's V_{ds}
- t_{d1} is the first dead time
- f_{sw} is the switching frequency

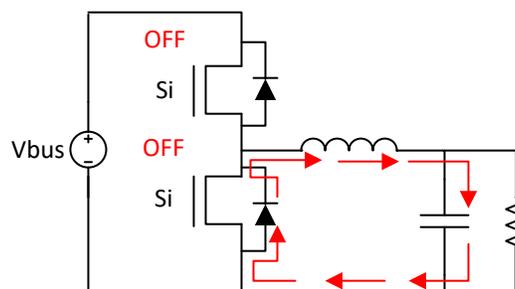


Figure 1-1. Inductor Current Path During Dead Time After High Side Turns Off In Buck Converter

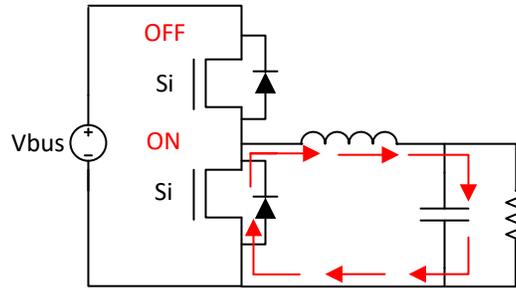


Figure 1-2. Inductor Current Path After Low Side MOSFET Turns On In Buck Converter

The second dead time as illustrated in [Figure 1-3](#) is followed by the turn on of the upper FET as shown in [Figure 1-4](#). The second dead time will start as soon as the lower switch turns off, and end when the upper switch turns on. The dead time loss in this period can be estimated in [Equation 2](#) :

$$P_{dt2, Si} = V_{sd} \cdot I_L \cdot t_{d2} \cdot f_{sw} \quad (2)$$

where

- t_{d2} is the second dead time

For other examples, such as the LLC converter or the synchronous buck converter operating under light load condition where the current reverses direction by the end of switching cycle, this term will be eliminated because there is no reverse current conduction in those cases.

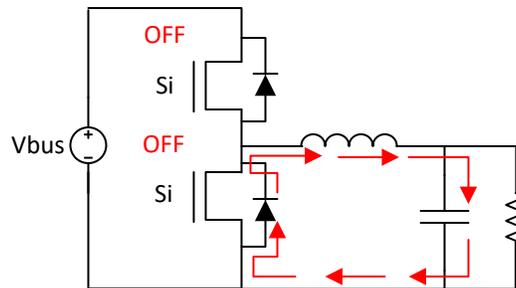


Figure 1-3. Inductor Current Path During Dead Time After Low Side Turns Off In Buck Converter

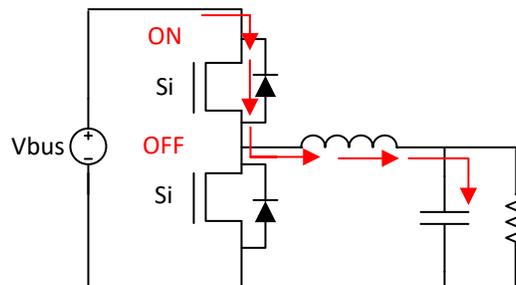


Figure 1-4. Inductor Current Path After High Side MOSFET Turns On In Buck Converter

The sum of the two dead time losses is the total loss due to the dead time in buck converter and it can be estimated according to (3) for Si MOSFET. In most cases though, the diode reverse recovery loss will be dominating the losses of Si MOSFETs. Please note that the analysis of reverse recovery losses are not part of this application note and those losses are not shown in equation [Equation 3](#).

$$P_{dt,Si,buck} = V_{sd} \cdot I_L \cdot (t_{d1} - t_f) \cdot f_{sw} + V_{sd} \cdot I_L \cdot t_{d2} \cdot f_{sw} \quad (3)$$

1.3 Third Quadrant Operation in GaN

As can be seen from the above discussion, the dead time loss is related to the reverse conduction voltage of the device. For Si MOSFETs, this voltage is determined by its body-diode's characteristics. For GaN HEMT, the reverse conduction voltage depends on the third quadrant characteristic. [Figure 1-5](#) shows the lateral GaN structure: the Source and Drain are connected to the conducting two-dimensional electron gas (2DEG) channel and the gate voltage controls the conductivity of the channel, see [SNOAA36](#).

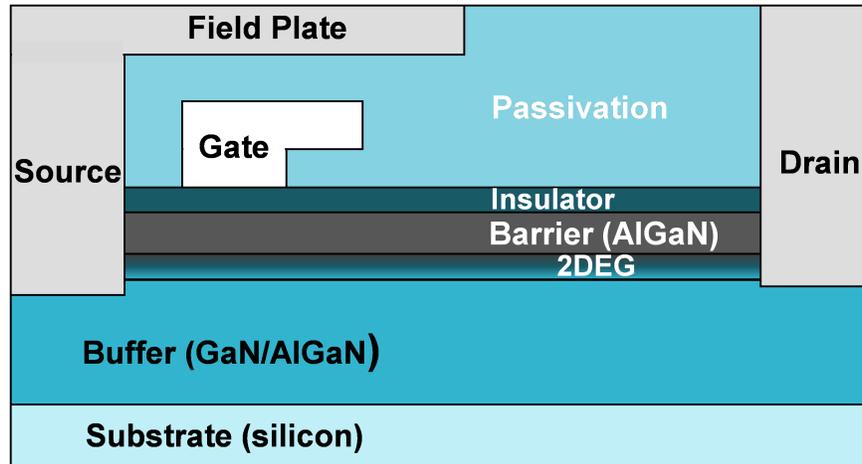


Figure 1-5. Cross Section Of The Lateral Structure Of GaN FETs

In third quadrant conduction, the Drain potential is lower than the Gate. When the gate-to-drain voltage is larger than the threshold voltage as indicated in [Figure 1-6](#), the channel region is on thus allowing a reverse conduction.

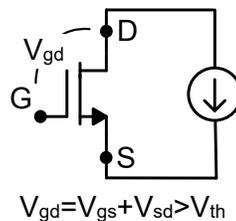


Figure 1-6. Conditions To Turn On The Channel In The Forward And Reverse Conduction

Like a diode, the reverse voltage V_{sd} is self-biased such that V_{gd} can reach V_{th} and the channel in GaN HEMT is self-commutated to conduct the reverse current. Under third quadrant operation, the reverse conduction voltage V_{sd} is composed of the bias voltage $V_{th} - V_{gs}$ and the resistive part as indicated in [Equation 4](#). The equivalent on-resistance in third quadrant $R_{on_Reverse}$ is a function of junction temperature.

$$V_{sd} = (V_{th} - V_{gs}) + I_L \cdot R_{on_Reverse} \quad (4)$$

Based on [Equation 4](#), the third quadrant characteristic of GaN HEMT is derived and plotted in [Figure 1-7](#). Compared with Si MOSFET's body diode, GaN HEMTs have higher V_{sd} drop as $V_{th} - V_{gs}$ is usually higher than 0.7 V when the gate is off. For instance, the commercial 650 V enhancement-mode GaN device has a typical threshold voltage of 1.7 V, which is higher than the intrinsic voltage drop of the silicon body diode. For some high-power applications, a negative off-state gate voltage is normally applied to mitigate the cross-talk's impact. As a result, the reverse voltage drop starts with 4.7 V considering a negative gate bias of -3 V, and increases

further as the load current increases. Similarly, a high reverse conduction voltage is observed for the depletion-mode GaN devices. Depending on the applied gate-to-source voltage during off-state, the reverse voltage drop is in the range of 5 -7 V. As can be seen, the high reverse conduction voltage can cause excessive dead time losses if the dead time is long, and it brings concerns on the system efficiency and device's thermal limitation.

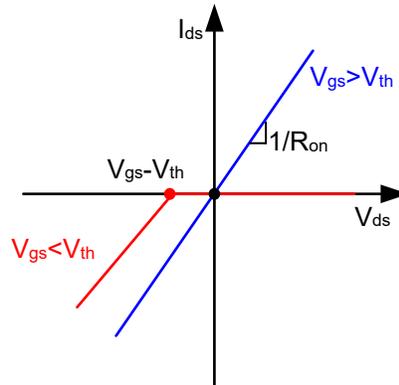


Figure 1-7. Simplified Behavior Of GaN in 1st and 3rd Quadrant

2 Ideal Diode Mode (IDM) in TI GaN

2.1 Function and Operation of Ideal Diode Mode

As previously mentioned, GaN will conduct current in third quadrant when gate is off with a high reverse voltage drop. If the dead time is prolonged, the power loss from the third quadrant conduction will be high, and results in lower efficiency and thermal performance. A popular method to shorten the dead time is adaptive dead time control. As discussed in [5], the minimum required dead time varies, and an optimum dead time can be selected based on device characterization at different operating conditions. However, this method requires intensive testing of the device and cannot deal with the part variations easily. On the other hand, the adaptive dead time scheme is proposed with the assist of different circuit implementations [6, 7, 8 and 9], and it is helpful to improve the system efficiency. However, the implementations in [6 and 7] require fast comparator to detect the switch node voltage, along with delay generation circuit. Additionally, it requires a tuning process to find the optimal dead time as the load changes, and a shoot-through can happen during the tuning process, which causes device reliability issues. For the counter based method in [8 and 9], an iteration process is needed to find the dead time, which takes time to execute thus ending up with a long delay time. While the abovementioned methods have shortcomings such as shoot-through and long delays, the ideal diode mode is a built-in feature of TI GaN that can optimize the dead time and improve the overall system performance with no external circuitry required.

The ideal diode mode allows GaN FET to be turned on automatically by the built in gate driver after a very short delay t_{3rd_Det} when a negative drain to source voltage is sensed. As the gate is turned on, the device is no longer off and the voltage drop will be depending on the on state resistance, which greatly reduces the amount of loss during dead time. It is important to note, that the TI GaN devices need to be switched in every switching cycle for the device to enter the ideal diode mode on a cycle by cycle basis.

A working example of the ideal diode mode is shown in Figure 2-1 and Figure 2-2 taking a boost converter as an example. Figure 2-1 shows the circuit diagram, and Figure 2-2 shows the timing diagram for the PWM input signal, real gate signal, as well as the switch node waveforms. Firstly, as the low-side device turns off, the inductor current starts to charge the switch node capacitances as shown between T1 and T2. When the switch node slightly exceeds the output voltage, the high side switch enters third quadrant operation as pointed at time T2, which will cause the third quadrant voltage drop. Next, the negative source to drain voltage will be detected by the internal circuitry, and after a short detection time t_{3rd_Det} , the high side GaN switch will be turned on automatically despite low IN signal as shown at T3. As soon as the GaN device is on, the TI GaN will no longer exhibit large, third quadrant voltage drop. Accordingly, between T3 and T4 the V_{sd} voltage drop will be the product on the R_{dson} and the inductor current. T4 shows when high side IN signal is received while the switch is in ideal diode mode, the FET will be kept on. The next event is that when the high side IN signal goes low, the FET will be turned off per IN pin signal as shown at T5. After the turn off event is initiated by the IN signal and the GaN device turns off, re-triggering of the IDM mode will be prevented for the duration of a blanking time t_{3rd_Blank} specified in the datasheet of the TI GaN devices.

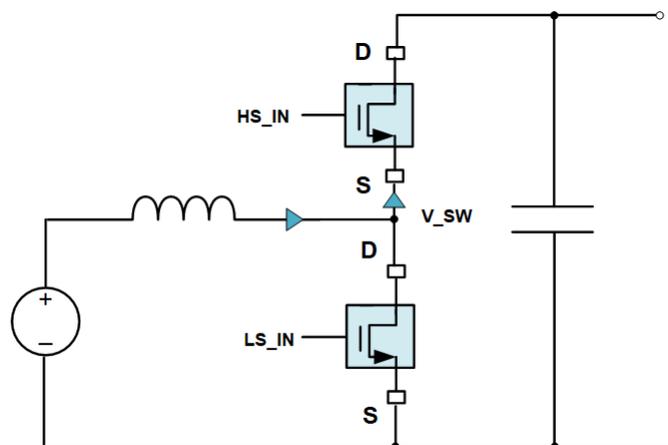


Figure 2-1. Boost Converter Diagram

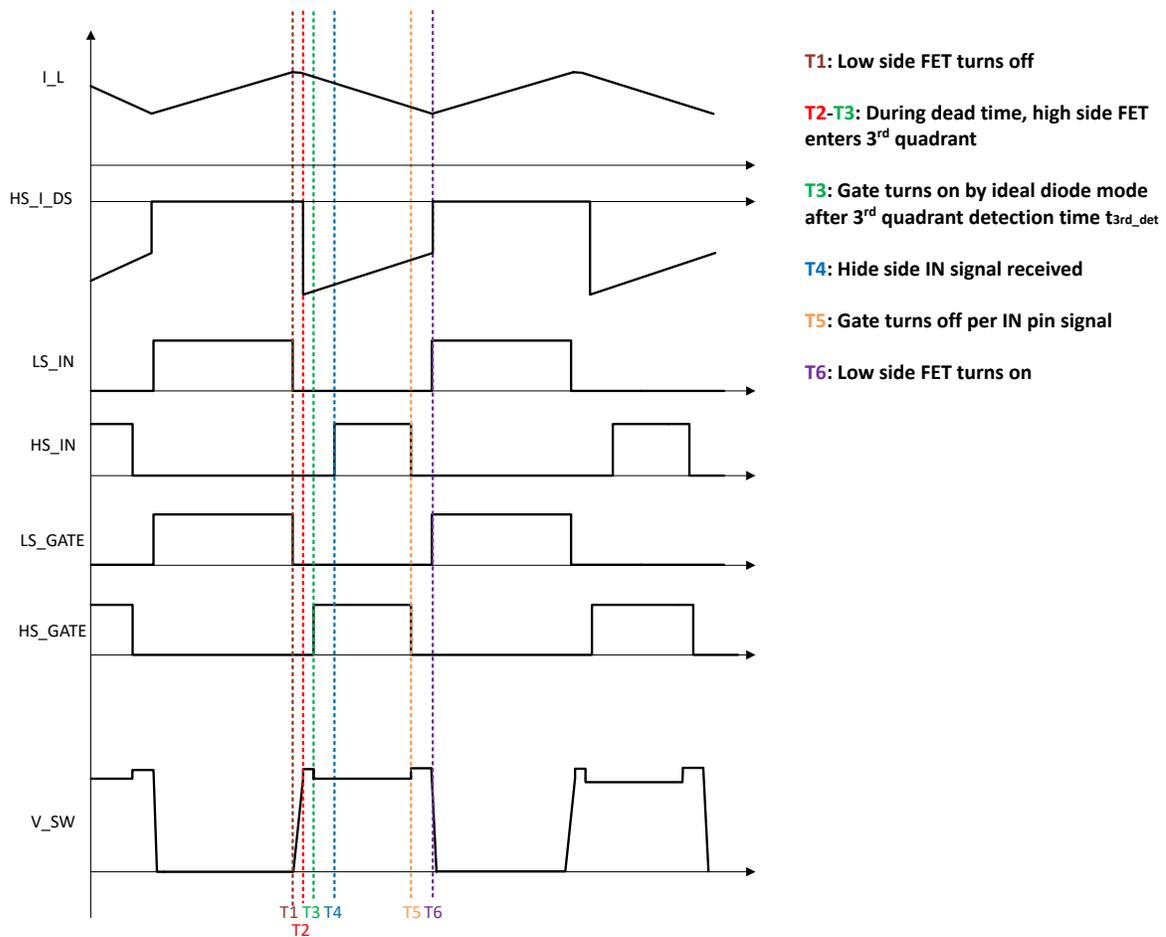


Figure 2-2. Figure 11. Operation Steps Of Ideal Diode Mode Feature

The dead time loss with ideal diode mode GaN for hard-switching application can be estimated as shown in Equation 5 :

$$P_{dt,IDM,boost} = V_{sd} \cdot I_L \cdot t_{3rd_Det} \cdot f_{sw} + R_{dson} \cdot I_L^2 \cdot (t_{d1} - t_r - t_{3rd_Det}) \cdot f_{sw} + V_{sd} \cdot I_L \cdot t_{d2} \cdot f_{sw} \quad (5)$$

in Equation 5 is a very small value, and the will be much less than the reverse conduction voltage . Hence, the dead time loss can be greatly reduced compared to the GaN FET without the ideal diode mode feature.

2.2 Comparison Between IDM GaN, SiC and Discrete GaN

Figure 2-3 shows a comparison between TI GaN with ideal diode mode, a 650V SiC MOSFET, discrete e-mode GaN FET and discrete d-mode GaN FET without the ideal diode mode feature at 10A current. The dead time here is the dead time after the active switch turns off and before the synchronous switch turns on. As the dead time after synchronous switch turns off is not load dependent and should be minimized, the dead time loss here only considers the loss described in equation (1). The dead time is fixed at 100ns, and the switching frequency is swept from 100 kHz to 500 kHz. The advantage of ideal diode mode becomes more significant when the switching frequency goes up. Figure 2-4 shows comparison of the same three devices with the switching frequency fixed at 200 kHz, and the dead time power loss of TI GaN with ideal diode mode remains very flat with increased dead time setting due to the fact that the voltage drop with ideal diode mode is much lower than the ones without ideal diode mode.

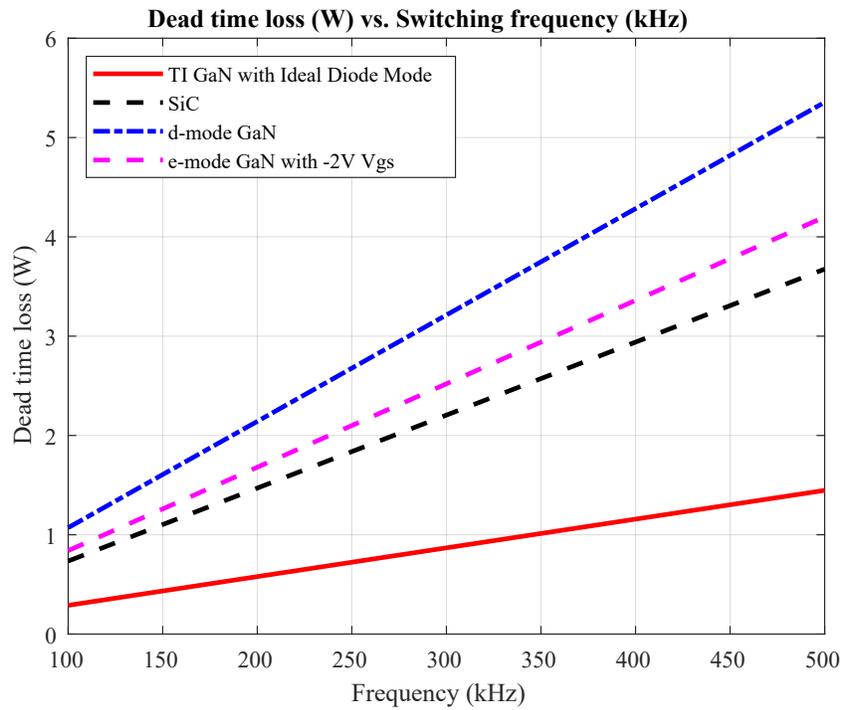


Figure 2-3. Dead Time Loss Versus Frequency With 100ns Dead Time Settings

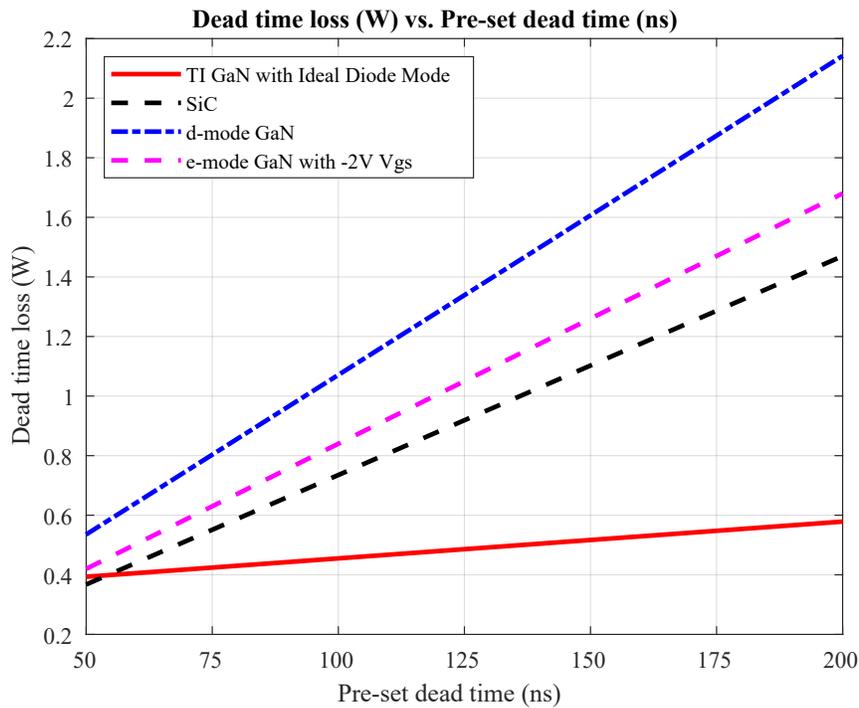


Figure 2-4. Dead Time Loss Versus Dead Time Settings With 200kHz Switching Frequency

2.3 TI GaN Ideal Diode Mode Test Results

Experiments were conducted to validate the effectiveness of ideal diode mode for loss reduction during dead time. At first, the experiment waveform without ideal diode mode is presented. Two LMG3422R030 devices are configured in a half-bridge, and are tested in a buck converter setup utilizing the LMG3422EVM-043 EVM card. The dead time is configured to be 200ns, with 40 V bus voltage and 4 A of output current. As shown in [Figure 2-5](#), with 200 ns dead time setting, the device remains in third quadrant conduction for more than 180 ns, and excessive dead time loss is generated due to the high reverse conduction loss. This loss will be even higher as the load current further increases.

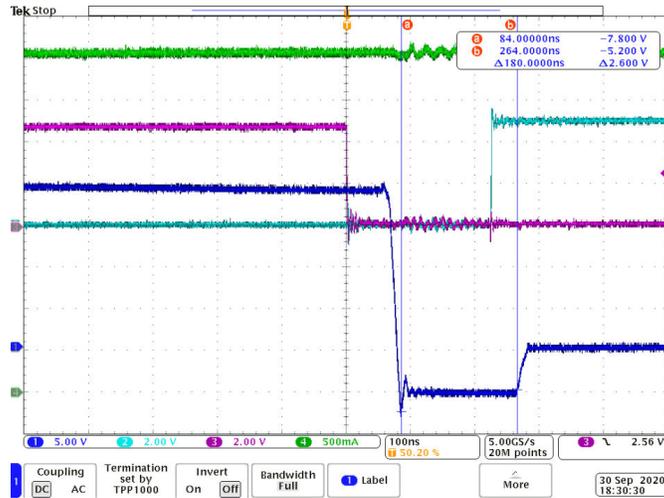


Figure 2-5. GaN Without Ideal Diode Mode Shows 180ns Of Dead Time With 200ns Dead Time Setting

In comparison, the ideal diode mode feature is evaluated on the LMG3425EVM-043 EVM card, which configures two LMG3425R030 devices with the ideal diode mode feature in a half-bridge configuration. Under the same buck converter setup and dead time setting (200ns), the third-quadrant conduction period is reduced to 38 ns as shown in [Figure 2-6](#), and the GaN is automatically turned on by the ideal diode mode feature even though the PWM input signal is still low. As can be seen, the reverse conduction loss can be significantly reduced with the aid of TI GaN's ideal diode mode feature.

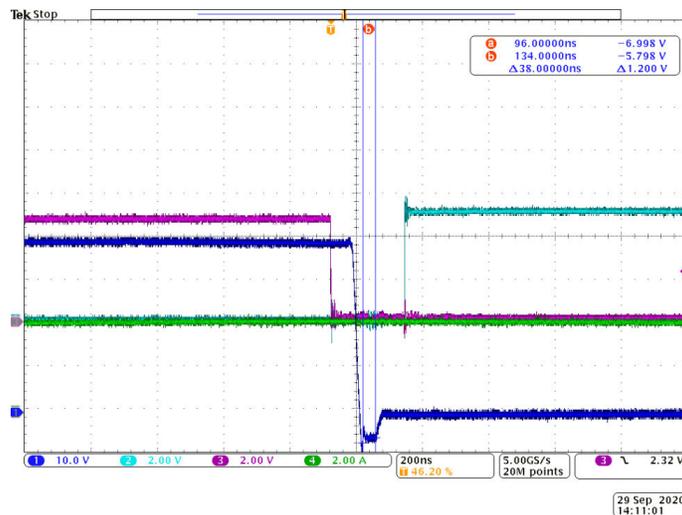


Figure 2-6. TI GaN With Ideal Diode Mode Shows 38ns Of Dead Time With 200ns Dead Time Setting

3 Conclusion

GaN HEMT has intrinsic advantages over Si with smaller gate charge, smaller output capacitance and zero reverse recovery loss. To further improve the efficiency, dead time needs to be optimized for GaN to reduce the third quadrant conduction loss. Compared to the traditional adaptive dead time approach, TI GaN with ideal diode mode requires zero external circuitry and control to minimize the dead time. A background and overview of the TI GaN's ideal diode mode along with loss estimation and experimental results have been provided to designers to better understand the feature and its benefits.

4 References

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2. [TIDA-010062](#)
3. [PMP20637](#)
4. [SNOAA36](#)
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