

# AN-2224 LP8727B Micro/Mini USB Interface With Integrated 28V Charger Evaluation Kit

Ville Allikvere

#### **ABSTRACT**

The LP8727B is designed to provide automatic multiplexing switches between a Micro/Min USB connector and USB, UART and Audio paths in cellular phone applications. It also contains a single-input Li-Ion battery charger and an over-voltage protected LDO. Programming is handled via an I<sup>2</sup>C-compatible Serial Interface allowing control of the charger, multiplexing switches, and reading status information of the device.

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www.ti.com General Description

## 1 General Description

The LP8727B is designed to provide automatic multiplexing switches between a Micro/Min USB connector and USB, UART and Audio paths in cellular phone applications. It also contains a single-input Li-Ion battery charger and an over-voltage protected LDO. Programming is handled via an I<sup>2</sup>C-compatible Serial Interface allowing control of the charger, multiplexing switches, and reading status information of the device.

The multiplexing switches on USB and UART support high-speed USB, and audio inputs can be driven to negative voltage rail. The LP8727B is compatible with USB charging specifications rev 1.1 from USB IF.

The Li-lon charger requires few external components and integrates the power FET. Charging is thermally regulated to obtain the most efficient charging rate for a given ambient temperature. It has an Over-Voltage Protection (OVP) circuit at the charger input protecting the PMU (Power Management Unit) from input voltages up to +28V, eliminating the need for any external protection circuitry.

An over-voltage-protected LDO which can supply up to 50 mA is designed for powering up low-voltage USB transceiver or waking up a PMU when an external power source (either USB VBUS or wall adapter) is connected to the USB connector.

The LP8727B PMU is available in a 25-bump 0.4 mm pitch thin micro SMD package (2.015 mm x 2.015 mm).

#### 2 Features

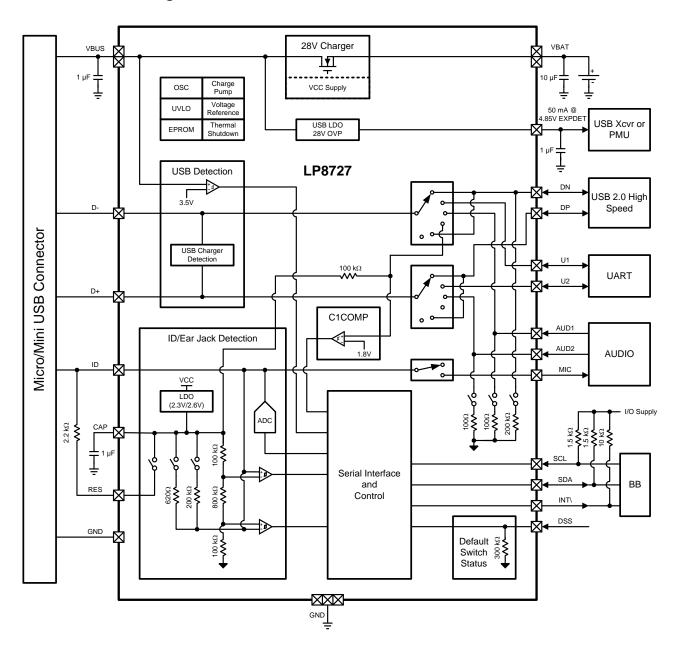
- · USB Multiplexing Switches
  - High-speed USB on USB and UART Inputs
  - Negative Voltage Rail on Audio Inputs
  - Internal LDO for ID detection and MIC Bias
  - Compatible with USB Charging Specification Rev. 1.1
  - DSS Input for Default Switch Connection
  - Low-Power MIC Standby Mode
- Linear Charge with Single Input
  - 28 OVP On VBUS input
  - High-Current Mode For Production Test
  - Thermal Regulation
- Over-Voltage Protected LDO For USB Transceivers And PMU Wakeup
- UVLO (Under-voltage Lock Out)
- Interrupt Request To Reduce SW Polling
  - USB / ID Detection
  - SEND / END Button Detection
  - MIC Removal
  - OVLO / UVLO On VBUS
  - Charger Status
- Thermal Shutdown Protection
- I<sup>2</sup>C-Compatible Serial Interface
- 25-bump 0.4 mm Pitch Thin micro SMD Package

#### 3 Applications

- GSM, GPRS, EDGE, CDMA and WCDMA Handsets
- Portable Media Players/MP3 Players

LP8727B Block Diagram www.ti.com

## 4 LP8727B Block Diagram



## 5 Evaluation Kit Overview

The LP8727B Evaluation Kit is based on all on-board system. The board operates through the USB port. The kit supports complete functional evaluation of the LP8727B circuit. The evaluation kit consists of:

- LP8727B Evaluation Board REV1
- USB Interface Cable
- · CD including:
  - Evaluation software for PC REV 1.0.7
  - LP8727B datasheet
  - Evaluation Kit document (this document)



www.ti.com Evaluation Kit Setup

## 6 Evaluation Kit Setup

Please use ESD protection when handling the evaluation boards to prevent any damage due to ESD events.

## 6.1 Hardware Setup

Connect the LP8727B Evaluation Board to the USB port of a PC using the USB cable.

When the USB board is plugged in for the first time, the operating system prompts for "New hardware found" and installs the USB driver. If this does not happen, try unplugging, then plugging in the cable again.

#### 6.2 Software Setup

LP8727B evaluation software can be run directly from the CD by double-clicking its icon. It can also be copied to the PC's hard disk and run from there. However, we recommend that it be copied to the PC's hard disk and run from there.

The software is now ready to start and will automatically detect the type of interface board used.

Please note: for a WinXP like OS, administrator rights may be required to run the software.

Always disconnect the USB cable from the computer when inserting or removing the evaluation board or changing jumper settings. Failing to do so may stop the evaluation board respond.

If the evaluation board is not responding or the software hangs up, disconnect the USB cable for 5 seconds.

The evaluation software allows control of all registers necessary to program the device. To simplify the use of the software, the registers are set by directly named controls; you do not need the register value as this is taken care of by the software, (for example, to change charging current, choose the related value and the software will send the correct value to the control register).

## 6.3 Using the Evaluation Software

The graphic user (GUI) interface has a main screen background with 2 tab screens that allow control and indication for different functions of the device.

Once the evaluation board is connected to the PC, serial communication is enabled, and the device can be controlled via the software interface.

Because of jumper settings, The LP8727B should become active as soon as the micro-USB cable or the battery is plugged. All the device functions can be accessed via the software.

#### 6.3.1 Main Screen

The right, upper, and lower parts of the screen are visible as the background for both tab screens. Common functions can be controlled from here.

## 6.3.2 The Upper Part of the Screen

Access to the device registers is allowed via the Direct Register Access frame. Binary data may be written and read from the registers. Use the hexadecimal address in the 'Addr (HEX): input window and use the buttons to create the correct binary data to be written. The Read and Store buttons carry out the action, and the returned data from a Read command is shown in the 'Data (BIN):' window.

The Poll Pins check box allows the continuous reading (1 reading per second) of the evaluation chip pins and the results of on-board ADC. The Poll Status check box allows the continuous reading (1 reading per second) of the evaluation chip status register.

The Auto Write check box is enabled by default. Auto Write will enable the settings generated from using the pulldown menu or buttons to be sent to the chip after every mouse click. If Auto Write is disabled, all registers are written after clicking the Write Regs button. In this way, you can change values in several registers and get all changes done simultaneously.



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#### 6.3.3 The Lower Part of the Screen

**Measure:** This will update and display the LDOs, the battery, VBUS voltages measured on the on-board ADCs.

Read Pins: This button reads status of the chip output pin.

**Read Regs:** This control initiates an all register read to update the indicators on the screens. Use this button if the direct register write/read facility has been used. This will update the screen to correctly indicate status.

Write Regs: If Auto Write check box is disabled, you can press this button to overwrite all register space.

**Indicators ('Chip Interface'):** The two boxes at the bottom left of the main screen show the interface type and the communication status.

## 6.3.4 The Right Part of the Screen

This part of the screen shows the output voltages and  $\overline{\text{INT}}$  pin state. The buttons in this frame are for controlling on board relays.

#### 6.3.5 System Settings Tab

Selecting this tab allows access to the controls for the device System Status/Interrupts, System Control, Charger Control.

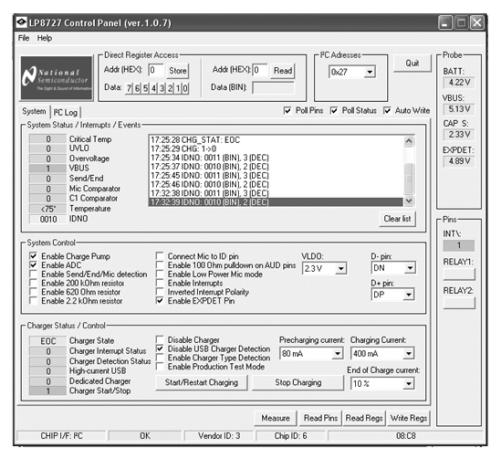


Figure 1. LP8727B Evaluation Software System Settings Tab



www.ti.com Evaluation Kit Setup

## 6.4 System Status and Interrupts Frame

#### 6.4.1 Interrupt Status

The LP8727B has 2 interrupt status registers: INT\_STAT1 and INT\_STAT2. These interrupt conditions are generated from VBUS comparator, D+/D- and ID detection, changes of SEND/END and MR\_COMP states, and charger events.

When any of these interrupt conditions occur, then the open drain output (INT) will be brought low. This change will show in Event Log window. If the Poll Status is checked, then the on-board USB controller reads two INT\_STAT1 and INT\_STAT2 registers sequentially through the serial interface to determine which bit caused the interrupt. Once the status register indicates the actual interrupt condition starts to be read, the INT output will be brought high immediately.

#### 6.4.2 Device Status

The LP8727B has two device status registers: STATUS1 and STATUS2. These registers can be read via the serial interface in much the same way as the interrupt status registers. These registers are not cleared on a read and always represent the current state.

### 6.5 UVLO and OVLO

The LP8727B measures system voltages on VBUS input and compares it to selected voltages. The function uses two comparators.

UVLO state '1' indicates that the voltage is below normal working range.

OVLO state '1' indicates that the voltage is over normal working.

#### 6.6 Thermal Shutdown

The thermal shutdown (TSHD) function monitors the chip temperature to protect the chip from temperature damage caused by excessive power dissipation.

When the chip temperature exceeds 160°C, '1' is written to TSHD bit on INT\_STAT2 register and INT is pulled to low; the LP8727B then initiates SHUTDOWN.

The STARTUP operation after TSHD trigger can be initiated only after the chip has cooled down to the +115°C threshold.

## 6.7 Temperature Monitor

The LP8727B supports the chip temperature monitoring feature. When the chip temperature reaches each temperature threshold, the TMP bit on INT\_STAT2 is set to '1', and it pulls the INT output low. The chip temperature can be obtained by reading TMP\_STAT bits on STATUS2 register.

#### 6.8 C1 Comparator

The C1 comparator can be used for detecting D- threshold (1.8V). The comparator state is available from STATUS1 register as a read-only bit. It is also possible to connect or disconnect from the software CONTROL register.

#### 6.9 Events Window

This window shows the current status of chip and includes the Event Log also.

#### 6.10 System Control Frame

In this frame the enable check boxes are provided.

#### 6.11 Charger Status and Control Frame

This frame allows control of charging functions of the chip.



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## 6.12 Charging Current

The charging current has 10 programmable values from 90 mA to 1000 mA. The possible charging current options are shown in pulldown window.

#### 6.13 Production Test Mode (PTM)

If PTM bit is set, then the charger enters special high-load mode. In this mode the charger should be able to supply up to 2.3A.

## 6.14 Precharge

Following the correct detection of a voltage at the charger input, the charger enters precharge mode. In this mode the battery is charged with a small constant current. If battery reaches the full-rate charging threshold, then the charger will move on to full charging mode. Pre-charge settings are available in register 0x08.

## 6.15 End-of-Charge Current and Restart

When an EOC condition is met, the LP8727B will generate an interrupt to the processor; the processor is responsible for controlling the charger operation (top-off or maintenance mode) via I<sup>2</sup>C. Once the charger goes into maintenance mode (stop charging), you are also responsible for monitoring the battery voltage and restarting the charger when the battery voltage drops to restart voltage by pressing Start/Restart Charging button. Pressing the Stop Charging button will cancel all charger activities.

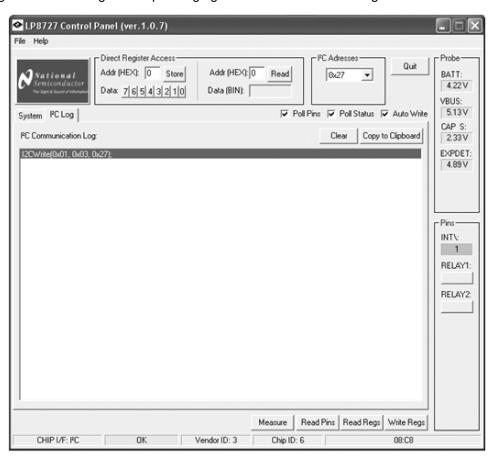


Figure 2. LP3925 Evaluation Software I<sup>2</sup>C Log Tab

## 6.16 I2C Log Tab

This tab screen allows trace I<sup>2</sup>C writing; you can copy write sequence to the Clipboard.



www.ti.com Control Registers

## 6.17 Slave Address

The current version of software supports slave address for LP8727B hex(27) only.

## 7 Control Registers

Addr	Register	POR Default	Bit7 <sup>(1)</sup>	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0					
0x00	DEVICE ID	0011xxxx		VENDOR ID			VENDOR ID				CHIF	_REV			
0x01	CONTROL1	x0000001	RESV'D	ID_2P2	ID_620	ID_200	VLDO	SEMREN	ADC_EN	CP_EN					
0x02	CONTROL2	0000xx01	INTPOL	INT_EN	MIC_L P	CP_AUD	RESV'D	RESV'D	CHG_TY P	USB_DET_ DIS					
0x03	SW CONTROL	x0000000	RESV'D	MIC_ON	DP2		DP2		DP2		DP2		DM1		
0x04	INT_STAT1	00000000	CHGDET	MR_ COMP	SEND/ END	VBUS	IDNO								
0x05	INT_STAT2	00000000	CHG	TSHD	TMP	OVLO	UVLO	RESV'D	RESV'D	RESV'D					
0x06	STATUS1	00000000	DCPORT	CHPORT	CHG	_STAT	RESV'D	RESV'D	RESV'D	C1COMP					
0x07	STATUS2	00000000	Т	MP_STAT		RESV'D	RESV'D	RESV'D	RESV'D	RESV'D					
0x08	CHARGER CONTROL1	010010xx	CHG_EN	EXPDET_ EN	PTM	CHG_OF F	IPRE	CHG	RESV'D	RESV'D					
0x09	CHARGER CONTROL2	0010x001	CHG_SET				RESV'D		IMIN_SET						

<sup>(</sup>Bolded locations are Read-Only Bits.)
Resv'd = Reserved



## 8 Detail Register Descriptions

**Table 1. Register Descriptions** 

Addr	Register Name	Bit Name (1)	Bit	POR Default	Description
000	DEVICE ID	CHIP_REV	[3:0]	xxxx	Chip revision.
0x00		VENDOR ID	[7:4]	0011	NSC vendor ID.
					Enable charge pump for analog switch operation.
		CP_EN	0	1	When CP_EN = 0, input signals to the analog switches should not go below GND.
					0: Disable
					1: Enable
					Enable ID detection LDO and internal ADC.
		ADC_EN	1	0	0: Disable
					1: Enable
			2	0	Enable ID detection LDO and SEND/END and MR comparators.
	CONTROL1	SEMREN			0: Disable
					1: Enable
		VLDO	3	0	ID detection LDO voltage setting.
					0: 2.3V
0x01					1: 2.6V
		ID_200	4	0	Connect ID detection LDO to ID pin through an internal 200 k $\Omega$ resistor.
					0: Disable
					1: Enable
					Connect ID detection LDO to ID pin through an internal $620\Omega$ resistor.
		ID_620	5	0	0: Disable
					1: Enable
		ID_2P2	6	0	Connect ID detection LDO to RES output for microphone biasing. A 2.2 k $\Omega$ external resistor is required between RES and ID pins.
					0: Disable
					1: Enable
		RESERVED	7	х	Not used.

<sup>(1)</sup> **Bolded** entries are read-only.



## **Table 1. Register Descriptions (continued)**

Addr	Register Name	Bit Name (1)	Bit	POR Default	Description
7144	riogioto: riumo				Disable USB charger detection.
		USB_DET_DIS	0	1	0: Enable
					1: Disable
				0	Enable charger type detection. CHG_TYP will be automatically set to 0 at the end of detection sequence.
		CHG_TYP	1		0: Disable
					1: Enable
		RESERVED	[3:2]	xx	Not used.
				_	Enable internal 100 $\Omega$ pull-down resistors on AUD1 and AUD2.
		CP_AUD	4	0	0: Disable
0x02	CONTROL2				1: Enable
					Enable microphone low-power mode.
		MIC_LP	5	0	0: Disable
					1: Enable
			6	0	Enable interrupt output. When disabled, INT output will be masked and pending interrupts will not be cleared.
		INT_EN			0: Disable
					1: Enable
		INTPOL	7	0	Interrupt polarity setting.
					0: Active low
					1: Active high
			[2:0]	000	Set the switch connection to D- pin.
					000: D- pin is connected to DN pin.
		DM1			001: D- pin is connected to U1 pin.
					010: D- pin is connected to AUD1 pin.
					011: D- pin is connected to C1COMP.
					100: D- pin is connected to DN pin regardless of VBUS
					101 to 111: Hi-Z
					Set the switch connection to D+ pin.
000	OW CONTROL				000: D+ pin is connected to DP pin.
0x03	SW CONTROL				001: D+ pin is connected to U2 pin.
		DP2	[5:3]	000	010: D+ pin is connected to AUD2 pin.
					011: Hi-Z
					100: D+ pin is connected to DP pin regardless of VBUS
					101 to 111: Hi-Z
		MIC_ON	6		Connect MIC pin to ID pin.
				0	0: Disable
					1: Enable
		RESERVED	7	х	Not used.



## **Table 1. Register Descriptions (continued)**

	1			•	(Continued)
Addr	Register Name	Bit Name (1)	Bit	POR Default	Description
		IDNO	[3:0]	0000	ADC output with 200 k $\Omega$ / 2.2 k $\Omega$ / 620 $\Omega$ of pullup resistor (Activated only when ADC_EN = '1'). Change of IDNO state triggers assertion of $\overline{\text{INT}}$ output.
		VPUO			VBUS comparator output. Change of VBUS state triggers assertion of INT output.
		VBUS	4	0	0: V <sub>VBUS</sub> < V <sub>VBUSDET</sub>
					1: V <sub>VBUS</sub> > V <sub>VBUSDET</sub>
		SEND/END	5	0	SE comparator output (Activated only when SEMREN = '1'). Change of SEND/END state triggers assertion of INT output.
0x04	INT_STAT1				0: V <sub>MIC</sub> > V <sub>SEND/END</sub>
	_				1: V <sub>MIC</sub> < V <sub>SEND/END</sub>
		MR_COMP	6	0	MR comparator output (Activated only when SEMREN = '1'). Change of MR_COMP state triggers assertion of INT output.
		_			0: V <sub>MIC</sub> < V <sub>MR_COMP</sub>
					1: V <sub>MIC</sub> > V <sub>MR_COMP</sub>
		CHO DET	7	0	Charger detection is completed. Change of CHG_DET state will trigger assertion of INT output.
		CHG_DET			0: VBUS is not present or no charger is detected.
					1: Charger is detected.
	INT_STAT2	RESERVED	[2:0]	000	Not used.
		UVLO	3	0	0: V <sub>VBUS</sub> > UVLO <sub>USB</sub>
				Ŭ	1: V <sub>VBUS</sub> < UVLO <sub>USB</sub>
		OVLO	4	0	0: V <sub>VBUS</sub> < V <sub>OV</sub>
					1: V <sub>VBUS</sub> > V <sub>OV</sub>
0x05		ТМР	5	0	0: TMP_STAT state is not changed.
				5	1: TMP_STAT state is changed.
		TSHD	6	0	0: Thermal shutdown is not triggered.
					1: Thermal shutdown is triggered.
		СНС	7	0	0: CHG_STAT state is not changed.
					1: CHG_STAT state is changed.
			0	0	C1COMP output.
		C1COMP			0: V <sub>D</sub> .< V <sub>D-DET</sub>
					1: V <sub>D</sub> .> V <sub>D-DET</sub>
		RESERVED	[3:1]	000	Not used.
					Charger status.
0.5-	074740	0116 0===			00: Pre-charge
0x06	STATUS1	CHG_STAT	[5:4]	00	01: Fast charging
					10: Not used
		CHPORT	6		11: EOC
				0	0: High-current USB Host/Hub is not detected.
					1: High-current USB Host/Hub is detected.
		DCPORT	7	0	0: Dedicated charger is not detected.
					1: Dedicated charger is detected.



## **Table 1. Register Descriptions (continued)**

Addr	Register Name	Bit Name (1)	Bit	POR Default	Description
		RESERVED	[4:0]	00000	Not used.
					Die temperature.
					000: 75°C
					001: 95°C
007	07.471.100				010: 115°C
0x07	STATUS2	TMP_STAT	[7:5]	000	011: 135°C
					100: Reserved
					101: Reserved
					110: Reserved
					111: Reserved
		RESERVED	[1:0]	XX	Not used.
	CHARGER CONTROL1	IPRECHG	[3:2]	10	Pre-charge current setting.
					00: 40 mA
					01: 60 mA
					10: 80 mA
					11: 100 mA
			4	0	Charger block disable.
					0: Enable
0x08					1: Disable
UXUO				0	Enable production test mode (PTM).
		PTM	5		0: Disable
					1: Enable
					Enable EXPDET LDO.
		EXPDET_EN	6	1	0: Disable
					1: Enable
					Charger stop / start control.
		CHG_EN	7	0	0: Stop charging (Force EOC).
					1: Start charging (Restart).



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**Table 1. Register Descriptions (continued)** 

Addr	Register Name	Bit Name (1)	Bit	POR Default	Description
			10.01	001	EOC level setting.
					000: 5%
					001: 10%
		IMINI SET			010: 16%
		IMIN_SET	[2:0]		011: 20%
					100: 25%
					101: 33%
					110: 50%
	CHARGER CONTROL2	RESERVED	3	х	Not used.
0x09		CHG_SET	[7:4]	0010	Charging current setting.
0.03					0000: 90 mA
					0001: 100 mA
					0010: 400 mA
					0011: 450 mA
					0100: 500 mA
					0101: 600 mA
					0110: 700 mA
					0111: 800 mA
					1000: 900 mA
					1001: 1000 mA

## 9 Evaluation Board Hardware

## 9.1 Power Supply to the Board

The on-board USB controller and ADC are powered from dedicated USB port through mini-USB connector J9.

The LP8727B can be powered from a battery connector J2 or from the micro-USB connector CON1. If VBUS voltage is provided from the micro-USB connector, then the jumper JP8 has to be set. The pins of JP8 may be used for current measurements also.

Additionally, the external VBUS connector J1 is provided.

On-board relays can be used for power routing for downstream USB ports. The relays should be controlled by you through the software buttons RELAY1 and RELAY2.

**Table 2. Battery Connector Pins** 

Pin	Function
1	Battery positive terminal
2	GND
3	GND
4	No connection

## 9.2 Using the Evaluation Hardware

The connector J3 is provided to allow an EXPDET LDO output load connection.

Jumpers allow you to disconnect LP8727B from the on-board USB controller and to connect to the target system. The logic input/output signals can be accessed externally through JP2( $\overline{\text{INT}}$ ), JP3(SCL), JP4(SDA). Set or remove the jumpers from JP2 to JP4 accordingly.



Test points for EXPDET, BATT, VBUS and CAP voltage measurements also are provided.

## 10 LP8727B Evaluation Board Layout and Schematics

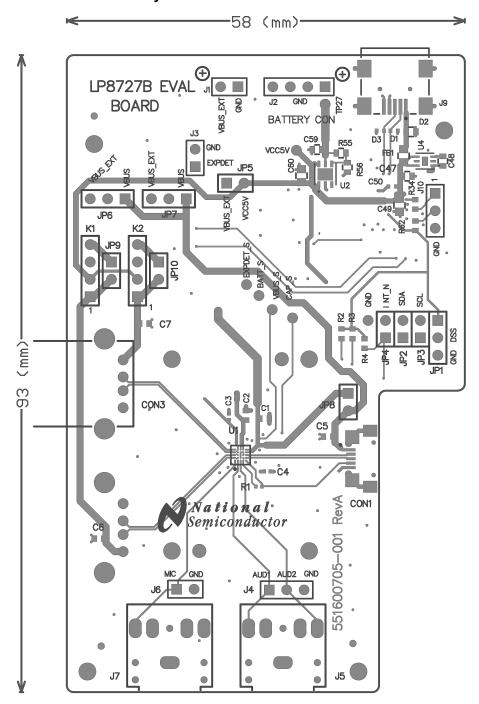


Figure 3. LP8727B Layout



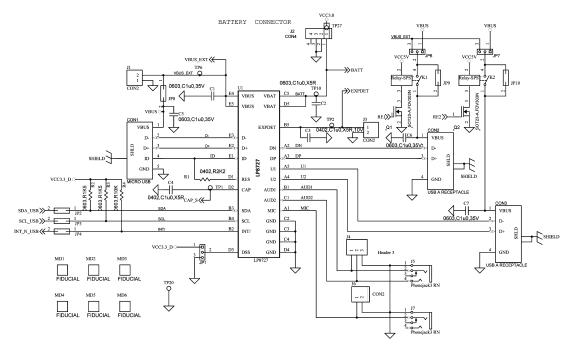


Figure 4. Schematic of Evaluation Board (part 1)

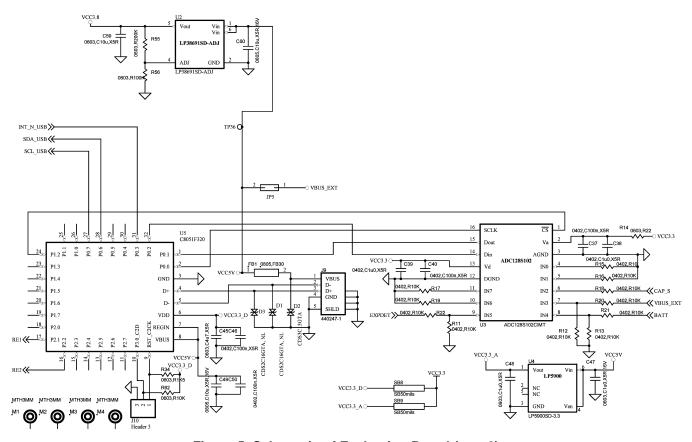


Figure 5. Schematic of Evaluation Board (part 2)

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