LP8863-Q1 External Component Selection Guide

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ABSTRACT

The LP8863-Q1 device is an automotive LED driver with a boost or SEPIC converter to support infotainment display, automotive cluster, and lighting applications. Automotive displays often require high brightness for better visibility under bright ambient conditions; therefore, LED drivers that support automotive displays also require high output power, which often causes high voltage ripple, current limitation, and instability of the boost loop. Automotive applications also require a wide input voltage of the boost converter, making the selection of boost components difficult. This application note provides the information for boost components recommended for various LP8863-Q1 application conditions.

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1 Typical Application

Figure 1 shows a connection diagram for a typical LP8863-Q1 application. The LP8863-Q1 device uses an external switching FET with gate drive controlled internally to support high power conditions. Switching FET (Q1), inductor (L1), Schottky diode (D1), and output capacitors (C_{OUT}) are required to form a boost converter topology. The LP8863-Q1 needs more components to configure boost characteristics and device operation such as a power-line FET (Q2), input current-sensing resistor (R_{ISENSE}), boost current-sense resistor (R_{SENSE}), input capacitors (C_{IN}), boost feedback resistors (R_{FB1}, R_{FB2}), charge-pump flying (C_{2X})/output (C_{PUMP}) capacitors, SD pulldown resistor (R_{SD}) for power-line FET, and bypass capacitors (C_{VDD}, C_{LDO}) for power rails. Section 2 shows how to calculate the required rating of each component or generic values commonly used.

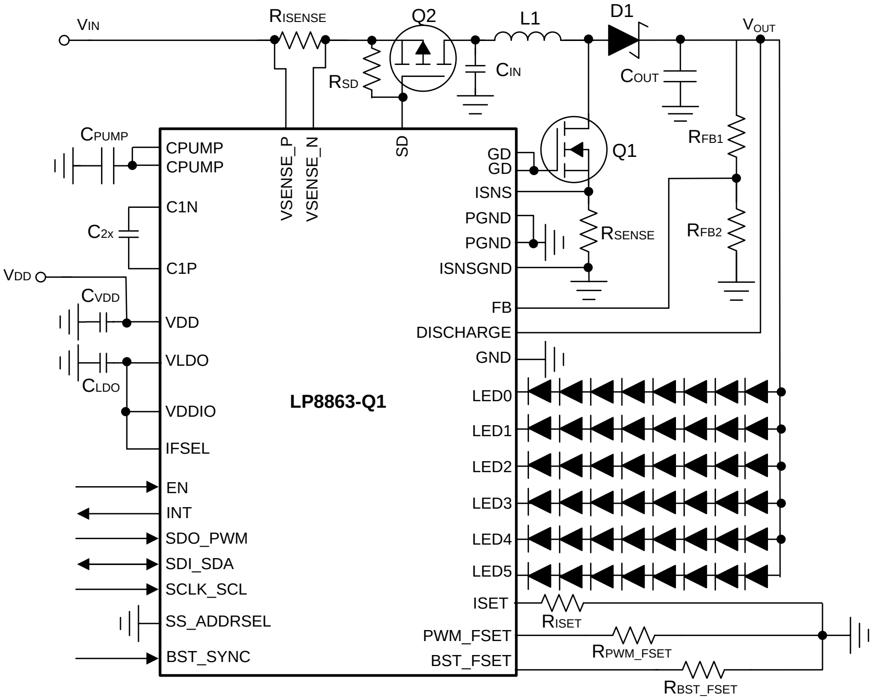

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Figure 1. Simplified Schematic for LP8863-Q1 Application

2 External Components of LP8863-Q1

2.1 Inductor Selection

There are a few things to consider when selecting inductors including inductance, current rating, and DCR.

Inductance of the LP8863-Q1 circuit is provided by Table 1, and all boost compensation controls are set automatically depending on switching frequency. Current rating can be calculated as following:

$$D = 1 - \frac{V_{IN(min)} \times \eta}{V_{OUT}}$$

where

- D = boost duty cycle
- $V_{IN(min)}$ = minimum input voltage
- V_{OUT} = desired output voltage
- η = efficiency of the converter, estimated at 80%. This efficiency varies with load condition, switching frequency, and components, but 80% is a good estimation to start. (1)

Maximum switching current of the boost is calculated with Equation 2:

$$I_{SW(max)} = \frac{\Delta I_L}{2} + \frac{I_{OUT(max)}}{1 - D}$$

where

- ΔI_L = inductor ripple current
- $I_{OUT(max)}$ = maximum output current necessary in the application. (2)

ΔI_L can be calculated with a given inductor value:

$$\Delta I_L = \frac{V_{IN(min)} \times D}{f_S \times L}$$

where

- f_S = minimum switching frequency (3)

The current rating of the inductor must be at least 25% higher than the maximum switching frequency of the boost calculated with Equation 2.

The $DCR_{(max)}$ must be lowest possible to minimize DC loss, but package size increases for lower DCR inductor. Consideration between package size and DCR is required for inductor selection.

Table 1 shows the recommended inductor values for each frequency selection. The inductor values were selected from simulation/calculation results. Maximum current rating must be still calculated by preceding equations. Switching frequency is the most dominant factor when considering selection of inductor value.

Table 1. Inductance Values for Switching Frequencies

SWITCHING FREQUENCY (kHz)	INDUCTANCE (µH)
300	22
400	22
600	15
800	15
1000	10
1250	10
1667	10
2222	10

2.2 Output Capacitor Selection

The voltage rating of the capacitors must be at least 25% higher than output voltage level to consider the variation of each component (50% or higher is recommended). Output capacitance required for a desired output voltage ripple is shown in Equation 4:

$$C_{OUT(min)} = \frac{I_{OUT(max)} \times D}{f_S \times \Delta V_{OUT}}$$

where

- $C_{OUT(min)}$ = minimum capacitance
- $I_{OUT(max)}$ = maximum output current of the application
- D = duty cycle calculated with Equation 1
- f_S = minimum switching frequency of the converter
- ΔV_{OUT} = desired output voltage ripple (4)

The ESR of the output capacitor(generally electrolytic capacitors) adds more ripple with Equation 5:

$$\Delta V_{OUT(ESR)} = ESR \times \left(\frac{I_{OUT(max)}}{1 - D} + \frac{\Delta I_L}{2} \right)$$

where

- $\Delta V_{OUT(ESR)}$ = additional output voltage ripple due to ESR of capacitor
- ESR = equivalent series resistance of the used output capacitor
- $I_{OUT(max)}$ = maximum output current of the application (5)

Output capacitors also affect boost stability as well as inductor value. High enough capacitance results in decent (> 45 to 50 degrees) phase/gain margin. As a typical value, TI recommends using 2 × 33-µF electrolytic capacitors and 2 × 10-µF ceramic capacitors for most application conditions; these components were used on LP8863-Q1EVM. 2 × 33-µF electrolytic capacitors ensure high enough capacitance to reduce voltage ripple and increase boost stability. Electrolytic capacitors must support high ripple current of boost output stage, which can be a few Amps depending on load conditions. Generally, Al-polymer capacitors support higher ripple current compared to regular Al electrolytic capacitors. This ripple current must be checked on capacitor manufacturer's data sheet for best selection.

Capacitance of ceramic capacitors degrade linearly with DC bias voltage. Therefore, TI recommends using ceramic capacitors with high enough (50% to 100% higher) voltage rating compared to application conditions. Table 2 shows recommended capacitor values for each application condition. These are simulated values to make high enough stability (phase margin > 45 to 50 degrees) when the correct boost-current-sensing resistor values for each application condition are used, which is explained in Section 2.7. These values can be used as initial references and increased to better support warm or cold crank conditions. Effective capacitance must be considered for ceramic capacitors, which is de-rated by bias voltages. Actual required capacitance required is more than calculated values. Two 10-µF ceramic capacitors help reduce the ESR effect of electrolytic capacitors, which can affect voltage ripple.

Table 2. Recommended Capacitance for Each Application Condition C_{OUT}(µF) – Effective Output Capacitance

V_{IN} (V)	V_{OUT} (V)	I_{LOAD} (A)	SWITCHING FREQUENCY (kHz)			
			300/400	600/800	1000/1250	1650/2220
INDUCTOR			22 µH	15 µH	10 µH	10 µH
6 to 9	20 to 27	0.4	3 × 10	3 × 10	3 × 10	3 × 10
		0.6				
		0.9				
	28 to 35	0.4	3 × 10	3 × 10	3 × 10	3 × 10
		0.6				
		0.9				
	36 to 43	0.4	3 × 10 (V_{IN} 6 V – 4 × 10)	3 × 10	4 × 10	4 × 10
		0.6				
		0.9				
10 to 15	20 to 27	0.4	2 × 10	2 × 10	2 × 10	2 × 10
		0.6				
		0.9				
	28 to 35	0.4	2 × 10	2 × 10	2 × 10	2 × 10
		0.6				
		0.9				
	36 to 43	0.4	2 × 10	2 × 10	2 × 10	2 × 10
		0.6				
		0.9				
16 to 21	21 to 27	0.4	1 × 10	1 × 10	2 × 10	2 × 10
		0.6				
		0.9				
	28 to 35	0.4	2 × 10	2 × 10	2 × 10	2 × 10
		0.6				
		0.9				
	36 to 43	0.4	2 × 10	2 × 10	2 × 10	2 × 10
		0.6				
		0.9				
22 to 27	28 to 35	0.4	1 × 10	1 × 10	2 × 10	2 × 10
		0.6				
		0.9				
	36 to 43	0.4	1 × 10	1 × 10	2 × 10	2 × 10
		0.6				
		0.9				

2.3 *Input Capacitor Selection*

The voltage rating of capacitors must be at least 25% higher than output voltage level to consider the variation of each component (50% or higher is recommended for ceramic capacitors). Input capacitance is not critical for boost operation, but it must support enough filtering for input power and charges for both normal operation and transition state such as warm/cold crank conditions. TI recommends same capacitance with output capacitance for a simple application, but input capacitance can be reduced monitoring input power requirements.

2.4 *Output Diode Selection*

The voltage rating of the output diode must be at least 25% higher than the output voltage level to consider the variation of each component. A diode with short transition/recovery time and low forward voltage, such as a Schottky diode, must be selected to reduce power loss. The forward voltage of Schottky diodes is lower than regular PN-junction diodes. It is important to make sure that the forward voltage of a Schottky diode at maximum current at application is as low as possible. Forward voltage itself affects power loss by P = V × I, and if this increases with load current, reverse recover time is also increased, which often causes high switching current across the switching FET. A forward voltage < 0.5 V for all target conditions is necessary.

2.5 *Switching FET Selection*

The switching FET is a critical component to decide power efficiency of boost DC-DC converter. A few things to consider when selecting a switching FET are switching voltage, current rating, R_{DSON}, power dissipation, thermal resistance, input capacitance, rise/fall time, total gate charge, Miller voltage, and gate-input resistance.

- Voltage rating must be at least 25% higher than boost output voltage.
- Current rating of switching FET can be obtained from the calculation of maximum switching current for inductor selection. Current rating of switching FET must be at least 25% higher than calculated value.
- R_{DSON} must be as low as possible. Typical value used for LP8863-Q1 applications is < 20 mΩ.
- Maximum power dissipation must be at least a few times higher than expected power loss on the FET
- Thermal resistance (for example, $R_{\theta JA}$) must be also low to dissipate heat from power loss on switching FET, but lower thermal resistance means a larger package size, thus this trade-off must be considered.
- Input capacitance, rise/fall time, total gate charge, and Miller voltage affect switching speed of switching FET. Typical ranges of each parameter are:
  - Input capacitance: < 1000 pF
  - Rise/fall time: a few ns — approximately 1 × ns
  - Total gate charge: a few nC — approximately 1 × nC
  - Miller voltage: 2 V to 3 V
- Input resistance of switching FET must be considered not to make gate drive current higher than 2.5 A. Gate drive current can be calculated by V_{GD} / (G_{DRDSON} + total resistance to gate input of SW FET). If gate drive current is higher than 2.5 A with switching FET, add a series resistor on gate drive path to lower current.

2.6 *Power-Line FET Selection*

A power-line FET can be used to protect boost components in case of any fault conditions such as an overcurrent state. The power-line FET disconnects input power from boost input, therefore prevents excessive current flow into LP8863-Q1 device itself and other boost components. A P-type MOSFET is used for power-line FET and there are no requirements for switching speed. The voltage rating of a power-line FET must be at least 25% higher than input voltage range. Low R_{DSON} is important to reduce power loss on the FET. Typical value is < 20 mΩ.

2.7 *Boost Feedback Divider Resistor Selection*

Two resistor values on the FB input of the LP8863-Q1 device determine maximum boost output voltage. Figure 2 shows the structure of the feedback input block.

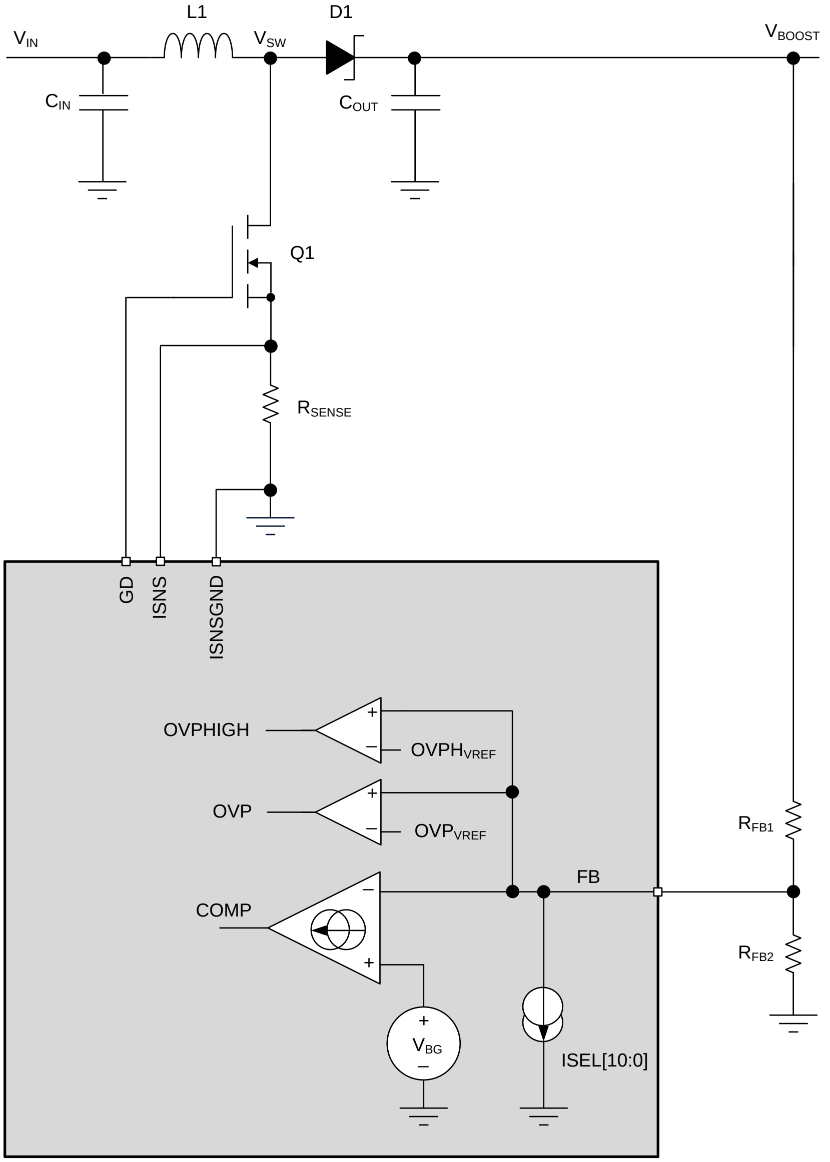

Figure 2. LP8863-Q1 Feedback Divider

Equation 6 and Equation 7 show calculations for maximum output voltage:

$$V_{OUT\_MAX} = \left(\frac{V_{BG}}{R_{FB2}} + I_{SEL\_MAX} \right) \times R_{FB1} + V_{BG} \tag{6}$$

$$V_{OUT\_MIN} = \left(\frac{V_{BG}}{R_{FB2}} + I_{SEL\_MIN} \right) \times R_{FB1} + V_{BG}$$

where

- V_{BG} = 1.21 V
- I_{SEL_MAX} = 38.381 µA
- I_{SEL_MIN} = 0 µA (7)

For example, default values on the EVM are:

R_{FB1} = 910 kΩ and R_{FB2} = 100 kΩ; V_{OUT_MAX} = 47.15 V, V_{OUT_MIN} = 12.22 V.

2.8 SD Pulldown Resistor Selection

SD is the pulldown signal to enable the power-line FET to connect external power source to boost input. SD current through resistor between source and gate makes voltage difference (V_{GS}) to turn on the FET. The typical value of SD pulldown current is 292 µA, and V_{GS} = 292 µA × R_{SD} must be higher than the maximum V_{GS} specification of the power-line FED to turn it on correctly.

2.9 Input Current Sense Resistor Selection

The input current sense resistor (R_{ISENSE}) is used as a sensor to detect input overcurrent fault. An overcurrent condition is detected when the voltage across the sensor resistor is higher than 230 mV. Typical sense resistor value is 20 mΩ, so the overcurrent limit becomes 11.5 A. This sense resistor value can be increased to lower the overcurrent limit as needed for each application; for example, 230 mV/OCP limit = sense resistor value.

2.10 Boosting Switch Current Sense Resistor Selection

Boost current sense resistor (R_{SENSE}) is used as a sensor to decide boost overcurrent condition (not a fault) for every boost switching cycle. The typical resistor value is 15 mΩ for maximum current condition 13.5 A, and this sense resistor value can be increased to lower overcurrent limit. Be careful when increasing resistor value because it affects the maximum duty cycle of boost. Table 3 shows boost current sense resistor values for various load conditions.

Table 3. Boost Current Sense Resistor Values for Various Load Conditions (Maximum R_{SENSE} (mΩ))

V_{IN} (V)	V_{OUT} (V)	I_{LOAD} (A)	SWITCHING FREQUENCY (kHz)			
			300/400	600/800	1000/1250	1650/2220
INDUCTOR			22 µH	15 µH	10 µH	10 µH
6 to 9	20 to 27	0.4	50	59	62	60
		0.6	40	45	45	42
		0.9	27	30	28	28
	28 to 35	0.4	40	47	46	45
		0.6	30	33	31	30
		0.9	23	25	22	21
	36 to 43	0.4	36	40	36	35
		0.6	25	28	24	23
		0.9	15	20	16	15
10 to 15	20 to 27	0.4	72	90	91	98
		0.6	58	65	65	68
		0.9	40	45	45	47
	28 to 35	0.4	51	70	71	75
		0.6	45	50	51	52
		0.9	34	38	35	35
	36 to 43	0.4	50	59	59	61
		0.6	40	45	41	42
		0.9	30	32	31	28
16 to 21	21 to 27	0.4	90	120	128	145
		0.6	79	94	96	105
		0.9	60	69	69	74
	28 to 35	0.4	76	96	98	110
		0.6	60	72	73	80
		0.9	45	53	53	56
	36 to 43	0.4	65	79	81	90
		0.6	50	59	60	65
		0.9	38	42	43	45
22 to 27	28 to 35	0.4	90	113	122	143
		0.6	76	92	94	105
		0.9	56	69	70	76
	36 to 43	0.4	76	94	97	114
		0.6	60	73	75	84
		0.9	45	55	56	60

2.11 Charge-Pump Flying/Output Capacitor Selection

An integrated charge pump can be used to supply high gate-drive voltage of switching FET. To use the charge pump, a 2.2-µF capacitor is required as a flying capacitor between C1P and C1N, and a 10-µF capacitor is required for the charge-pump output to hold the energy for the gate drive. Voltage rating of both capacitors must be at least 25% higher than the gate-drive level of switching FET (50% or higher is recommended)

2.12 Bypass Capacitor Selection for VDD/VLDO/VDDIO

TI recommends at least 1-µF capacitance for VDD and VDDIO, and 4.7 µF for VLDO near the pins. The voltage rating of each capacitor must be at least 25% higher than each voltage level (50% or higher is recommended).

2.13 Components on Evaluation Board

Table 4 shows the components are used on the LP8863-Q1EVM evaluation board as examples. All components listed in Table 4 support operation temperature –40°C to +125°C, and all capacitors are X7R type.

Table 4. Component List for LP8863Q1EVM Evaluation Board

COMPONENTS	SW FREQUENCY = 300/400 kHz	SW FREQUENCY = 600/800 kHz	SW FREQUENCY = 1000/1250 kHz	SW FREQUENCY = 667/2222 kHz
Boost inductor	SRP1770TA-220M (22 µH)	IHLP6767GZER150MA1 (15 µH)	IHLP5050FDER100M01 (10 µH)	IHLP5050FDER100M01 (10 µH)
Boost input capacitors	EEH-ZC1J330P × 2 (2 × 33-µF electrolyte)			
	C5750X7S2A106M230KB × 2 (2 × 10-µF ceramic)			
Boost output capacitors	EEH-ZC1J330P × 2 (2 × 33-µF electrolyte)			
	C5750X7S2A106M230KB × 2 (2 × 10-µF ceramic)			
Output diode	FSV10100V (Schottky, 100 V, 10 A)			
Switching FET	NVMFS5C682NLT3G (60 V, 25 A)			
Power-line FET	SQJ461EP (60 V, 30 A)			
Boost feedback-divide resistors	R1 (upper): RC0603FR-07910KL (910 kΩ, 0.1 W); R2 (lower): RC0603FR-07100KL (100 kΩ, 0.1 W)			
SD pulldown resistor	CRCW06030K0FKEA (20 kΩ, 0.1 W)			
Input current-sense resistor	CRA2512-FZ-R020ELF (20 mΩ, 3 W)			
Boost current-sense resistor	CRA2512-FZ-R015ELF (15 mΩ, 3 W)			
Charge-pump flying capacitor	GRM21BR71E225KA73L (2.2 µF, 25 V)			
Charge-pump output capacitor	C3216X7R1C106M (10 µF, 16 V)			
Bypass capacitor - VDD	LMK212B7475KG-T (4.7 µF, 10 V)			
Bypass capacitor - VLDO	GRM21BR71A106KE51L (2.2 µF, 25 V)			
Bypass capacitor - VDDIO	0603ZK475KAT2A (4.7 µF, 10 V)			

3 Summary

Recommended external component values for the LP8863-Q1 device can be selected by input/output voltages, load current, and other component values, accordingly, as previously explained. It is very important to note that these values are only simulated or calculated values, not tested for entire use cases. User can refer to these recommended values as a starting point and must consider extra margins of characteristics for each component.

4 References

- TI Application Report *Basic Calculation of a Boost Converter's Power Stage*
- Simulation results for the LP8863-Q1 device

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (April 2017) to A Revision	Page
• First public release to WEB	1

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