

# Mitigating the Indeterminate Output of a Voltage Supervisor (Reset IC) During Power Up/Down



## What is the indeterminate output voltage issue on the output of a voltage supervisor?

Voltage Supervisors (Reset ICs) require a minimum voltage called the Power-on-Reset Voltage ( $V_{POR}$ ) on the supply pin before the internal circuitry that creates the voltage reference for comparing the sensed voltage is operational. Specifically,  $V_{POR}$  defines the minimum required voltage threshold to turn on the internal output MOSFET (circled in RED in Figure 1) that defines the output logic state. When the supply voltage is below  $V_{POR}$ , the output logic state is undefined and the output voltage is indeterminate. The indeterminate output voltage only appears at the output (RESET) of an active-low Voltage Supervisor when VDD is below  $V_{POR}$ .

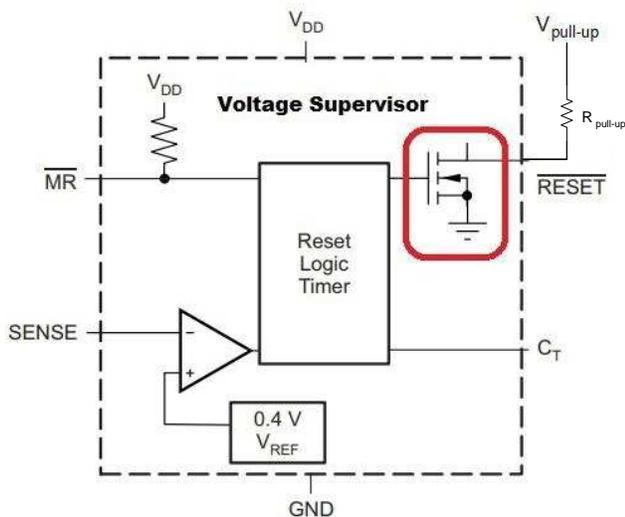
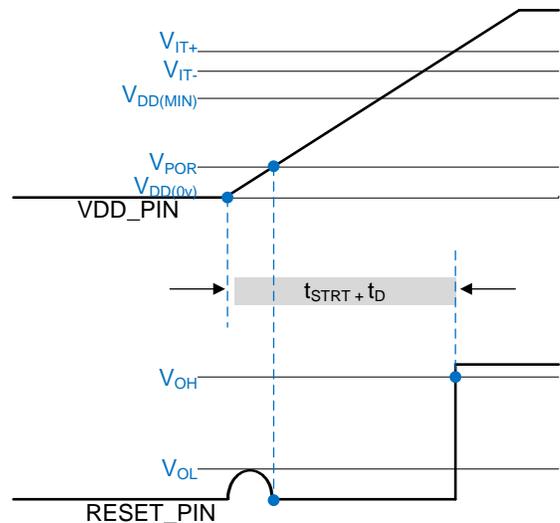


Figure 1. Voltage Supervisor Latch Circuit

When  $V_{DD}$  is below  $V_{POR}$ , there isn't enough voltage for the internal circuitry driving the output MOSFET to operate so the output MOSFET is off and the supervisor has no way to control the output RESET voltage. As shown in Figure 2, RESET will rise up in proportion to the pull-up voltage,  $V_{PULL-UP}$ , until the

voltage at  $V_{DD}$  is above  $V_{POR}$  to provide enough voltage to turn on the internal MOSFET to pull RESET to GND. Since RESET may have a voltage potential when  $V_{DD}$  is not above the undervoltage threshold ( $V_{IT}$ ) of the supervisor, an error could result in the system.



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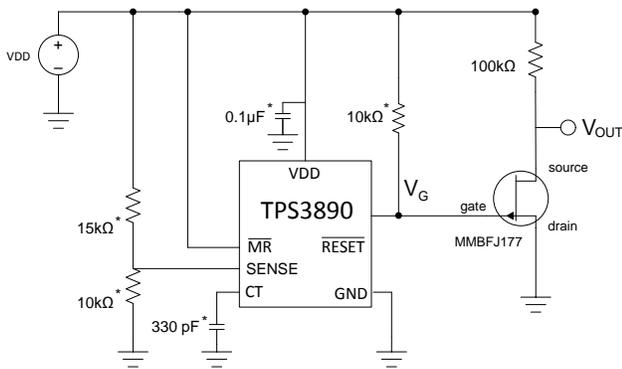
Figure 2. Timing Diagram of Device Startup

Once  $V_{DD}$  is above  $V_{POR}$ , the internal MOSFET turns on, connects RESET to GND, and causes RESET to output the correct low logic level.

For active-high output devices, the same indeterminate voltage occurs when  $V_{DD}$  is below  $V_{POR}$ , but when  $V_{DD}$  is below  $V_{IT}$ , the device is supposed to pull-up to logic high anyway, so seeing a voltage potential at RESET in this case is not considered an issue.

## How to prevent the indeterminate output voltage when $V_{DD}$ is below $V_{DD(min)}$ ?

In the case the system cannot accept the output voltage being undefined when  $V_{DD}$  is below  $V_{POR}$ , adding a P-channel junction field effect transistor (JFET), to RESET as shown in Figure 3 ensures that the output remains low even during power up and power down.

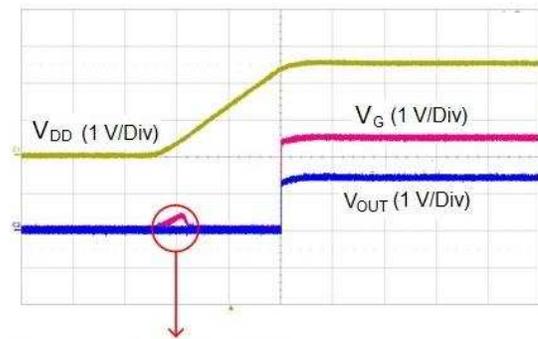


\* = Components populated on TPS3890 EVM (TPS3890EVM-775)

**Figure 3. Adding a P-type JFET to Mitigate the Indeterminate Output Voltage**

In **Figure 3**, the normal output of the TPS3890 voltage supervisor is represented as  $V_G$ . When  $V_{DD}$  rises, the voltage at  $V_G$  also rises because the internal circuitry driving the MOSFET is not operational yet. By adding a standard JFET configured in a source-follower configuration, the voltage at the source (labeled as  $V_{OUT}$ ) will follow the voltage at  $V_G$  minus the threshold voltage of the JFET. The threshold of the JFET causes approximately a 1V drop between  $V_G$  and  $V_{OUT}$  and eliminates the voltage potential rise on the output until the internal circuitry becomes operational. Note: when connecting the  $V_{OUT}$  of the JFET to the next device, the user must account for the drop in output voltage caused by the JFET threshold.

**Figure 4** shows the effect of using a JFET on the output of a TPS3890. The Yellow trace shows the power supply at  $V_{DD}$ , the Pink trace shows the rising indeterminate system output as  $V_{DD}$  rises using just the voltage supervisor, and the Blue trace shows the system output remaining low as  $V_{DD}$  rises using the voltage supervisor with the additional JFET.



$V_G$  rises up to  $\sim 400$  mV because  $V_{DD}$  is too low to pull  $V_G$  to 0V

**Figure 4. TPS3890 Start-up with JFET (Blue Trace) and without JFET (Pink Trace)**

This solution can be used for all active-low supervisors with proper choice of the JFET and pull-up resistor. The selected JFET should have a voltage threshold higher than  $V_{POR}$  so the JFET remains turned on connecting the system output to GND until after  $V_{POR}$  in which the voltage supervisor internal circuitry is operational and causes system output to be in the correct defined logic state. The selected pull-up resistor should be low enough for the required system output response time and high enough to minimize the voltage drop across the JFET when conducting.

**Table 1. Alternative Device Recommendations**

Device	Description
TPS3808	SOT package type
TPS389x	Additional output topologies, higher $V_{DD(max)}$

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