Interlace Operation in TI Virtual-Phase CCD Image Sensors

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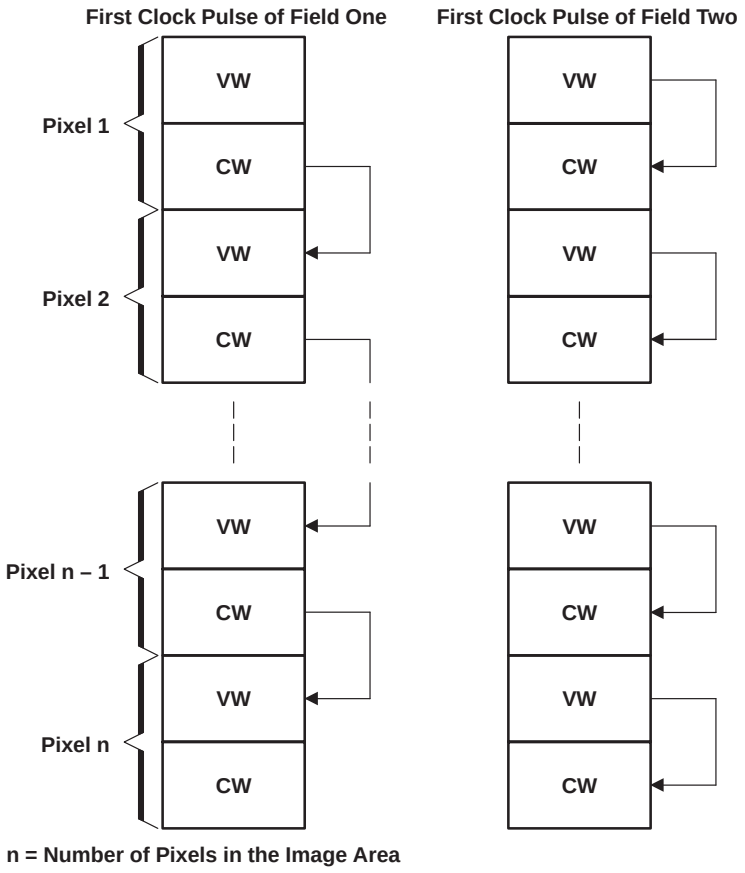

Figure 1. Virtual-Phase Pixel Structure and Centroid Shift

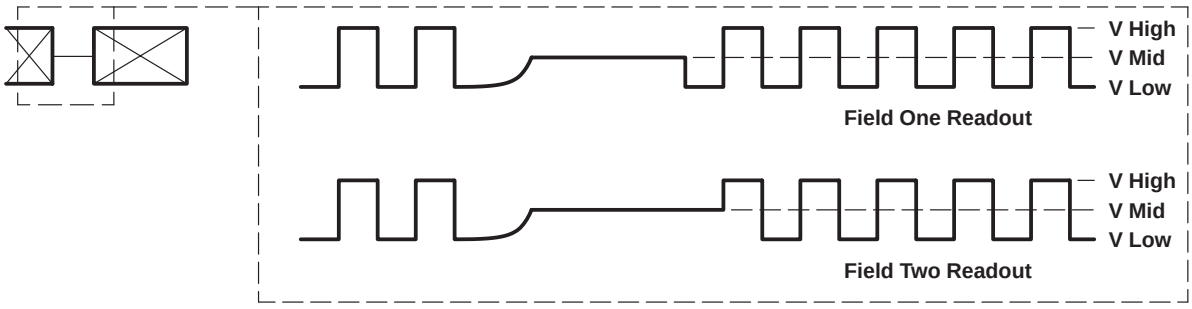

Figure 2. Image-Area Gate Timing for Interlace

NOTES: A. Interlace operation is obtained by performing a centroid shift on the virtual-phase pixels.
B. The centroid shift is obtained by holding the image-area gate at mid-level during integrate time and making a mid-to-low transition at the start of field one and then making a mid-to-high transition at the start of field two.
C. Optimum midlevel for the image-area gate (IAG) is obtained when the charge is equally distributed between the virtual well (vW) and the clocked well (cW).
D. Antiblooming needs to be clocked for interlace to work.
E. Adjustment is as follows:
IAG midlevel should be low (about –10 V). AB+ should be low (about 0 V).
While viewing a saturated target, increase AB+ until the signal is 35% of full well.
Increase IAG midlevel until the signal doubles.