Impact of ZPLL Jitter on CAN Communication

Peter Steffan, Rainer Troppmann

Advanced Embedded Control

ABSTRACT

The first section describes the impact of the clock jitter introduced by the analog phase−locked loop module (ZPLL) on the system clock (SYSCLK) and the peripheral clock (ICLK). In the second section, the resulting impact on the CAN communication is explained.

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1 Impact of ZPLL Clock Jitter on SYSCLK and ICLK

Texas Instruments, Inc, (TI) has taken PLL jitter characterizations on multiple TMS470 x10 and x05 devices across voltage, temperature, and frequency. 20,000 random samples of the period were measured on each tested device at a given voltage, temperature, and frequency condition. The worst case PLL jitter that was measured was well within ± 5%. The ZPLL has a maximum relative clock jitter of ±5%. This jitter relates to the output frequency of the ZPLL module (= f_{ZPLL}).

A natural behavior of the ZPLL module is that jitter never accumulates, i.e., during one or more f_{OSC} cycle(s) an absolute clock jitter of $\frac{0.05}{f_{ZPLL}}$ can be measured.

The maximum absolute jitter at the output of a locked ZPLL is seen when the lowest possible frequency is used as the reference clock for the ZPLL and the minimum value for the ZPLL feedback divider *M*. Using the ZPLL in combination with an oscillator, the lowest frequency for the ZPLL reference clock is given by the minimum frequency of the crystal as $f_{Crystalmin}$.

For an oscillator frequency of 4 MHz and a feedback divider of 4, the maximum clock deviation caused by PLL jitter would be 0.05 x 62.5 ns = 3.125 ns. This absolute clock deviation is valid for one or more clock cycles. Measuring the overall clock deviation during 100 or 1000 cycles would also reveal a maximum accumulated drift caused by a PLL jitter of 3.125 ns.

The signal flow diagram in Figure 1 visualizes the dependency of the PLL clock jitter on the CAN bit timing.

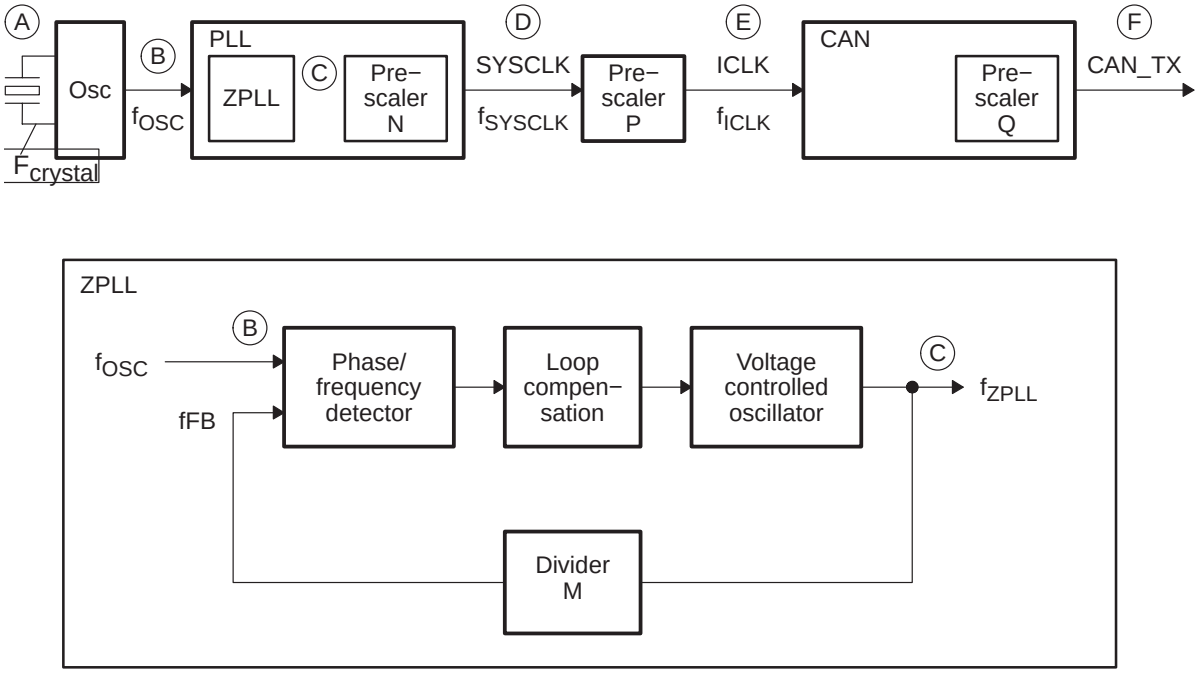

Figure 1. Dependency of PLL Clock Jitter on the CAN Bit Timing

Relevant parameters for F05 devices:

$f_{Crystal}$ = 4..20MHz

$f_{OSC} = f_{Crystal}$

$f_{SYSCLK} = \frac{M}{N} * f_{OSC}$; $f_{SYSCLKmax}$ is device−dependent

$f_{ICLK} = \frac{1}{P} * f_{SYSCLK}$; $f_{ICLKmax}$ = 25MHz

$CANdatarate = \frac{1}{Q} * f_{ICLK}$; $CANdatarate_{max}$ = 1Mbit/s (ISO11898)

with:

M = 4 or 8

N = 1..8

P = 1..16

Q = 1..256

TI measurements using a jitter−free reference clock at the oscillator input (point A) as the clock source have shown that the worst case PLL jitter at the ZPLL output (point C) is well within ±5%. Since these measurements include also the jitter caused by the oscillator, a model can be used to discuss the impact of the PLL jitter on the clocks used. The model assumes the oscillator to be jitter−free and the maximum jitter is located at the ZPLL output.

Assuming that the crystal will not introduce jitter, the worst case scenario is shown in Table 1, where [M=4, N=1, P=1, Q=16]:

Table 1. Worst−Case Scenario for Jitter at ZPLL Output

Location	A	B	C	D	E	F
Frequency	$f_{Crystal}$= 4MHz	f_{OSC}= 4MHz	f_{ZPLL}= 16MHz	f_{SYSCLK}=16MHz	f_{ICLK} = 16MHz	datarate = 1Mbit/s
Period	$t_{Crystal}$= 250ns	t_{OSC}= 250ns	t_{ZPLL}= 62. 5ns	t_{SYSCLK} = 62.5ns	t_{ICLK} = 62.5ns	t_{data} = 1000ns
Absolute jitter	0	0	3.125ns	3.125ns	3.125ns	3.125ns
Relative jitter	0	0	5%	5%	5%	0.3125%
Jitter @ frequency	0 @ 4MHz	0 @ 4MHz	± 3.125ns @ 16MHz	± 3.125ns @ 16MHz	± 3.125ns @ 16MHz	± 3.125ns @ 1MHz

The relative clock jitter is varying with the different prescalers (see Table 1); however the absolute clock jitter stays the same, independent of the prescaler values N, P, and Q. In addition, keep in mind that the clock jitter never accumulates, i.e., the absolute maximum clock jitter is never exceeded no matter how many clock cycles are considered.

Assuming that the crystal does not introduce jitter, a typical case scenario is shown in Table 2, where [M=8, N =2, P=3, Q=20].

Table 2. Typical Case Scenario for Jitter at ZPLL Output

Location	A	B	C	D	E	F
Frequency	$f_{Crystal}$= 15MHz	f_{OSC}= 15MHz	f_{ZPLL}= 120MHz	f_{SYSCLK}= 60MHz	f_{ICLK} = 20MHz	datarate = 1Mbit/s
Period	$t_{Crystal}$= 66.67ns	t_{OSC}= 66.67ns	t_{ZPLL}= 8.33ns	t_{SYSCLK}= 16.67ns	t_{ICLK} = 50ns	t_{data} = 1000ns
Absolute jitter	0	0	0.4165ns	0.4165ns	0.4165ns	0.4165ns
Relative jitter	0	0	5%	2,5%	0,833%	0,04165%
Jitter @ frequency	0 @ 15MHz	0 @ 15MHz	±0.4165ns @ 120MHz	±0.4165ns @ 60MHz	±0.4165ns @ 20MHz	±0.4165ns @ 1MHz

2 Impact of ZPLL Clock Jitter on CAN Communication

In the previous section, the following rules for the ZPLL clock jitter were discussed:

- The maximum relative clock jitter at the ZPLL output is ±5%.
- The clock jitter never accumulates, i.e. the maximum absolute clock deviation measured over more than one clock cycle never exceeds $\frac{0.05}{f_{ZPLL}}$.

These two rules help to define the worst−case scenario for the CAN communication:

- Reducing the oscillator frequency to a minimum increases the absolute ZPLL clock jitter to its maximum.
- Increasing the CAN bit rate to its maximum increases the clock deviation relative to the CAN bit time to its maximum.

Minimum $f_{Crystal}$ = 4MHz (according to the specific TMS470R1x data sheet)

Minimum f_{ZPLL} = 16MHz

Maximum CAN bit rate = 1 Mbit/s (according to ISO11898)

Assuming a falling−edge synchronization is selected for the CAN controller, the clock deviation relative to the CAN bit time can be calculated as follows:

$$\Delta CAN = \frac{0.05}{f_{zpll} \times n \times CBT}$$

where:

n = number of CAN bits between two falling edges

CBT = CAN bit time in [ns]

The parameter *n* describes the number of bits between two successive synchronizations. It can have a value between 2 (1 dominant bit + 1 recessive bit) and 10 (5 dominant bits + 5 recessive bits). Taking the above worst−case parameters into consideration, the relative clock deviation with varying *n* can be calculated as follows:

f_{ZPLL} = 16MHz

CBT = 1000ns (1Mbit/s)

The results are shown in Table 3.

Table 3. Relative Clock Deviation with Varying *n*

n	2	3	4	5	6	7	8	9	10
Δ_{CAN} in [%]	0.15625	0.10425	0.07825	0.0625	0.052	0.04475	0.039	0.03475	0.03125

The maximum clock deviation introduced by the clock jitter varies from 0.15625% to 0.03125%. The worst−case scenario for CAN communication is usually n = 10, since the static resonator/crystal drift is highest. Here, the relative ZPLL clock jitter is the lowest.

To get a better grasp on the above result, the relative clock deviation can be compared to the atomic unit of a CAN bit (time quantum TQ):

According to the maximum possible ICLK frequency, the maximum CAN controller clock is 25 MHz. Assuming that the prescaler Q is set to 1, the CAN bit comprises 25 time quanta at 1 Mbit/s. One time quantum corresponds to a time of 40 ns (1000 ns/25). The absolute clock deviation is constant over a varying number of clock cycles, here it is 3.125 ns.

The clock deviation relative to one time quantum is below 7.8125% (3.125 ns/40 ns), i.e., the clock jitter is well below the atomic unit of a CAN bit and therefore has very low impact on the CAN communication.

3 Summary

In contrast to the static clock deviation of a crystal or resonator (manufacturing tolerance, temperature, and time drift), the clock deviation caused by the ZPLL clock module is a fixed absolute time value that does not change over any number of clock cycles. In fact, the relative clock deviation, which is important for CAN communication, decreases over an increasing number of clock cycles.

In a worst case scenario, the ±5% ZPLL jitter causes a clock deviation of ± 0.03125% at 1Mbit/s over a synchronization period of 10 CAN bit times. This corresponds to a share of 7.8125% of a time quantum, which represents the atomic unit of a CAN bit. At a bit rate of 500 kBit/s, the above worst case values are even divided in half (±0.015625%).

The clock deviation calculated in the first section has a very low impact on CAN communication. Nevertheless, it is still recommended to take the individually determined clock jitter into account when calculating the maximum allowed crystal/resonator tolerance.

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265