Application Report
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Recommended Initializations for TMS570LS20x/10x Microcontrollers

TMS570 ARM Cortex-R4F MCUs

ABSTRACT

This application report covers the recommended initialization procedure for TMS570LS20x/10x Microcontrollers. It includes core registers, memories, ECC, FPU, clocks, and peripherals.

Contents

1 Introduction and Features

This section describes the recommended initialization for core registers, ECC, clocks, peripherals, and memory.

1.1 Features for Initialization on the TMS570LS20x/10x Cortex™-R4F Device

The following items are necessary for proper initialization of the device:

- Initialization of internal R4F core registers and return stack
- Setup stacks
- Configure Flash memory option
- Setup system and peripheral clocks

The following items are optional:

- FPU initialization
- ECC initialization

For an overview of the lock-step device and checker module, see the *Core Compare Module for Cortex-R4F* section in the *TMS570LS20216 Technical Reference Manual* (SPNU489). This lock-step device has two CPU's that run the same program code. The output signals of those cores are compared in the checker module, which allows for detection of faults in the CPU. If a compare fail occurs during execution, the compare error signal is generated to the error signaling module (ESM). To prevent an error during the system initialization, internal core registers need to be initialized to a predefined state.

The Cortex-R4F core supports seven modes of operation: user (USR), fast interrupt (FIQ), interrupt (IRQ), supervisor (SVC), abort (ABT), system (SYS) and undefined (UND). All modes except user mode are considered to be in privilege state. Additional details about the Cortex-R4F can be found in the *Cortex-R4 and Cortex-R4F Technical Reference Manual* available from ARM® at http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0363e/ch01s10s03.html.

During this initialization, the core is configured in system mode. Registers (R0 - R13), as well as the banked registers, need to be initialized so that core compare will not report an erroneous failure. The following register initialization sequence is in assembly language instructions for TI compilers. Comments are shown beside the assembly instructions for further clarification.

```
•mov   r0,      #0x2DF    Configure core to system mode for initialization
•msr   cpsr,    r0
•mov   r1,      #0
•mov   r2,      #0
•mov   r3,      #0
•mov   r4,      #0
•mov   r5,      #0
•mov   r6,      #0
•mov   r7,      #0
•mov   r8,      #0
•mov   r9,      #0
•mov   r10,     #0
•mov   r11      #0
•mov   r12      #0
•mov   r13      #0
```

The following initialization code configures the core to FIQ mode and uses its corresponding Stack Pointer Register (SPSR).

```
•mov   r0,      #0x2D1
•msr   cpsr,    r0
•mov   r8,      #0
•mov   r9,      #0
•mov   r10,     #0
•mov   r11,     #0
•mov   r12,     #0
•mov   r13,     #0
•mov   r14,     #0
•msr   spsr_cxsf, r6
```

The following initialization code configures the core to IRQ mode and uses its corresponding SPSR register.

```
•mov   r0,      #0x2D2
•msr   cpsr,    r0
•mov   r14,     #0
•msr   spsr_cxsf, r6
```

The following initialization code configures the core to SVC mode and uses its corresponding SPSR register.

```
•mov   r0,        #0x2D3
•msr   cpsr,      r0
•mov   r14,       #0
•msr   spsr_cxsf, r6
```

The following initialization code initializes FPU registers with two ARM core registers.

```
•fmdrr d0,  r1, r1
•fmdrr d1,  r1, r1
•fmdrr d2,  r1, r1
•fmdrr d3,  r1, r1
•fmdrr d4,  r1, r1
•fmdrr d5,  r1, r1
•fmdrr d6,  r1, r1
•fmdrr d7,  r1, r1
•fmdrr d8,  r1, r1
•fmdrr d9,  r1, r1
•fmdrr d10, r1, r1
•fmdrr d11, r1, r1
•fmdrr d12, r1, r1
•fmdrr d13, r1, r1
•fmdrr d14, r1, r1
•fmdrr d15, r1, r1
```

The following initialization is for the return stack of Cortex-R4F.

- bl $+4
- bl $+4
- bl $+4
- bl $+4
- mov r14, #0

Each CPU mode supports a SPSR. Depending on the application, software needs to configure the SPSR register of different modes with the appropriate memory address. The address of each stack is software dependent.

The following initialization code configures the address for the SVC stack.

```
• ldr          sp,  [pc]
• mov          pc,  pc
• .word 0x08001300  The start address is software application dependent
```

The following initialization code configures the address for the FIQ stack.

- mov r0, #0x2D1
- msr cpsr, r0
- ldr sp, [pc]
- mov pc, pc
- .word 0x08001600 *The start address is software application dependent*

The following initialization code configures the address for the IRQ stack.

- mov r0, #0x2D2
- msr cpsr, r0
- ldr sp, [pc]
- mov pc, pc
- .word 0x08001500 *The start address is software application dependent*

The following initialization code configures the address for the user/system stack. Both user and system mode use the same CPSR register. This changes the device from privilege mode to user mode. The following configuration requires the device to be in privilege mode:

- mov r0, #0x2DF
- msr cpsr, r0
- msr spsr, r6
- ldr sp, [pc]
- mov pc, pc
- .word 0x08001700 *The start address is software application dependent*

It is necessary to enable FPU prior to using it. This setup needs be performed in privilege mode. Configuration of FPU is possible with coprocessor registers.

Configure the coprocessor 11 and 10 to be user accessible, which requires enabling of the Neon/VFP coprocessor access control register.

Setup of privilege and user mode access to coprocessors CP10 and CP11. Set to 0b11 to enable the access.

- MRC p15,#0x0,r0,c1,c0,#2 *bits {23:22} of CP11 and {21:20} of CP10*
- MOV r3, #0xf00000
- ORR r0, r0, r3
- MCR p15, #0x0, r0, c1, c0, #2
- mrc p15, #0x0, r0, c0, c0

Set the EN bit of FPEXC[30] to enable Neon/VFP

- MOV r0, #0x40000000
- VMSR FPEXC, r0
- VMRS R1, FPSID

Prior to enabling the ECC, initialize all the device memories. Enable the RAM memories for hardware initialization with the MBIST Controller/Memory Initialization Enable Regoster (MSINENA) and the MBIST Hardware Initialization Global Control Register (MMINITGCR). Verify that the memory initialization is complete by reading the MINIDONE bit of the Memory Self-Test Fail Status Register (MSTCGSTAT).

Default enable/disable of ECC is device dependent. If ECC is disabled after reset, the following assembly language instructions can turn on the ECC of ATCM, B0TCM, and B1TCM interfaces. Explanation of TCM interfaces is available in the *Cortex-R4 and Cortex-R4F Technical Reference Manual*. The device-specific data sheet details the memories that are connected to these interfaces.

```
•MRC   p15,#0,r1,c15,c0,#0
•ORR   r1, r1, #0x00000003     Set 0th and 1st bit of Aux Cntrl Reg2 to enable RMW for A and B TCMs
•MCR   p15,#0,r1,c15,c0,#0x0
•MRC   p15,#0,r1,c9,c12,#0     Reading back to verify that the write happened properly or not
```

The following initialization code disables the RMW on TCM interfaces.

```
•MRC   p15,#0,r1,c15,c0,#0
•ORR   r1, r1,#0x1<<0
•MCR   p15,#0,r1,c15,c0,#0x0

•MRC   p15,#0,r1,c15,c0,#0
•ORR   r1, r1,#0x1<<1
•MCR   p15,#0,r1,c15,c0,#0x0

•MRC   p15,#0,r1,c15,c0,#0     2nd Aux Cntrl Reg used for the correction of data
•ORR   r1, r1,#0x1<<2
•MCR   p15,#0,r1,c15,c0,#0x0

•MRC   p15,#0,r1,c15,c0,#0     Aux
```

The following initialization code enables ECC on TCM's with the Auxiliary Control Register.

```
•MRC   p15, #0, r1, c1, c0, #1   Enable ATCM with 1st Aux Cntrl Reg for the ecc checking
•ORR   r1, r1, #0x1<<25
•DMB
•MCR   p15, #0, r1, c1, c0, #1
•ISB

•MRC   p15, #0, r1, c1, c0, #1   Enable B0TCM with 1st Aux Cntrl Reg for the ecc checking
•ORR   r1, r1, #0x1<<26
•DMB
•MCR   p15, #0, r1, c1, c0, #1
•ISB
```

```
•MRC    p15, #0, r1, c1, c0, #1    Enable B1TCM with 1st Aux Cntrl Reg for the ecc checking
•ORR    r1, r1, #0x1<<27
•DMB
•MCR    p15, #0, r1, c1, c0, #1
•ISB
```

The flash wrapper provides multiple configurations of Flash memory. Flash registers can be used to modify the default settings. Detailed description of memory-mapped registers and configurations are available in the *F035 Flash Module* section of the *TMS570LS20216 Technical Reference Manual* (SPNU489).

The following features can be configured in the application software:

- Flash pipeline mode enable/disable with the Flash Option Control Register (FRDCNTL)
- Address and data wait states with the Flash Option Control Register (FRDCNTL)
- Flash bank modes with the Flash Bank Fallback Power Register (FBFALLBACK)
- Flash parity or ECC enable with the Flash Error Detection and Correction Control Register 1 (FEDACCTRL1)

The device-specific data sheet should be referenced for all the available Flash module configurations.

The RAM wrapper supports a few configurations of RAM memory. The RAM wrapper and system registers can be used to modify the default settings.

The following features can be configured in the application software:

- RAM data and address wait states with the RAM Control Register (RAMGCR)

The system module in conjunction with GCM module generates the clocks for cores, bus masters, and peripherals. A detailed description of clock controls is available in the *Architecture Overview* section in the *TMS570LS20216 Technical Reference Manual* (SPNU489). After reset, the device is running on OSCIN (primary device crystal), which is clock source 0.

The following setup can be used to configure the PLLx and device clock sources.

- Setup PLL's of the device with the PLL Controlx Registers (PLLCTRL1, PLLCTRL2, or PLLCTRL3)
- Wait for the clock sources to be locked with the Clock Source Valid Status Register (CSVSTAT)
- Enable the device clock source with the GCLK, HCLK, VCLK, and VCLK2 Source Register (GHVSRC). This register defines the clock source for GCLK, HCLK, VCLK, and VCLK2 domains
- Configure the clock sources for clock domains such as the VCLKA1, VCLKA2, RTI1CLK, and RTI2CLK with VCLKASRC and RCLKSRC registers

The device-specific data sheet should be referenced for all the available clock sources for configuration.

The following procedure should be used to setup the peripheral controls using the system and PCR modules:

1. Disable peripherals after reset.
2. Power-up the peripherals with the Peripheral Power-Down Clearx Registers (PSPWRDWNCLRx).
3. Configure the VCLK and VCLK2 clock ratio with the Clock Control Register (CLKCNTL). By default, VCLK and VCLK2 are divided by 2.
4. Enable the peripherals with the PENA bit of the Clock Control Register (CLKCNTL).

The device-specific data sheet should be referenced for all the available peripherals, peripherals selects, and clock domains.

2 References

- *TMS570LS20216 Technical Reference Manual* (SPNU489)
- *Cortex-R4 and Cortex-R4F Technical Reference Manual* available at http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0363e/ch01s10s03.html
- CoreSight and Trace for Cortex-R Series Processors http://www.arm.com/products/system-ip/debug-trace/coresight-for-cortex-r.php
- Cortex-R4 Processor http://www.arm.com/products/processors/cortex-r/cortex-r4.php

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