

32-kbit/s ADPCM with the TMS32010

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Abstract

This report discusses 32-kbit/s Adaptive Differential Pulse Code Modulation (ADPCM) transcoders. A half-duplex ADPCM transcoder, which complies with the CCITT recommendation (G.721), can be achieved with a single TMS32010. If the transcoder is used only for private lines, a full duplex non-CCITT ADPCM transcoder is more cost-effective and can be designed with a single TMS32010 processor. Both the CCITT and non-CCITT algorithms and code implementations are covered in the report.



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INTRODUCTION

Digital voice communication is typically transmitted in a 64-kbit/s PCM bit stream. Voice and data communications demand increasing capacities for signal transmission without significant degradation in the quality of the transmitted signal. One of the recommended solutions for accomplishing this task is that of Adaptive Differential Pulse Code Modulation (ADPCM). This solution has been reviewed by CCITT (International Telegraph and Telephone Consultative Committee), and a specific standard* has been recommended. Two solutions, a full-duplex solution and a half-duplex solution, are discussed in this application report. Both follow the model recommended by CCITT for 32-kbit/s ADPCM, although only the half-duplex solution provides a bit-for-bit compatible data stream as required by the recommendation. At 32 kbit/s, the ADPCM solution provides double the channel capacity of the current 64-kbit/s PCM technique. Each solution has been totally incorporated in the internal memory space of the Texas Instruments TMS32010 microprocessor.

This application report presents a brief review of the basic principles of PCM and ADPCM. Hardware requirements, software logic flow, and key features of the TMS32010 microprocessor for the implementation of ADPCM are also given. Source code is provided for the implementation and creation of an ADPCM transmission channel.

DIGITIZATION

Over the past 20 years, the telecommunications industry has changed from totally analog circuits to networks which integrate both analog and digital circuits. Digital signal encoding has the advantages of greater noise immunity, efficient regeneration, easy and effective encryption, and uniformity in transmitting voice and data signals. Increased bandwidth is required to transmit digital signals while maintaining a given analog signal quality at the receiver.

Voice store and forward systems have been changing from totally analog storage media, such as audio tape, to digitized storage which allows random access of stored data, but with the tradeoff of increased storage media requirements.

Signal quality begins with the digitization of the original analog signal. The process of digitization and coding introduces a distortion associated with the quantization of the digitized signal, as shown in Figure 1. This signal distortion or noise is different from the channel noise normally associated with a transmitted signal. After a signal

has been digitized, the signal is much less susceptible to channel noise since the signal can be regenerated as well as amplified along the way, thus reducing the possibility of being corrupted by the transmission system. The overall quality of digital transmission is then limited by the digitization process in an error-free transmission system.

Figures 2 and 3 show general representations of a digital communication channel. The actual transmission (and storage of a digital waveform) uses an analog channel. The outside points of the communications channel are the transmitter and receiver, as shown in Figure 2. These are commonly combined in a single device known as a combo-CODEC (CODing and DECoding device). The codec supplies, on the coding or transmitting side, the necessary filtering to bandlimit the analog signal and avoid signal alias and A/D conversion. On the decoding or receiving side, the codec performs a D/A conversion and then interpolates or smooths the resultant signal.

Figure 3 shows the digitized signal modulated for transmission in the network and then demodulated at the receiving end to retrieve the transmitted digital signal.

PCM

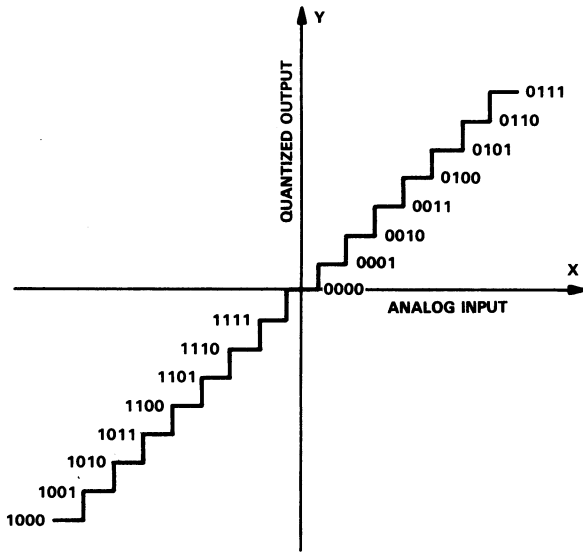
Digitization and coding of the analog signal at the transmitter can be performed in several ways. The complexity of the chosen method is related to availability of encoder memory and to the resultant delay in the encoding process.

When digital signal transmission is implemented, memory and the resultant delay dictate that a simple scheme, such as Pulse Code Modulation (PCM), be implemented. PCM codes each sampled analog value of the input waveform to a unique or discrete value. The digital quantization introduces distortion into the signal waveform, as shown in Figure 1.

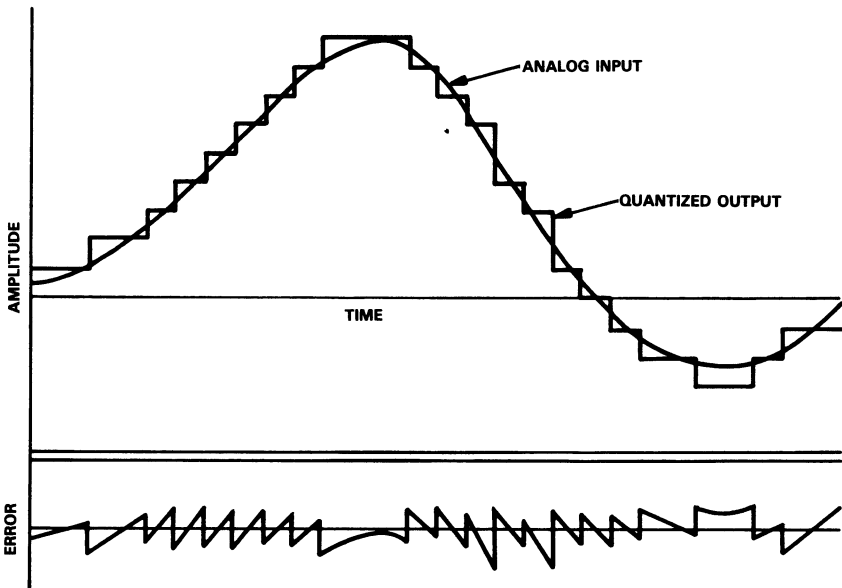
A nonuniform quantization scheme may be used to COMPAND (COMpress and exPAND) the signal in the waveform coding and decoding blocks in the system, generating log-PCM. By using larger quantization steps for large amplitude signals and smaller steps for small amplitude signals, efficient use is made of the data bits for digital transmission while maintaining specific signal-to-quantization noise thresholds. With the two current methods of COMPANDING (A-law and μ -law), the signal quality of a 13-bit digitized signal is maintained while transmitting only 8 bits per sample.

While quantizers remove the irrelevancy in a signal, coders remove the redundancy. In PCM encoding, each sample of the input waveform is independent of all previous samples; no encoder memory is required.

*Recommendation G.721, 32 kbit/s Adaptive Differential Pulse Code Modulation, CCITT, 1984.



(a) SIGNAL QUANTIZATION



(b) SIGNAL QUANTIZATION ERROR

Figure 1. Quantization Errors in a Digitized Signal

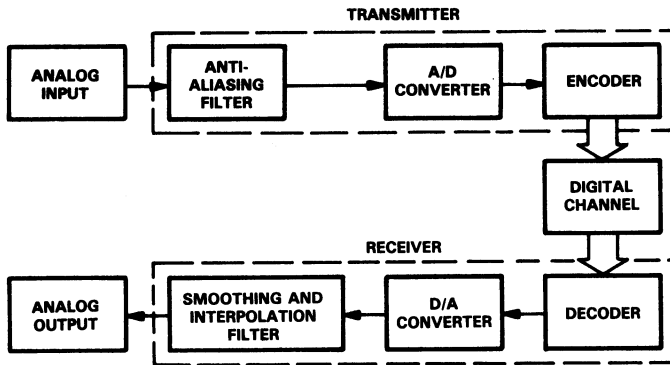


Figure 2. Digital Communication of Waveforms



Figure 3. Digital Channel

ADPCM

Analysis of speech waveforms shows a high sample-to-sample correlation. By taking advantage of this property in speech signals, more efficient coding techniques have been designed to further reduce the transmission bit rate while preserving the overall signal quality.

APCM

Adaptive PCM (APCM) is a method that may be applied to both uniform and nonuniform quantizers. It adapts the stepsize of the coder as the signal changes. This accommodates amplitude variations in a speech signal between one speaker and the next, or even between voiced and unvoiced segments of a continuous signal. The adaptation

may be instantaneous, taking place every few samples. Alternatively, it may occur over a longer period of time, taking advantage of more slowly varying features. This is known as syllabic adaptation.

The basic concept for an adaptive feedback system, APCM, is shown in Figure 4. An input signal, $s(k)$, in the transmitter is quantized and coded to an output, $I(k)$. This output is also processed by stepsize adaptation logic to create a signal, $q(k)$, that adapts the stepsize in the quantizer. Correspondingly, in the receiver, the received signal, $I(k)$, is processed by an inverse quantizer (i.e., decoded), producing the reconstructed signal, $s_r(k)$. Like the transmitter, the quantized signal, $I(k)$, is processed by adaptation logic to create a stepsize control signal, $q(k)$, for the inverse quantizer.

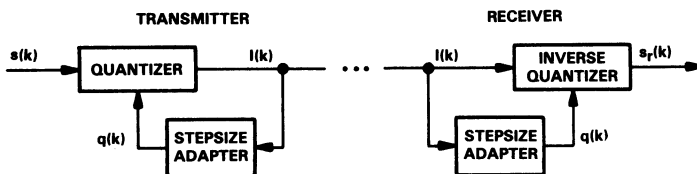


Figure 4. APCM Block Diagram

DPCM

The method of using the sample-to-sample redundancies in the signal is known as differential PCM (DPCM). The overall level of high correlation on a sample-by-sample basis indicates that the difference between adjacent samples produces a waveform with a much lower dynamic range. Correspondingly, an even lower variance can be expected between samples in the difference signal. A signal with a smaller dynamic range may be quantized to a specific signal-to-noise ratio with fewer bits.

A differential PCM system, DPCM, is shown in Figure 5. In Figure 5, the signal difference, $d(k)$, is determined using a signal estimate, $s_e(k)$, rather than the actual previous sample. By using a signal estimate, $s_e(k)$, the transmitter uses the same information available to the receiver. Each successive coding actually compensates for the quantization error in the previous coding. In this way, the reconstructed signal, $s_r(k)$, can be prevented from drifting from the input signal, $s(k)$, as a result of an accumulation of quantization errors. The reconstructed signal, $s_r(k)$, is formed by adding the quantized difference signal, $d_q(k)$, to the previous signal estimate, $s_e(k)$. The sum is the input to predictor logic which determines the next signal estimate. A decoding process is used in both the transmitter and receiver to determine the quantized difference signal, $d_q(k)$, from the transmitted signal, $I(k)$.

ADPCM

ADPCM combines the features of both the APCM and DPCM systems. Figure 6 shows the basic blocks combining adaptation and differencing features in an ADPCM system.

Both quantizer adaptation and signal differencing require the storage (in memory) of one or more samples in both the transmitter and receiver. Furthermore, the transmitter must use some method to ensure that the receiver is operating synchronously. This is accomplished by using only the transmitted signal, $I(k)$, to determine stepsize adaptation in the quantizer and inverse quantizer and to predict the next signal estimate. In this way, the blocks in the receiver can be identical to those in the transmitter. Additionally, the specific adaptation techniques are designed to be convergent and thereby help provide quick recovery following transmission errors.

The ADPCM system, as used in digital telephony, is not an original signal coding system, but is actually a transcoder, converting between log-PCM and ADPCM codes. Currently there are a large number of systems using log-PCM for transmission. The ADPCM system incorporates both an adaptive quantizer and an adaptive predictor. The adaptive quantizer contains speed-control and scale-factor adaptation. A measure of the rate-of-change of the difference signal provides a means of determining the speed control. The scale factor adjustments to the difference signal adapt the fit of the quantization levels to minimize the signal-to-noise ratio. With speed control, the system can take advantage of both the instantaneous and syllabic adaptation rates, thereby adapting better to both speech and data signals. In the adaptive predictor, the prediction filter coefficients are updated by a gradient algorithm. Predictor adaptation improves the performance of the predictor for nonstationary signals (e.g., speech).

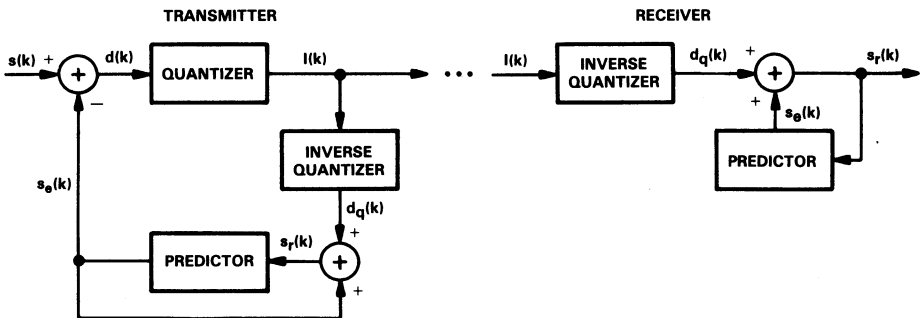


Figure 5. DPCM Block Diagram

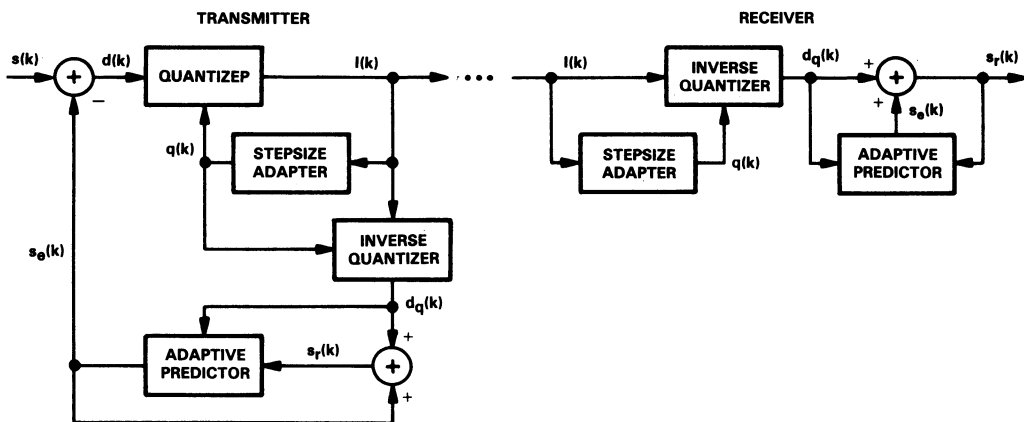


Figure 6. ADPCM Block Diagram

THE ADPCM ALGORITHM

The ADPCM algorithm has a receiver imbedded in the transmitter. This is important since, if the signal feedback used to determine the signal estimate, $s_e(k)$, and consequently the quantized difference signal, $d_q(k)$, is the same as in the decoder, then the compensation for quantization errors can be made with subsequent difference samples. Since the decoder is actually imbedded in the encoder, each of the common blocks for transmitting and receiving is discussed in the following paragraphs.

Figures 7 and 8 show block diagrams of an ADPCM transmitter and receiver as specified by CCITT.

Encoder

The function of the encoder or transmitter, shown in Figure 7, is to receive a 64-kbit/s log-PCM signal and transcode it to a 32-kbit/s ADPCM signal. This is accomplished by converting the log-PCM signal, $s(k)$, to a linear signal, $s_l(k)$, from which an estimate, $s_e(k)$, of the signal is subtracted to obtain a difference signal, $d(k)$. The next step is to adaptively quantize this difference signal, $d(k)$, by first taking the log (base 2), then normalizing by the quantization scale factor, $y(k)$, and finally coding the result, $I(k)$. A more uniform signal-to-noise ratio can be achieved by coding the log of the signal rather than the linear representation. The normalization provides the adaptation to the quantization and is based on past coded samples. Adaptation is controlled bimodally, being comprised of a fast adaptation factor for signals with large amplitude fluctuations (i.e., speech) and a slow adaptation factor for signals which vary more slowly (i.e., data). A speed-control factor, $a_1(k)$, weights the fast and the slow adaptation factors to form a single quantization scale factor, $y(k)$.

The inverse adaptive quantizer uses the same signal, $I(k)$, that has been transmitted to reconstruct a quantized version of the difference, $d_q(k)$, and the same adaptive quantization characteristics as the adaptive quantizer section.

The quantized difference signal, $d_q(k)$, is input to an adaptive predictor which uses this input to compute a signal estimate, $s_e(k)$. The signal estimate, $s_e(k)$, is combined with the difference signal, $d_q(k)$, to determine a reconstructed signal, $s_r(k)$, which is the output in the decoder. This output is then subtracted from the next input sample to complete the feedback loop.

The adaptive predictor makes use of both an all-pole filter and an all-zero filter. The all-pole filter is a second-order filter with constrained adaptive coefficient values designed to match the slowly varying aspects of the speech signal. Since an all-pole predictor is particularly sensitive to errors, the predictor makes use of a sixth-order all-zero filter to offer signal stability even with transmission errors.

Decoder

The function of the decoder or receiver, shown in Figure 8, is to receive a 32-kbit/s ADPCM signal and transcode it to a 64-kbit/s log-PCM signal. To accomplish this, the decoder utilizes many of the elements used by the encoder. The received data, $I(k)$, is processed by an inverse adaptive quantizer, identical to the one in the corresponding encoder, to determine a quantized difference signal, $d_q(k)$. By filtering the difference signal, $d_q(k)$, through the adaptive predictor together with the previously reconstructed signal, $s_r(k)$, a signal estimate, $s_e(k)$, is obtained. The signal estimate, $s_e(k)$, is added to the difference signal, $d_q(k)$, to compute the reconstructed signal, $s_r(k)$. The reconstructed signal, $s_r(k)$, is converted from a linear-PCM to a log-PCM signal, $s_p(k)$, which is then output following a synchronous

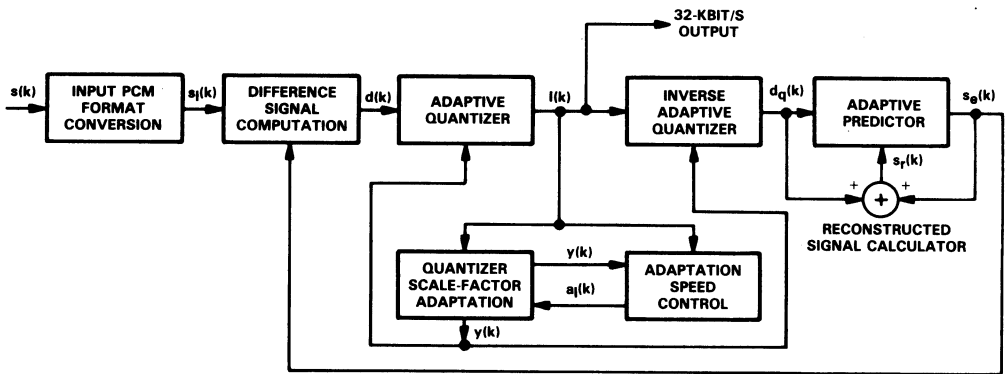


Figure 7. ADPCM Encoder Block Diagram
(Diagram taken from CCITT Recommendation G.721)

coding adjustment. The coding adjustment limits the errors in tandem codings of a signal.

Note that the algorithm design achieves a convergence of the states of the encoder and decoder in spite of transmission errors. This convergence is a part of each of the adaptation computations and is demonstrated equationally in the following sections. The convergence is brought about by the inclusion of $(1-2^{-N})$ terms which provide a finiteness to the memory of the adaptation parameters.

Adaptive Quantization

Adaptive quantization, a multistage process, is used to determine the quantization scale factor and the speed control that controls the rate at which the scale factor is adapted. Quantization is actually a four-bit quantization (a sign bit plus three-bit magnitude), since a four-bit signal is the transmitted output of the ADPCM transcoder. The adaptive quantizer block can be noted in Figure 7.

The difference signal, $d(k)$, an input to the quantization process, is calculated by subtracting the signal estimate, $s_e(k)$, from the linear-PCM signal, $s_1(k)$.

$$d(k) = s_1(k) - s_e(k) \quad (1)$$

This difference signal is normalized by taking the log (base 2) and subtracting from it the quantizer scale factor, $y(k)$.

$$|I(k)| - \log_2 |d(k)| - y(k) \quad (2)$$

Table 1 is used to provide the magnitude of the quantization result, $|I(k)|$, from this normalized input. The

sign bit of the ADPCM output value, $I(k)$, is the sign of the difference signal, $d(k)$.

The quantizer scale factor, $y(k)$, is comprised of two parts, and therefore bimodal in nature. The two parts, $y_l(k)$ and $y_u(k)$, are weighted by the speed-control factor, $a_1(k)$. For speech signals, $a_1(k)$ will tend toward a value of one; for voiceband data, $a_1(k)$ will tend toward zero. Refer to both Figures 7 and 8 for the inclusion of the quantizer scale factor and speed-control factor adaptation blocks.

$$y(k) = a_1(k)y_u(k-1) + [1 - a_1(k)] y_l(k-1) \quad (3)$$

where $0 \leq a_1(k) \leq 1$

One of the factors, $y_u(k)$, is considered to be unlocked, since it can adapt quickly to rapidly changing signals (e.g., speech) and has a relatively short-term memory. This factor, $y_u(k)$, is recursively determined from the quantizer factor, $y(k)$, and the discrete function, $W(I)$.

$$y_u(k) = [1 - 2^{-5}] y(k) + 2^{-5}W[I(k)] \quad (4)$$

where $1.06 \leq y_u(k) \leq 10.00$

The factor, $W(I)$, found in Table 2, is a function of I which causes $y_u(k)$ to adapt by larger steps for larger values of I . This gives $y_u(k)$ the freedom to track a signal almost instantaneously. Since $y(k)$ is in the logarithmic domain, $W(I)$ is effectively a multiplier of the scale factor.

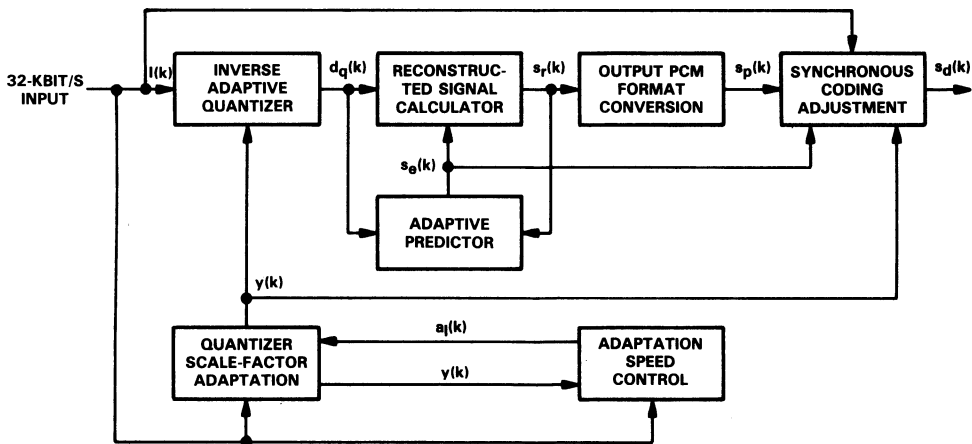


Figure 8. ADPCM Decoder Block Diagram
(Diagram taken from CCITT Recommendation G.721)

Table 1. I/O Characteristics of the Normalized Quantizer

Normalized Quantizer Input Range $\log_2[d(k)] - y(k)$	$ I(k) $	Normalized Quantizer Output $\log_2[d_q(k)] - y(k)$
[3.16, +∞)	7	3.34
[2.78, 3.16)	6	2.95
[2.42, 2.78)	5	2.59
[2.04, 2.42)	4	2.23
[1.58, 2.04)	3	1.81
[0.96, 1.58)	2	1.29
[-0.05, 0.96)	1	0.53
(-∞, -0.05)	0	-1.05

The other factor, $y_1(k)$, adapts more slowly and tracks signals which change slowly (e.g., voiceband data). This factor includes a lowpass filtering of the unlocked factor, $y_u(k)$. By including $y_u(k)$ in the manner shown, $y_1(k)$ is implicitly limited to the same range of values as the explicit limit placed on $y_u(k)$. Furthermore, the unity limit of $a_1(k)$ provides the same limit implicitly for $y(k)$ as for $y_1(k)$ and $y_u(k)$.

$$y_1(k) = [1 - 2^{-6}] y_1(k-1) + 2^{-6} y_u(k) \quad (5)$$

A speed-control factor, $a_1(k)$, adjusts the relative weighting of these two scale factors by making use of the short- and long-term averages, $d_{ms}(k)$ and $d_{ml}(k)$, respectively, of the coded output to determine how rapidly the signal is changing. The combined scale factor, $y(k)$, cannot be larger than either the unlocked, $y_u(k)$, or locked $y_1(k)$, terms. Therefore, $a_1(k)$ is limited to one even if the predicted speed control, $a_p(k)$, is larger than one.

$$a_1(k) = \begin{cases} 1 & , \text{if } a_p(k-1) > 1 \\ a_p(k-1) & , \text{if } a_p(k-1) \leq 1 \end{cases} \quad (6)$$

Note that $a_p(k)$ is implicitly limited to a maximum value of 2, while the speed-control factor used to mix the two scale factors is capped at a value of 1. In determining $a_p(k)$, an additional term of 1/8 is added each time if the difference in the short- and long-term averages becomes too large (i.e., $|d_{ms}(k) - d_{ml}(k)| \geq 2^{-3} d_{ml}(k)$) or if there is an idle channel (i.e., $y(k) < 3$). Where neither of these conditions exist, a uniform, slowly varying signal can be assumed, such as occurs in data transmission.

Table 2. Scale-Factor Multipliers

$ I $	7	6	5	4	3	2	1	0
$W(I)$	69.25	21.25	11.50	6.12	3.12	1.69	0.25	-0.75

$$a_p(k) = \begin{cases} [1 - 2^{-4}] a_p(k-1) + 2^{-3}, & \text{if } |d_{ms}(k) - d_{ml}(k)| \geq 2^{-3} d_{ml}(k) \\ [1 - 2^{-4}] a_p(k-1) + 2^{-3}, & \text{if } y(k) < 3 \\ [1 - 2^{-4}] a_p(k-1), & \text{otherwise} \end{cases} \quad (7)$$

The short-, $d_{ms}(k)$, and long-term, $d_{ml}(k)$, averages of the transmitted ADPCM signal, $I(k)$, are actually determined by averaging a weighted function, $F(l)$, of the transmitted I , shown in Table 3.

$$d_{ms}(k) = [1 - 2^{-5}] d_{ms}(k-1) + 2^{-5} F[I(k)] \quad (8)$$

$$d_{ml}(k) = [1 - 2^{-7}] d_{ml}(k-1) + 2^{-7} F[I(k)] \quad (9)$$

The scale-factor and speed-control adaptations are a part of both the encoder and decoder logic. The adaptive quantization block has been specifically included in Figure 7, showing the encoder. For the decoder, the adaptive quantizer is included as part of the synchronization block to aid in the reduction of errors in tandem codings.

Table 3. Rate-of-Change Weighting Function

l	7	6	5	4	3	2	1	0
F(l)	7	3	1	1	1	0	0	0

Inverse Adaptive Quantization

Inverse adaptive quantization is a process in which the four-bit ADPCM signal, $I(k)$, is used to determine the normalized log of the difference signal from Table 1. The result is actually a quantized version of the difference signal, $d_q(k)$, determined by adding the scale factor, $y(k)$, to the value specified by Table 1 and calculating, the inverse log (base 2) of this sum.

$$d_q(k) = \log_2^{-1} [\{\log_2 |d_q(k)| - y(k)\} + y(k)] \quad (10)$$

For both the encoder and decoder, this quantized difference signal is the input to the reconstruction signal calculator and the adaptive predictor, as shown in Figures 7 and 8.

Adaptive Prediction

The adaptive predictive filter is a two-pole, six-zero filter used to determine the signal estimate. The combination of both poles and zeroes allows the filter to model more effectively any general input signal. The sixth-order all-zero section helps to stabilize the filter and prevent it from drifting into oscillation. For both the poles and the zeroes, the coefficients, $a_i(k)$ and $b_i(k)$, respectively, are adapted. This adaptation is based upon a gradient algorithm to further adjust the filter model to the input signal. Figures 9 and 10 show the sixth-order and second-order filters, respectively.

The signal estimate, $s_e(k)$, represents the sum of the all-pole filter and the all-zero filter. Since the sum of the all-zero filter is used to aid the determination of the pole coefficients, it is also extracted as a separate sum, $s_{ez}(k)$. The reconstructed signal, the output in the receiver, is the sum determined by the quantized difference signal $d_q(k)$, and the signal estimate, $s_e(k)$.

$$s_e(k) = \sum_{i=1}^2 a_i(k-1) s_r(k-i) + s_{ez}(k) \quad (11)$$

$$s_{ez}(k) = \sum_{i=1}^6 b_i(k-1) d_q(k-i) \quad (12)$$

$$s_r(k-i) = s_e(k-i) + d_q(k-i) \quad (13)$$

The adaptation of the pole coefficients, $a_i(k)$, is shown in the equations below. The gradient function is determined from a signal, $p(k)$, that is equivalent to the reconstructed signal minus the contribution of the pole filter output. Stability of the filter is further provided by explicitly limiting the coefficients.

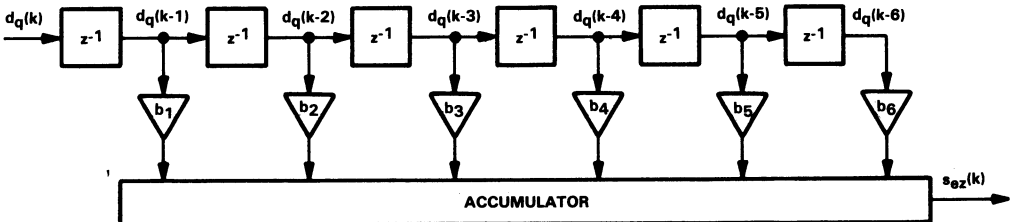


Figure 9. Sixth-Order All-Zero (FIR) Filter

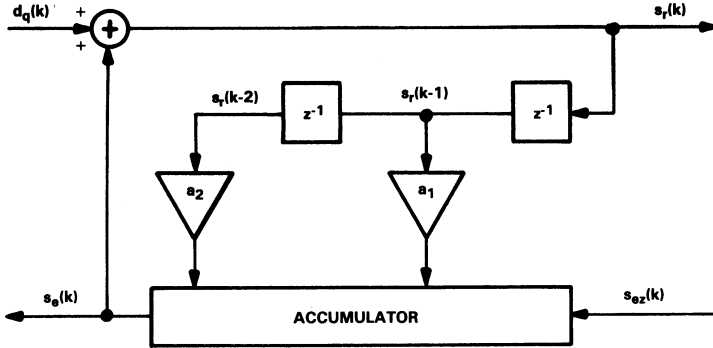


Figure 10. Second-Order IIR Filter

$$a_1(k) = [1 - 2^{-8}] a_1(k-1) + 3 \cdot 2^{-8} \text{sgn}[p(k)] \text{sgn}[p(k-1)] \quad (14)$$

$$\text{where } |a_1(k)| \leq 1 - 2^{-4} - a_2(k)$$

$$a_2(k) = [1 - 2^{-7}] a_2(k-1) + 2^{-7} \{\text{sgn}[p(k)] \text{sgn}[p(k-2)] - f[a_1(k-1)] \text{sgn}[p(k)] \text{sgn}[p(k-1)]\} \quad (15)$$

$$\text{where } |a_2(k)| \leq 0.75$$

$$p(k) = d_q(k) + s_{ez}(k) \quad (16)$$

$$f(a_1) = \begin{cases} 4a_1 & , \text{ if } |a_1| \leq 1/2 \\ 2\text{sgn}(a_1), & \text{ if } |a_1| > 1/2 \end{cases} \quad (17)$$

$$\text{where } \text{sgn}(0) = +1$$

For the coefficients, $b_i(k)$, of the sixth-order all-zero filter, the adaptation procedure is similar, but the limit is implicit in the equations to a maximum of ± 2 . The gradient function, in this case, is determined by the current difference signal, $d_q(k)$, and corresponding difference signal, $d_q(k-i)$, at the specific filter tap.

$$b_i(k) = [1 - 2^{-8}] b_i(k-1) + 2^{-7} \text{sgn}[d_q(k)] \text{sgn}[d_q(k-i)] \quad (18)$$

$$\text{where } i = 1, 2, \dots, 6 \text{ and } -2 \leq b_i(k) \leq +2$$

Signal Conversion

Signal conversion consists of the conversion from an 8-bit log-PCM representation of a signal to a 13-bit linear PCM representation (note Figure 7), or the reverse (note Figure 8). Signal conversions of this type are described in the application report on COMPANDING ROUTINES FOR THE TMS32010. In the encoder, the log-PCM signal, $s(k)$, is expanded to create the linear-PCM value, $s_l(k)$. The decoder, on the other hand, compresses the reconstructed signal, $s_r(k)$, to create the log-PCM signal, $s_p(k)$.

Reconstructed Signal Synchronization

To avoid a cumulative distortion in synchronous tandem codings, an adjustment to the reconstructed signal is specified. The adjustment block, shown in Figure 8, estimates the quantization of the encoder by determining a difference signal and executing the adaptive quantization logic. The quantization result is an estimate of the received value of $I(k)$.

The difference signal, $d_x(k)$, is determined by subtracting the signal estimate, $s_e(k)$, from the linear-PCM signal, $s_{lx}(k)$, which is itself determined by expanding the log-PCM signal, $s_p(k)$.

$$d_x(k) = s_{lx}(k) - s_e(k) \quad (19)$$

The adaptive quantization process produces the estimate of the ADPCM code value, $I_d(k)$. If the estimate implies a difference signal that is lower than the received interval boundary, the log-PCM code is changed to the next most positive value. An estimate implying a difference signal

larger than the received interval boundary requires the log-PCM code to be changed to the next most negative value; otherwise, the log-PCM value is left unchanged. The adjusted log-PCM value is denoted as $s_d(k)$ in the following equation to differentiate it from the input value, $s_p(k)$.

$$s_d(k) = \begin{cases} s_p^+(k), & d_x(k) < \text{lower interval boundary} \\ s_p^-(k), & d_x(k) \geq \text{upper interval boundary} \\ s_p(k), & \text{otherwise} \end{cases} \quad (20)$$

where

$s_d(k)$ = output PCM of the decoder

$s_p^+(k)$ = next more positive PCM level (if $s_p(k)$ is the most positive level, then $s_p^+(k) = s_p(k)$)

$s_p^-(k)$ = next more negative PCM level (if $s_p(k)$ is the most negative level, then $s_p^-(k) = s_p(k)$)

FULL-DUPLEX IMPLEMENTATION OF ADPCM ON A TMS32010

The specific implementation of ADPCM presented here involves the use of a single TMS320M10 to accomplish a

full-duplex transcoder. The TMS320M10 is a masked ROM, microcomputer version of the TMS32010, which requires no external program memories. A full-duplex transcoder provides transmission in both directions simultaneously. Such a transcoder is depicted in Figure 11. A complete system diagram of a full-duplex communications channel is shown in Figure 12. In comparison to current systems that modulate a 64-kbit/s A-law or μ -law PCM signal on a carrier for transmission, the described system transcodes the 64-kbit/s code to a 32-kbit/s code. This 32-kbit/s code, which requires correspondingly less bandwidth, is modulated on the carrier for transmission.

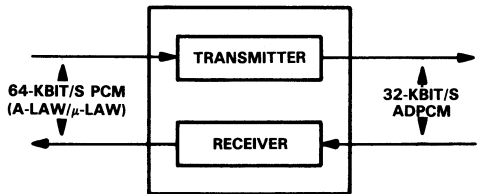


Figure 11. Full-Duplex ADPCM Transcoder

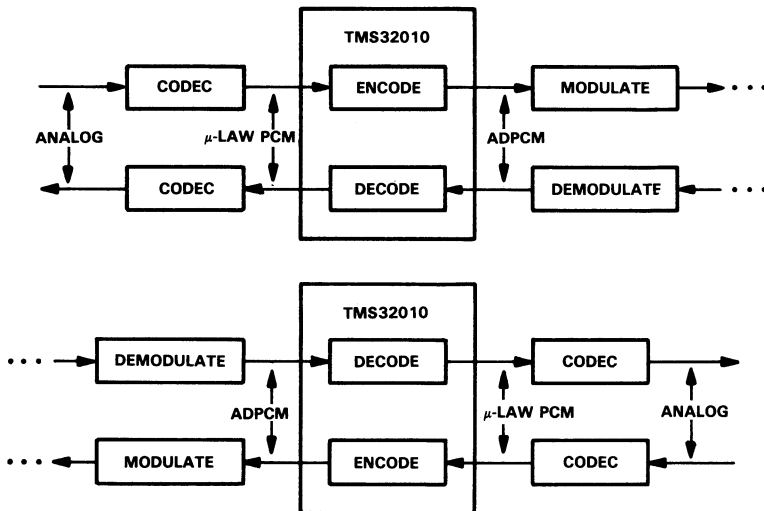


Figure 12. Full-Duplex Telecommunications Channel

Hardware Logic and I/O

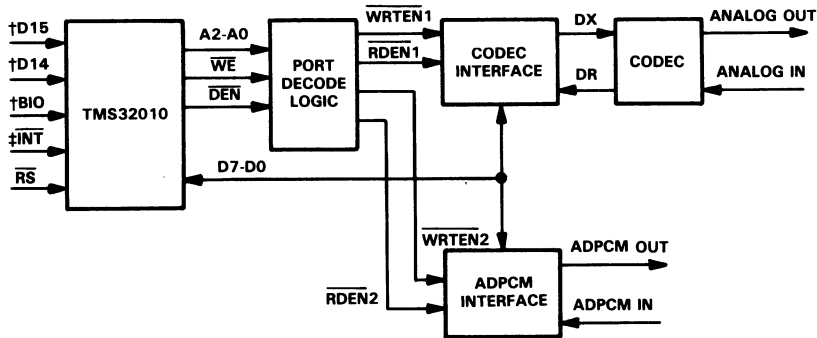
The hardware required to implement the ADPCM system consists of an addition to an existing circuit. As shown in Figure 13, the TMS32010 addresses the external I/O blocks through its port addressing structure. The lower three address lines, A2-A0, form a port address that can be decoded by port decode logic to provide specific enable lines (e.g., $\overline{\text{WRTE}}\text{N1}$ and $\overline{\text{RDEN}}\text{1}$) to the various peripheral blocks. The TMS32010 reads and writes the 64-kbit/s data through the codec interface eight bits at a time. The sampling frequency is 8 kHz. For this full-duplex implementation, one sample is written and one sample is read every 125 μs .

Figure 13 also shows the serial interface to the codec that provides the μ -law companded PCM data, although this is not part of the transcoding system itself. The log-PCM signal may already be available (e.g., in existing digital telecom networks) and, as such, may be interfaced to the TMS32010 either directly as parallel data or serially through conversion logic. Parallel codecs are also becoming available to reduce the hardware logic and interface required for those systems which do not already include a codec. The TMS32010 is available at crystal and clock input rates of 20.5 MHz which may be divided down to provide the codec timing and further reduce the logic requirement.

At the other end of the transcoder function, the TMS32010 reads and writes the 32-kbit/s ADPCM data through the ADPCM interface four bits at a time for each 125- μs period. This interface provides four-bit parallel data which may be serialized, if required, for transmission or storage.

Software Logic and Flow

Tables 4 and 5 list the various blocks in the algorithm, directly relating them to Figures 7 and 8 by the signal names given in the description and function. The blocks are listed in the order in which they are executed. Also listed is processor demand or loading which consists of the amount of program memory used to implement the given function and the number of instruction cycles executed in worst case. There are more blocks in the table than are shown in the figures (e.g., the algorithm uses the adaptive predictor at one point to produce the signal estimate, and later returns to update or adapt the predictor coefficients). Each block has been implemented using the equations given in previous sections concerning the ADPCM algorithm. For convenience, the equations implemented in each block are listed in the description section for the block. A more detailed description of the TMS32010 implementation is given in the next section.



† Half-duplex, CCITT bit-compatible, version only

‡ Full-duplex version only

Figure 13. System Interface of a TMS32010 ADPCM Transcoder

Table 4. Full-Duplex Transmitter

Order	Function	Description	CPU Clocks	Program Memory (Words)
1.	INPUT PCM	Read an 8 bit μ -law PCM sample $[s(k)]$ and linearize it to a 12-bit sample $[s_l(k)]$.	7	0004
2.	COMPUTE SIGNAL ESTIMATE	Calculate the signal estimate $[s_g(k)]$ from the previous data samples $[d_q(k)]$ and reconstructed samples $[s_r(k)]$ through the predictor filter. (12),(11)	30	001E
3.	COMPUTE ADAPTIVE QUANTIZER	Calculate speed control $[a_l(k)]$ and quantizer scale factor $[y(k)]$ from past quantizer output $[l(k)]$. (6),(3)	33	0021
4.	COMPUTE DIFFERENCE SIGNAL	Calculate the difference signal $[d(k)]$ from the current sample $[s_l(k)]$ and signal estimate $[s_g(k)]$. (1)	3	0003
5.	COMPUTE QUANTIZED OUTPUT	Calculate the log of the difference signal $[d(k)]$ and adaptively quantize the result to yield the ADPCM output $[l(k)]$. (2)	46	00AD
6.	OUTPUT ADPCM	Write the ADPCM output $[l(k)]$.	2	0001
7.	COMPUTE RECON-STRUCTED SIGNAL	Calculate the inverse of the adaptively quantized signal $[d_q(k)]$ and the reconstructed signal difference $[s_r(k)]$. (10),(13)	43	0027
8.	COMPUTE SCALE FACTOR	Calculate the updates for the scale-factor adaptation. (4),(5)	46	002F
9.	COMPUTE SPEED CONTROL	Calculate the update for the speed-control adaptation. (8),(9),(7)	30	001B
10.	COMPUTE PREDICTOR ADAPTATION	Calculate the updates for the adaptive predictor filter coefficients. (18),(16),(17),(14),(15)	102	006B

Table 5. Full-Duplex Receiver

Order	Function	Description	CPU Clocks	Program Memory (Words)
1.	INPUT ADPCM	Read the ADPCM input $\{l(k)\}$.	2	0001
2.	COMPUTE SIGNAL ESTIMATE	Calculate the signal estimate $\{s_g(k)\}$ from the previous data samples $\{d_q(k)\}$ and reconstructed samples $\{s_r(k)\}$ through the predictor filter. (12),(11)	30	001E
3.	COMPUTE ADAPTIVE QUANTIZER	Calculate speed control $\{a_l(k)\}$ and quantizer scale factor $\{y(k)\}$ from the past quantizer output $\{l(k)\}$. (6),(3)	33	0021
4.	COMPUTE QUANTIZED DIFFERENCE	Calculate the inverse of the adaptively quantized signal $\{d_q(k)\}$. (10)	47	002F
5.	COMPUTE SCALE FACTOR	Calculate the updates for the scale-factor adaptation. (4),(5)	48	002F
6.	COMPUTE SPEED CONTROL	Calculate the update for the speed-control adaptation. (8),(9),(7)	29	001B
7.	COMPUTE RECONSTRUCTED SIGNAL	Calculate the reconstructed signal $\{s_r(k)\}$. (13)	3	0003
8.	COMPUTE PREDICTOR ADAPTATION	Calculate the updates for the adaptive predictor filter coefficients. (18),(16),(17),(14),(15)	90	006B
9.	COMPUTE LOG-PCM	Convert the reconstructed linear-PCM signal $\{s_r(k)\}$ to a μ -law PCM signal $\{s_p(k)\}$.	39	0074
10.	OUTPUT PCM	Write the μ -law output $\{s_p(k)\}$.	2	0001
11.	WAIT	Spin until the next interrupt.	—	0006

Implementation and Advantages of TMS32010 Architecture

This implementation is only concerned with μ -law PCM, although A-law PCM may also be used. Additional information on log-PCM companding is found in an application report, COMPANDING ROUTINES FOR THE TMS32010. The implementation is simplified here so that the expansion is a simple table lookup which saves 21 instruction cycles over the algorithmic approach.

The processing of the signal through the predictor filter is similar to the processing discussed in the application report, IMPLEMENTATION OF FIR/IIR FILTERS WITH THE TMS32010. The filter used in this ADPCM algorithm is a combination of a second-order IIR filter and a sixth-order

all-zero or FIR filter. The filters are shown in Figures 9 and 10, respectively, with the system interaction shown in Figure 14.

Several manipulations of data format occur in adapting the predictor coefficients. In updating the coefficients of the all-zero filter (the B_i 's), the coefficients that are normally Q14 numbers are loaded with a shift allowing the calculations to be done in a Q29 representation. This greatly simplifies the subtraction of the leakage term and the prediction gain. The leakage term, which occurs here in the predictor coefficient adaptation and also in the speed-control and scale-factor adaptation, controls the rate of change of the parameter away from zero and towards the absolute maximum limits of the particular parameter. The prediction gain also uses

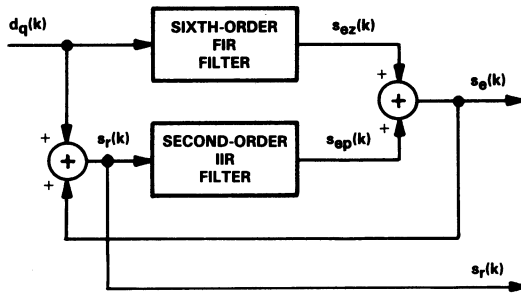


Figure 14. Predictor Filter

an approach whereby the signs are actually stored as a signed Q11 value. In this way, the product is a Q22 value of the correct sign and can be added to the B value, equivalent to a Q29 value times 2^{-7} . As with the filter process itself, the signs of the Dq values are propagated through each filter tap delay with the LTD instruction. An example for one of the B_i values is shown in Figure 15.

A similar process takes place in adapting the prediction coefficients (A_i's) in the second-order filter, although the fixed-point representation of the coefficients is Q26. The remaining requirement is to limit-check the A_i values.

The adaptive quantization section requires that the log (base 2) of the difference signal be taken, the result normalized, and the normalized value quantized. Taking the log (base 2) of a number is accomplished by using the approximation

$$\log_2(1 + x) = x \quad (21)$$

```

* ; *****
* ;
* ; COMPUTE COEFFICIENTS OF THE 6TH-ORDER PREDICTOR
* ;
* ; Bi(k) = [1 - 2** -8] * Bi(k-1)
* ;           + 2** -7 * SGN[DQ(k)] * SGN[DQ(k-i)]
* ;
* ; FOR i = 1 ... 6
* ; AND Bi IS IMPLICITLY LIMITED TO +/- 2
* ;
* ; NOTATION: Bn -- 16b TC (Q14)
* ;             SDQn -- +2048 IF DQn POSITIVE (Q11)
* ;                   -2048 IF DQn NEGATIVE (Q11)
* ; *****
* ;
GETB6 LT SDQ6 * (Q11)
      LAC B6,15 * (Q29)
      SUB B6,7 * B6 * 2** -8 (Q29)
      MPY SDQ * SGN(SDQ)*SGN(SDQ6)*2** -7 (Q29)
      LTD SDQ5 * (Q11)
      SACH B6,1 * (Q14)
      .
      .
      .

```

Figure 15. Predictor Coefficient Adaptation Code

Normalization of this log value is simply a subtraction of a scale factor which may be as large in fixed magnitude as the largest logarithmic value represented in Q7 notation. The result of the subtraction may be a negative value. Since the normalized result is to be quantized in a nonuniform manner and one of the quantization levels could contain both positive and negative values, the normalized result is scaled by adding a fixed value of 2048. Nonuniform quantization can be performed by a binary-type search technique. The normalization and quantization are included in the program shown in Figure 16.

Figure 16. Adaptive Quantization Code

```

        SACH TEMP1      * SAVE MANTISSA.
        LAC  TEMP1      * RELOAD FOR MANTISSA RECOMBINATION.
        B    GETMAN
        .
        .
        .
GETMAN AND M127          * MASK TO RETAIN ONLY SEVEN BITS.
        SAR 0,TEMP1      * MOVE EXPONENT TO MEMORY FROM ARO.
        ADD TEMP1,7      * ADD EXPONENT TO MANTISSA FOR LOG VALUE.

*;
*; SCALE BY SUBTRACTION
*;
SUBTB ADD ONE,11        * ADD AN OFFSET OF 2048.
      SUB TEMP3          * TEMP3 = Y(K) >> 2

*;
*; 4-BIT QUANTIZER
*;
*; QUANTIZATION TABLE FOR 32KB OUTPUT (OFFSET: 2048)
*;
ITAB1 EQU 2041
ITAB2 EQU 2171
ITAB3 EQU 2250
ITAB4 EQU 2309
ITAB5 EQU 2358
ITAB6 EQU 2404
ITAB7 EQU 2453
*;
QUAN SUB K2309          * ITAB4
      BGEZ CI4TO7
CI10TO3 ADD K138        * ITAB2      I = 0-3
      BGEZ CI12TO3
CI10TO1 ADD K130        * ITAB1      I = 0-1
      BGEZ IEQ1
IEQ0 LACK 0
      B GETIM
IEQ1 LACK 1
      B GETIM
CI12TO3 SUB K79         * ITAB3      I = 2-3
      BGEZ IEQ3
IEQ2 LACK 2
      B GETIM
IEQ3 LACK 3
      B GETIM
CI14TO7 SUB K95         * ITAB6      I = 4-7
      BGEZ CI16TO7
CI15TO6 ADD K46         * ITAB5      I = 5-6
      BGEZ IEQ5
IEQ4 LACK 4
      B GETIM
IEQ5 LACK 5
      B GETIM
CI16TO7 SUB K49         * ITAB6      I = 6-7
      BGEZ IEQ7

```

Figure 16. Adaptive Quantization Code (Continued)


```

IAQUAN LAC IM
      ADD INQTAB      * RECONSTRUCTION TABLE
      TBLR TEMP1      * READ NORMALIZED VALUE.

*;
*; ADD NORMALIZING SCALE FACTOR BACK IN
*;
ADDA LAC TEMP1
      ADD TEMP3      * Y >> 2
      AND M2047
      SACL TEMP2

*;
*; CONVERT THE LOG VALUE TO THE LINEAR DOMAIN
*;
*;
ALOG LAC TEMP2,9      * EXTRACT EXPONENT.
      SACH TEMP1      * SAVE EXPONENT VALUE.
      LACK 127
      AND TEMP2      * MASK FOR LOG MANTISSA ONLY.
      ADD ONE,7      * 1+x
      SACL TEMP2      * EXTRACT MANTISSA.
      LT TEMP2      * PREPARE TO SHIFT.
      LAC TEMP1
      ADD SHIFT      * LOOK UP MULTIPLIER.
      TBLR TEMP3
      MPY TEMP3      * MULTIPLY MANTISSA BY SHIFT FACTOR.
      PAC
      BLZ LEFTSF      * NEGATIVE VALUES CORRESPOND TO LEFT SHIFT.
      SACH DQ,1      * RIGHT SHIFT; SAVE MAGNITUDE OF DQ.
      B ADDSGN
LEFTSF ABS      * LEFT SHIFT; RESTORE MAGNITUDE.
      SACL DQ      * SAVE MAGNITUDE OF DQ.
ADDSGN LAC ONE,11      * ASSUME POSITIVE AND SAVE THE SIGN.
      SACL SDQ      * (SIGN IS Q11; REMEMBER FILTER.)
      LAC I      * CHECK SIGN OF SAMPLE.
      SUB ONE,3
      BLZ QSFA      * FINISHED FOR POSITIVE VALUES (I<8).
      ZAC
      SUB DQ      * COMPUTE TWO'S COMPLEMENT OF THE MAGNITUDE.
      SACL DQ      * SAVE NEGATIVE DQ VALUE.
      LAC MINUS,11      * SIGN IS Q11; REMEMBER FILTER.
      SACL SDQ      * SAVE SIGN.
      .
      .
      .

*;
*; INVERSE QUANTIZING TABLE
*;
IQTAB BSS 0
      DATA 65401
      DATA 68
      DATA 165
      DATA 232
      DATA 285
      DATA 332
      DATA 377
      DATA 428

```

Figure 17. Inverse Adaptive Quantization Code (Continued)


```

* ;
* ; SHIFT MULTIPLIER TABLE
* ;
SHIFT    BSS    0
          DATA 256
          DATA 512
          DATA 1024
          DATA 2048
          DATA 4096
          DATA 8192
          DATA 16384
          DATA -1
          DATA -2
          DATA -4
          DATA -8
          DATA -16
          DATA -32
          DATA -64
          DATA -128

```

Figure 17. Inverse Adaptive Quantization Code (Concluded)

The adaptation of the speed-control and the scale-factor parameters, used to adapt the stepsize in the adaptive quantizer and inverse adaptive quantizer, requires multiple uses of the technique of adjusting the fixed-point representation. The Q point is adjusted for convenience of the table constants which are part of the adaptation process and for saving the output value from the accumulator. Some limit-checking must also take place in calculating the unlocked-scale factor and the speed-control parameter.

In the calculation of the locked-scale factor and its inclusion in the mixing process for determining the overall scale factor used for stepsize quantization, the parameter is maintained with a greater resolution (19 bits of value plus its sign) than can be stored in a single memory. Calculations involving this parameter must then become two stage, both in terms of accumulations and in determining products. The code involving this parameter is listed in Figures 18 and 19.

```

* ;
* ; *****
* ;
* ; QUANTIZER SCALE FACTOR ADAPTATION
* ;
* ; INPUT: I : 32KB CODED SAMPLES
* ;
* ; OUTPUT: YU,YL : NEXT SAMPLE SCALE FACTOR
* ;
* ; NOTATION: Y -- 13b SM (Q9) POSITIVE VALUE ONLY
* ; YU -- 13b SM (Q9) POSITIVE VALUE ONLY
* ; YL -- 19b SM (Q15) POSITIVE VALUE ONLY
* ;
* ; *****
* ;
* ;
* ;
* ;
* ; UPDATE SLOW ADAPTATION SCALE FACTOR -- CONSTANT = 1/64
* ;
* ;  $YL(k) = (1-2^{-6}) * YL(k-1) + 2^{-6} * YU(k)$ 
* ;
FILTE LAC YLH,6 * SHIFT YL LEFT BY 6.
      SACL TEMP1 * TEMP1 = YLH *  $2^{**6}$ 
      LAC YLL,6
      SACL TEMP2
      SACH TEMP3 * TEMP3 ! TEMP2 = YLL *  $2^{**6}$ 
      LAC TEMP3 * SUPPRESS SIGN EXTENSION.
      AND M63
      SACL TEMP3
      ZALH TEMP1
      ADDH TEMP3
      ADDS TEMP2 * ACCUM = YL *  $2^{**6}$ 
      SUBH YLH
      SUBS YLL * ACCUM = YL *  $2^{**6}$  - YL
      ADD YU,6 * ACCUM = YL *  $2^{**6}$  - YL + YU
      SACL TEMP1
      SACH TEMP2 * RESULT = YL (SHIFTED LEFT BY 6)
      LAC TEMP1,10 * SHIFT RESULT RIGHT 6 --> q15
      SACH TEMP1
      LAC TEMP1
      AND M1023 * MASK SIGN EXTENSION.
      ADD TEMP2,10
      SACL YLL * SAVE YLL.
      SACH YLH
      LACK 7 * MASK UPPER 13 BITS.
      AND YLH
      SACL YLH * SAVE YLH.
* ;
* ;
* ;

```

Figure 18. Quantizer Scale-Factor Adaptation: Locked-Factor Calculation

```

* ;
* ;
* ; FORM LINEAR COMBINATION OF FAST AND SLOW SCALE FACTORS
* ;
* ;  $Y(k) = (1-AL(k))*YL(k-1) + AL(k)*YU(k-1)$ 
* ;
MIX  LAC  YLL,10      * SHIFT YL RIGHT BY 6.
     SACH TEMP3      * (IE SCALE YL TO MATCH YU SINCE YL
     LAC  TEMP3      * CONTAINS 6 MORE LSB'S)
     AND  M1023
     ADD  YLH,10
     SACL TEMP3      * LOW HALF
     LAC  YU
     SUB  TEMP3      * YU-(YLL>>6)
     SACL TEMP3
     ZALH YLH
     ADDS YLL
     LT   AL         * AL IS IN 1.Q6
     MPY  TEMP3
     APAC          * YL + AL*(YU-(YLL>>6))
     SACL TEMP3
     SACH TEMP2      * TEMP2 | TEMP3 = Y * 2**6
     LAC  TEMP3,10   * SHIFT RIGHT BY 6.
     SACH TEMP3
     LAC  TEMP3
     AND  M1023      * MASK SIGN EXTENSION.
     ADD  TEMP2,10
     AND  M8191
     SACL Y          * SAVE Y.
     LAC  Y,14
     SACH TEMP3      * SAVE Y >> 2 .
     .
     .
     .

```

Figure 19. Quantizer Scale-Factor Adaptation: Mixing

CCITT IMPLEMENTATION OF ADPCM ON A TMS32010

The implementation of ADPCM that produces a bit-for-bit compatible solution with the CCITT test vectors uses a single TMS320M10 to accomplish a half-duplex transcoder. This solution can provide capability as either a transmitter or a receiver using either A-law or μ -law companding.

Hardware Logic and I/O

The hardware system for this transcoder implementation differs from Figure 13 in that data pins D15 and D14 are used to determine the mode of operation. Table 6 shows the operating mode for the various combined states of the data pin inputs.

Additionally, as has been noted in Figure 13, the interrupt or sample timing is an input to the INT pin in

Table 6. Operating Mode Selection

D15*	D14*	Operating Mode
L	L	μ -law transmitter
L	H	μ -law receiver
H	L	A-law transmitter
H	H	A-law receiver

*H = High logic level

L = Low logic level

the full-duplex implementation; here it is an input to the BIO pin. Each 125- μ s period, the TMS32010 reads a 64-kbit/s sample from the codec and writes a 32-kbit/s sample to the ADPCM interface, or it reads the 4-bit ADPCM sample and writes an 8-bit PCM sample to the codec.

For real-time execution, the TMS32010 requires the use of a 25-MHz clock input.

Software Logic and Flow

Tables 7 and 8 list the various blocks in the algorithm, directly relating them to Figures 7 and 8 by the signal names given in the description and function. No differentiation is made between the transmitter or receiver using A-law or μ -law. The blocks are listed in the order in which they are executed. Also listed is processor demand or loading which consists of the amount of program memory used to implement the given function and the number of instruction cycles executed in worst case. There are more blocks in the tables than are shown in the figures (e.g., the algorithm uses the

adaptive predictor at one point to produce the signal estimate, and later returns to update or adapt the predictor coefficients). Each block has been implemented using the equations given in previous sections concerning the ADPCM algorithm. For convenience, the equations implemented in each block are listed in the description section for the block. Additional details of the TMS32010 implementation are given in the next section, especially as they differ from the full-duplex implementation. The appendix contains a complete listing of the code.

Table 7. CCITT Transmitter

Order	Function	Description	CPU Clocks	Program Memory (Words)
1.	INPUT PCM	Read an 8 bit log-PCM sample $[s(k)]$ and linearize it to a 12-bit sample $[s_l(k)]$.	25 μ -law 24 A-law	0024 μ -law 0031 A-law
2.	COMPUTE SIGNAL ESTIMATE	Calculate the signal estimate $[s_g(k)]$ from the previous data samples $[d_q(k)]$ and reconstructed samples $[s_r(k)]$ through the predictor filter. (12), (11)	396	0167
3.	COMPUTE ADAPTIVE QUANTIZER	Calculate speed control $[a_l(k)]$ and quantizer scale factor $[y(k)]$ from past quantizer output $[l(k)]$. (6), (3)	30	001E
4.	COMPUTE DIFFERENCE SIGNAL	Calculate the difference signal $[d(k)]$ from the current sample $[s_l(k)]$ and signal estimate $[s_g(k)]$. (1)	3	0003
5.	COMPUTE QUANTIZED OUTPUT	Calculate the log of the difference signal $[d(k)]$ and adaptively quantize the result to yield the ADPCM output $[l(k)]$. (2)	42	00AD
6.	OUTPUT ADPCM	Write the ADPCM output $[l(k)]$.	6	0005
7.	COMPUTE RECON- STRUCTED SIGNAL	Calculate the inverse of the adaptively quantized signal $[d_q(k)]$ and the reconstructed signal difference $[s_r(k)]$. (10), (13)	66	00B0
8.	COMPUTE SCALE FACTOR	Calculate the updates for the scale-factor adaptation. (4), (5)	33	0022
9.	COMPUTE SPEED CONTROL	Calculate the update for the speed-control adaptation. (8), (9), (7)	30	001C
10.	COMPUTE PREDICTOR ADAPTATION	Calculate the updates for the adaptive predictor filter coefficients. (18), (16), (17), (14), (15)	111	0074
11.	WAIT	Spin until the next sample is available.	2+	0004

Table 8. CCITT Receiver

Order	Function	Description	CPU Clocks	Program Memory (Words)
1.	INPUT ADPCM	Read the ADPCM input $\{l(k)\}$.	10	0009
2.	COMPUTE SIGNAL ESTIMATE	Calculate the signal estimate $\{s_a(k)\}$ from the previous data samples $\{d_q(k)\}$ and reconstructed samples $\{s_r(k)\}$ through the predictor filter. (12), (11)	396	0167
3.	COMPUTE ADAPTIVE QUANTIZER	Calculate speed control $\{a_i(k)\}$ and quantizer scale factor $\{y(k)\}$ from past quantizer output $\{l(k)\}$. (6), (3)	30	001E
4.	COMPUTE QUANTIZED DIFFERENCE AND RECON- STRUCTED SIGNAL	Calculate the inverse of the adaptively quantized signal $\{d_q(k)\}$ and the reconstructed signal $\{s_r(k)\}$. (10), (13)	66	00B0
5.	COMPUTE SCALE FACTOR	Calculate the updates for the scale-factor adaptation. (4), (5)	33	0022
6.	COMPUTE SPEED CONTROL	Calculate the update for the speed-control adaptation. (8), (9), (7)	30	001C
7.	COMPUTE PREDICTOR ADAPTATION	Calculate the updates for the adaptive predictor filter coefficients. (18), (16), (17), (14), (15)	111	0074
8.	COMPUTE LOG-PCM	Convert the reconstructed linear-PCM signal $\{s_r(k)\}$ to a log-PCM signal $\{s_p(k)\}$.	35 μ -law 33 A-law	0074 μ -law 0072 A-law
9.	SYNCHRON- OUS CODING ADJUSTMENT	Calculate an ADPCM signal from the output $\{s_p(k)\}$ and adjust to create $\{s_d(k)\}$ if it differs from $\{l(k)\}$.	63	00DA
10.	OUTPUT PCM	Write the log-PCM output $\{s_d(k)\}$.	4	0003
11.	WAIT	Spin until the next interrupt.	2 +	0004

Implementation and Advantages of TMS32010 Architecture

Many of the same features are used in the bit-compatible implementation as were discussed in the full-duplex implementation. Some changes are imperative, since performance to the recommended specification requires executing certain calculations in a floating-point representation. These changes or additions require further modifications in order to limit the required amount of program memory to the internal memory space of the TMS32010.

One of the first observed requirements is that the processor must be capable of doing either A-law or μ -law companding and function as either a transmitter or a receiver.

The burden of determining the mode of operation is simplified by selecting one of the four modes from information available at the time of reset, and then executing from one of the four control loops until the next reset. Each loop, therefore, tests the $\overline{\text{BIO}}$ pin to determine when the next input sample is ready, rather than depending on the hardware interrupt.

The requirement of selecting either A-law or μ -law companding also means that a table lookup approach is beyond the program memory capacity. The conversion must be done algorithmically to reduce the amount of memory. Figures 20 and 21 illustrate μ -law companding as it is implemented in this algorithm.

```

XMTMU   IN      SCRACH,ADC
EXPNDU  LAC      SCRACH,8      ; SEEE MMMM 0000 0000
        XOR      KFF00        ; INVERT FROM TRANSMISSION FORMAT
        SACL     TEMP1        ; SAVE VALUE FOR PCM SIGN
        AND      M32767       ; 0EEE MMMM 0000 0000
        SACH     TEMP2,4      ; SAVE EXPONENT VALUE
        AND      M4095        ; 0000 MMMM 0000 0000
        ADD      BIAS,7       ; 0001 MMMM 1000 0000
        SACL     SCRACH
        LAC      TEMP1
        SACH     TEMP1        ; SIGN = FFFF OR 0000
        LACK     SBASE
        ADD      TEMP2,1      ; CALCULATE PCM SHIFT ADDRESS
        CALA
        SUB      BIAS,12      ; 0000000X XXXXXXXX XXXX0000 00000000
        SACH     SAMPLE,4
        LAC      SAMPLE      ; 000XXXXX XXXXXXXX
        XOR      TEMP1        ; POS - DO NOTHING : NEG - 1's COMP
        SUB      TEMP1        ; POS - DO NOTHING : NEG - 2's COMP
        SACL     SAMPLE
        .
        .
        .
* ;
SBASE   LAC      SCRACH,5      ; 00000000 0000001M MMM10000 00000000
        RET
        LAC      SCRACH,6      ; 00000000 000001MM MM100000 00000000
        RET
        LAC      SCRACH,7      ; 00000000 00001MMM M1000000 00000000
        RET
        LAC      SCRACH,8      ; 00000000 0001MMMM 10000000 00000000
        RET
        LAC      SCRACH,9      ; 00000000 001MMMM1 00000000 00000000
        RET
        LAC      SCRACH,10     ; 00000000 01MMMM10 00000000 00000000
        RET
        LAC      SCRACH,11     ; 00000000 1MMMM100 00000000 00000000
        RET
        LAC      SCRACH,12     ; 00000001 MMMM1000 00000000 00000000
        RET

```

Figure 20. μ -Law Expansion Code

```

      LAC      SR      ; GET RECONSTRUCTED SIGNAL
* ;
* ; COMPRESS--CONVERT TO PCM
* ;
CMPRSU  SACH      TEMP4      ; SAVE SIGN OF SR
      ABS
      ADD      BIAS      ; ADD BIAS
      SACL     SCRACH      ; SAVE BIASED PCM VALUE
      SUB      ONE,9      ; EXP = 7 - 4 OR 3 - 0
      BGEZ     SCL427
SCL023  ADD      THREE,7    ; EXP = 3 - 2 OR 1 - 0
      BGEZ     SCL223
SCL021  ADD      ONE,6      ; EXP = 1 OR 0
      BGEZ     SCALE1
SCALE0  LAC      M15,1      ; EXP = 0
      AND      SCRACH      ; MASK FOR MANTISSA
      SACL     SCRACH
      ADD      BIAS
      SACL     SAMPLE      ; BIASED QUANTIZED VALUE
      LAC      SCRACH,15
      LARK     0,0
      B        FINI
SCALE1  LAC      M15,2      ; EXP = 1
      AND      SCRACH      ; MASK FOR MANTISSA
      SACL     SCRACH
      ADD      BIAS,1
      SACL     SAMPLE      ; BIASED QUANTIZED VALUE
      LAC      SCRACH,14
      LARK     0,1
      B        FINI
      .
      .
      .
FINI    SACH      SCRACH      ; SAVE NORMALIZED MANTISSA
      LAC      SCRACH
      SAR      0,TEMP1
      ADD      TEMP1,4      ; ADD EXPONENT
CLNUP   ADD      TEMP4,7
      AND      M255
      SACL     SCRACH      ; 2's COMPLEMENT OF MULAW-PCM
      LAC      SAMPLE      ; REMOVE BIAS FROM QUANTIZED VALUE
      SUB      BIAS
      XOR      TEMP4
      SUB      TEMP4
      SACL     SAMPLE      ; 2's COMPLEMENT OF QUANTIZED SAMPLE
* ;
* ;      CALL      AQUAN
* ;
* ;      CALL      SYNC
* ;
      XOR      M255      ; FLIP BITS FOR TRANSMISSION
      SACL     SCRACH
      OUT      SCRACH,DAC

```

Figure 21. μ -Law Compression Code

The predictor filter implementation is also modified from what has been previously presented. In the CCITT recommendation, the processing of the signal through the predictor filter is performed in a floating-point format. This requirement leads to several modifications. First, all input signals to the filter, $d_q(k)$ and $s_r(k)$, must be converted to a floating-point notation. The conversion to this notation is accomplished by a binary search of the original fixed-point word. As previously mentioned, this technique is explained in some detail in the application report, FLOATING-POINT ARITHMETIC WITH THE TMS32010. Second, the filter coefficients, $a_i(k)$ and $b_i(k)$, must also be floated for each sample so that a floating-point multiply can be executed for each filter tap.

Accumulation of the filter taps is carried out in fixed-point notation. Fixing a floating-point number is equivalent to the scaling presented for taking the anti-log of a number. Some of the floating-point results must be left-shifted, while others need to be right-shifted. The shift is accomplished by use of a scaling factor or multiplier, selected by the exponent sum of the floating-point multiply. Positive multipliers are used to indicate what is effectively a right shift with the result being stored from the high half of the accumulator. Negative multipliers indicate that the result is in the low half of the accumulator and is used for values which have been left shifted.

The process of a single filter tap, not including the code to float the signal and the coefficient, is shown in Figure 22.

```

* ;*****
* ;
* ; COMPUTE SEZ -- PARTIAL SIGNAL ESTIMATE
* ;
* ; SEZ(k) = B1(k-1)*DQ(k-1) + ... + B6(k-1)*DQ(k-6)
* ;
* ; MULTIPLIES ARE DONE IN FLOATING POINT
* ; DQ's ARE STORED IN FLOATING-POINT NOTATION
* ; B's ARE FLOATED EACH PASS
* ;
* ; NOTATION: DQnEXP -- 4 bits + OFFSET
* ; DQnMAN*8 -- 9 bits
* ; Bn -- 16 b TC ; q14
* ; SEZ -- 16 b TC ; q0
* ;*****
* ;
SIGDIF LAC B6,14 ; COMPUTE B6*DQ5.
CALL FLOAT ; RET/W MANTISSA IN TEMP1; EXP IN ACC.
ADD DQ5EXP
SACL SUM1
LAR 0,SUM1 ; EXP OF PRODUCT.
LT DQ5MAN ; DQnMAN SCALED BY 2**3.
LAC THREE,7 ; PRODUCT FUDGE FACTOR (48*8).
MPY TEMP1
LTA *,0 ; B6MAN*(DQ5MAN*8)+(48*8)
AND KFF80 ; SAVE ONLY 8 MSB'S.
SACL TEMP1
MPY TEMP1 ; APPLY SHIFT FACTOR.
PAC
BLZ RS1 ; EXP >= 26
SACH SUM1,1 ; EXP < 26
CHK1 ZALS B6 ; CHECK SIGN OF PRODUCT.
XOR SDQ6
AND K32768
BZ POS1
NEG1 ZAC ; NEGATE IF NECESSARY.
SUB SUM1

```

Figure 22. Predictor Filter Execution


```

POS1      SACL      SUM1
          LAC        B5,14    ; COMPUTE B5*DQ4.
          .
          .
          .
RS1        ABS                ; MAKE POSITIVE BEFORE MASK.
          AND        M32767    ; KEEP LOWER 15 BITS.
          SACL        SUM1     ; SAVE RESULT.
          B           CHK1

```

Figure 22. Predictor Filter Execution (Concluded)

SUMMARY

The TMS32010 provides an efficient solution to transcoding a 64-kbit/s PCM signal to a 32-kbit/s bit stream. Transcoding, as described in this application report, is an effective way to maintain the signal quality provided by 7-bit PCM while reducing the data rate.

The basic ADPCM algorithm has been implemented in two slightly different ways. One solution provides CCITT bit-for-bit compatibility. Using this algorithm, a half-duplex transcoder is created that can transcode either A-law or μ -law signals as either a transmitter or a receiver. No external program memory is required for this implementation, although it does require the use of a 25-MHz TMS32010 microprocessor. The second described solution is particularly attractive since it uses a single, 20.5-MHz TMS32010 microprocessor that requires no external program memory to perform a real-time full-duplex (non-CCITT) channel transcoding.

In selecting one of these two solutions, the primary consideration is the network interfacing requirement. For systems that only have analog interfaces to other parts of the network, the full-duplex solution will provide the best choice. On the other hand, a network that may include a digital interface to other ADPCM transcoders will probably require the CCITT bit-compatible solution. Both solutions provide high-quality signal transcoding.

A complete assembled code listing is provided in the appendix of this report and is also available in 1600-BPI

VAX/VMS tape format. The software may be purchased by ordering the TMS32010 Software Exchange Library, TMDC3240212-18, from Texas Instruments. For further information, please contact your nearest TI sales representative.

REFERENCES

- "Recommendation G.721, 32 kbit/s Adaptive Differential Pulse Code Modulation," *CCITT* (1984).
- N.S. Jayant (ed.), *Waveform Quantization and Coding*, IEEE Press (1976).
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- Bernhard E. Keiser, *Digital Telephony: Speech Digitization*, George Washington University (1981).
- Companding Routines for the TMS32010*, Texas Instruments Incorporated (1984).
- Floating-Point Arithmetic with the TMS32010*, Texas Instruments Incorporated (1984).
- Implementation of FIR/IIR Filters with the TMS32010*, Texas Instruments Incorporated (1984).
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Appendix
ADPCM Assembly Language Programs

CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03 03-20-85	PAGE 0005	CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03 03-20-85	PAGE 0006
A0175	0052 2618	SBASEA	LAC	SCRACH,6	:	00000000	00000000	MM000000	00000000
A0176	0053 0D4C	ADD	RET	ONE,13	:	00000000	00000000	MM100000	00000000
A0177	0054 7F80	NOP							
A0178	0055 2618	LAC		SCRACH,6	:	00000000	000001MM	MM100000	00000000
A0179	0056 2618	LAC		BIASA,6	:	00000000	000001MM	MM100000	00000000
A0180	0057 0671	RET							
A0181	0058 7F80	NOP							
A0182	0059 7F80	LAC		SCRACH,7	:	00000000	000000MM	MM000000	00000000
A0183	005A 2718	LAC		BIASA,7	:	00000000	00001MMH	MM100000	00000000
A0184	005B 0711	ADD	RET						
A0185	005C 7F80	NOP							
A0186	005D 7F80	LAC		SCRACH,8	:	00000000	000000MM	MM000000	00000000
A0187	005E 2818	LAC		BIASA,8	:	00000000	0001MMH	MM100000	00000000
A0188	005F 0871	RET							
A0189	0060 7F80	NOP							
A0190	0061 7F80	NOP							
A0191	0062 2918	LAC		SCRACH,9	:	00000000	000000MM	MM000000	00000000
A0192	0063 7971	ADD	RET	BIASA,9	:	00000000	001MMH	MM000000	00000000
A0193	0064 7F80	RET							
A0194	0065 7F80	NOP							
A0195	0066 2A18	LAC		SCRACH,10	:	00000000	000000MM	MM000000	00000000
A0196	0067 7A71	ADD	RET	BIASA,10	:	00000000	01MMH	MM100000	00000000
A0197	0068 7F80	RET							
A0198	0069 7F80	NOP							
A0199	006A 2818	LAC		SCRACH,11	:	00000000	000000MM	MM000000	00000000
A0200	006B 0B71	ADD	RET	BIASA,11	:	00000000	1MMH	MM100000	00000000
A0201	006C 7F80	RET							
A0202	006D 7F80	NOP							
A0203	006E 2C18	LAC		SCRACH,12	:	00000000	000000MM	MM000000	00000000
A0204	006F 0C71	ADD	RET	BIASA,12	:	00000001	MMH	MM100000	00000000
A0205	0070 7F80	RET							
<pre> : MU-LAW RECEIVER : RCVMU IN I,CCITT ; input ADPCM : LAC ; SACL I ; SUB ONE,3 ; determine magnitude of ADPCM BLZ DO32KU ; LAC I ; XOR M15 ; SACL I ; : compute pcm output : DO32KU CALL SIGDIF CALL PROICT : : LINEAR TO U-LAW PCM COMPRESSION/U-LAW TO LINEAR EXPANSION : : INPUT: LINEAR PCM SAMPLE -- SR : OUTPUT: A-LAW PCM SAMPLE -- SP (SCRACH) : LINEAR PCM SAMPLE -- SLX (SAMPLE) : : NOTATION: SR -- 16b TC (Q0) : SP -- 8b SM (Q4) : SLX -- 14b TC (Q0) : : : SR --> COMPRESS -----> EXPAND -----> : -----> -----> -----> -----> : -----> -----> -----> -----> : : LAC SR ; get reconstructed signal : compress--convert to pcm : CMPSU SACH TEMP4 ; save sign of SR ADD BIAS ; add bias SACL SCRACH ; save biased PCM value SUB ONE,9 ; exp = 7 - 4 or 3 - 0 BGEZ SCL427 : SCL023 ADD THREE,7 ; exp = 3 - 2 or 1 - 0 BGEZ SCL223 </pre>									
A0207									
A0208									
A0209									
A0210	0071 4201								
A0211	0072 2001								
A0212	0073 5002								
A0213	0074 134C								
A0214	0075 FA00								
A0215	0076 007A								
A0216	0077 2002								
A0217	0078 7860								
A0218	0079 5002								
A0219									
A0220									
A0221	007A F800								
A0222	007B 01B3								
A0223	007C F800								
A0224	007D 0555								
A0225									
A0226									
A0227									
A0228									
A0229									
A0230									
A0231									
A0232									
A0233									
A0234									
A0235									
A0236									
A0237									
A0238									
A0239									
A0240									
A0241									
A0242									
A0243									
A0244									
A0245									
A0246	007E 2013								
A0247									
A0248									
A0249									
A0250	007F 5824								
A0251	0080 7F88								
A0252	0081 004B								
A0253	0082 501B								
A0254	0083 194C								
A0255	0084 F000								
A0256	0085 0093								
A0257	0086 0770								
A0258	0087 F000								

```

A0259 008A 064C SCL021 ADD ONE,6 ; exp = 1 or 0
A0260 008A F000 BGEZ SCALE1
A0261 008C 2160 SCALED LAC M15,1
A0262 008E 791B AND SCRAH ; mask for mantissa
A0263 008E 791B AND SCRAH ; exp = 0
A0264 008F 004D ADD BIAS,1
A0265 0090 5026 SACL SAMPLE
A0266 0091 2F1B SACL SAMPLE
A0267 0092 7000 LARK LARK
A0268 0093 F900 B FINI
A0269 0095 226D SCALE1 LAC M15,2
A0270 0096 791B AND SCRAH ; exp = 1
A0271 0097 501B SACL SCRAH ; mask for mantissa
A0272 0098 014D ADD BIAS,1
A0273 0099 5026 SACL SAMPLE
A0274 009A 2E1B LARK LARK
A0275 009B 7001 B FINI
A0276 009C F900 B FINI
A0277 009E 174C SCL223 SUB ONE,7
A0278 009F F000 BGEZ SCALE3
A0279 00A1 236D SCALE2 LAC M15,3
A0280 00A2 791B AND SCRAH ; exp = 2
A0281 00A3 501B SACL SCRAH ; mask for mantissa
A0282 00A4 024D ADD BIAS,2
A0283 00A5 5026 SACL SAMPLE
A0284 00A6 2D1B LARK LARK
A0285 00A7 7002 B FINI
A0286 00A8 F900 B FINI
A0287 00A9 00E6 SCALE3 LAC M15,4
A0288 00AB 791B AND SCRAH ; exp = 3
A0289 00AC 791B SACL SCRAH ; mask for mantissa
A0290 00AD 034D ADD BIAS,3
A0291 00AE 5026 SACL SAMPLE
A0292 00AF 2C1B LARK LARK
A0293 00B0 7003 B FINI
A0294 00B1 F900 B FINI
A0295 00B3 197D SCL427 SUB THREE,9
A0296 00B4 F000 BGEZ SCL627
A0297 00B5 00C8 SCL425 ADD ONE,10
A0298 00B7 F000 BGEZ SCALE5
A0299 00B8 00C2 SCALE4 LAC M15,5
A0300 00B9 256D AND SCRAH ; exp = 4
A0301 00BB 791B SACL SCRAH ; mask for mantissa
A0302 00BC 044D ADD BIAS,4
A0303 00BD 5026 SACL SAMPLE
A0304 00BE 281A LARK LARK
A0305 00BF 7004 B FINI
A0306 00C0 F900 B FINI
A0307 00C2 266D SCALE5 LAC M15,6
A0308 00C3 791B AND SCRAH ; exp = 5
A0309 00C4 501B SACL SCRAH ; mask for mantissa
A0310 00C5 054D ADD BIAS,5
A0311 00C6 5026 SACL SAMPLE
A0312 00C7 2A1B LARK LARK
A0313 00C8 7005 B FINI
A0314 00C9 F900 B FINI
A0315 00CB 184C SCL627 SUB ONE,11
A0316 00CC F000 BGEZ SCALE7
A0317 00CE 276D SCALE6 LAC M15,7
A0318 00CF 791B AND SCRAH ; exp = 6
A0319 00D0 501B SACL SCRAH ; mask for mantissa
A0320 00D1 064D ADD BIAS,6
A0321 00D2 5026 SACL SAMPLE
A0322 00D3 291B LARK LARK
A0323 00D4 7006 B FINI
A0324 00D5 F900 B FINI
A0325 00D7 1C4C SCALE7 SUB ONE,12
A0326 00D8 FAD0 BLZ NORMAL
A0327 00DA 2767 SATCH LAC K63,7
A0328 00DB 5026 SACL SAMPLE
A0329 00DC 7E7F LACK 127
A0330 00DD F900 B CLNUP
A0331 00DF 286D NORMAL LAC M15,8
A0332 00E0 791B AND SCRAH ; mask for mantissa
A0333 00E1 501B SACL SCRAH ; exp = 7
A0334 00E2 074D ADD BIAS,7
A0335 00E3 5026 SACL SAMPLE
A0336 00E4 281B LARK LACK
A0337 00E5 7007 FINI
A0338 00E6 581B SACL SCRAH
A0339 00E7 201B LAC SCRAH
A0340 00E9 3021 SAR 0,TEMP1
A0341 00EA 0421 ADD TEMP1,4
A0342 00EA 072A CLNUP
A0343 00EB 7947 AND M255
A0344 00EC 501B SACL SCRAH
A0345 00ED 2026 LAC SCRAH
A0346 00EE 104D SUB BIAS
A0347 00EF 7824 XOR TEMP4
A0348 00F0 1024 SUB TEMP4
A0349 00F1 5026 SACL SAMPLE
A0350 00F2 F800 CALL AQUAN
A0351 00F3 02AA *;
A0352 00F4 F800 CALL SYNC
A0353 00F5 0188 *;
A0354 00F6 7847 XOR M255
A0355 00F7 501B SACL SCRAH

```

```

; exp = 7
; mag > 8191 ?
; save max biased quantized value
; set maximum mulaw magnitude
; mask for mantissa
; biased quantized value
; save normalized mantissa
; add exponent
; signed magnitude of mulaw-PCM
; remove bias from quantized value
; 2's complement of quantized sample
; flip bits for transmission

```

A0357	00FB	491B			
A0358	00FA	F600	MULAWR B10Z	OUT	SCRACH,DAC ; output mu-law PCM
	00FA	0071			; wait for next sample
A0359	00FB	F900	B		
	00FC	00F9		MULAWR	RCVMU

CCITT 32010 FAMILY MACRO ASSEMBLER PC2.1 84.107 16:36:03 03-20-85
PAGE 0010[illegible]


```

B0056 01B7 5022      SACL      ; mult mant, add 48, fetch shift fac
B0057 01B8 3822      LAR        ; exp of product offset by table add
B0058 01B9 4A50      LT         ; scaled up by 2**3
B0059 01BA 2000      LTR        ; multiply fudge factor
B0060 01BB 6021      LTA        ; mult mant, add 48, fetch shift fac
B0061 01BC 6C80      LTA        ; mult mant, add 48, fetch shift fac
B0062 01BD 796E      SACL      ; mult mant, add 48, fetch shift fac
B0063 01BE 5021      SACL      ; mult mant, add 48, fetch shift fac
B0064 01BF 6021      MPY        ; apply shift factor = f(exp)
B0065 01C0 7F8E      PAC        ; exp >= 26
B0066 01C1 FAD0      BLZ        ; exp < 26
B0067 01C2 04B6      BZ         ; check sign of product
B0068 01C3 5922      SACL      ; exp < 26
B0069 01C4 660F      CHK1       ; check sign of product
B0070 01C5 785A      XOR        ; compute B5*DQ4
B0071 01C6 7948      AND        ; ret/w mantissa in TEMPI; exp in ac
B0072 01C7 FF00      BZ         ; negate if necessary
B0073 01C8 01CC      NEG1       ; negate if necessary
B0074 01C9 7F89      ZAC        ; exp of product offset by table add
B0075 01CA 0122      SUB        ; scaled up by 2**3
B0076 01CB 2E0E      SACL      ; multiply fudge factor
B0077 01CC 01D0      CALL       ; mult mant, add 48, fetch shift fac
B0078 01CD F800      LTA        ; mult mant, add 48, fetch shift fac
B0079 01CE 040E      ADD        ; exp of product offset by table add
B0080 01CF 0017      DQ4EXP    ; scaled up by 2**3
B0081 01D0 6919      DQ4EXP    ; multiply fudge factor
B0082 01D1 5023      SACL      ; mult mant, add 48, fetch shift fac
B0083 01D2 3823      SACL      ; mult mant, add 48, fetch shift fac
B0084 01D3 685F      LAR        ; exp of product offset by table add
B0085 01D4 2770      LTD        ; scaled up by 2**3
B0086 01D5 6021      LAC        ; multiply fudge factor
B0087 01D6 6C80      MPY        ; mult mant, add 48, fetch shift fac
B0088 01D7 796E      AND        ; mult mant, add 48, fetch shift fac
B0089 01D8 5021      AND        ; mult mant, add 48, fetch shift fac
B0090 01D9 6021      TEMP1     ; apply shift factor = f(exp)
B0091 01DA 7F8E      PAC        ; exp >= 26
B0092 01DB FF00      BLZ        ; exp < 26
B0093 01DC 04B6      SACL      ; check sign of product
B0094 01DD 5922      ZAC        ; exp < 26
B0095 01DE 660F      CHK2       ; check sign of product
B0096 01DF 785A      XOR        ; compute B2*DQ1
B0097 01E0 7948      AND        ; ret/w mantissa in TEMPI; exp in ac
B0098 01E1 FF00      BZ         ; negate if necessary
B0099 01E2 01E6      NEG2       ; negate if necessary
B0100 01E3 7F89      ZAC        ; exp of product offset by table add
B0101 01E4 0123      SUB        ; scaled up by 2**3
B0102 01E5 5023      SACL      ; multiply fudge factor
B0103 01E6 2E00      LAC        ; mult mant, add 48, fetch shift fac
B0104 01E7 F800      CALL       ; mult mant, add 48, fetch shift fac
B0105 01E8 040E      ADD        ; exp of product offset by table add
B0106 01E9 0018      DQ3EXP    ; scaled up by 2**3
B0107 01EA 6918      DQ3EXP    ; multiply fudge factor
B0108 01EB 5025      SACL      ; mult mant, add 48, fetch shift fac
B0109 01EC 3825      LAR        ; exp of product offset by table add
B0110 01ED 277E      LTD        ; scaled up by 2**3
B0111 01EE 6021      LAC        ; multiply fudge factor
B0112 01EF 277E      MPY        ; mult mant, add 48, fetch shift fac
B0113 01F0 7F8E      LTA        ; mult mant, add 48, fetch shift fac
B0114 01F1 796E      AND        ; mult mant, add 48, fetch shift fac
B0115 01F2 5021      AND        ; mult mant, add 48, fetch shift fac
B0116 01F3 6021      MPY        ; apply shift factor = f(exp)
B0117 01F4 FF00      BLZ        ; exp >= 26
B0118 01F5 040E      ADD        ; exp of product offset by table add
B0119 01F6 6917      DQ2EXP    ; scaled up by 2**3
B0120 01F7 501E      SACL      ; multiply fudge factor
B0121 01F8 001E      LAR        ; mult mant, add 48, fetch shift fac
B0122 01F9 381E      LTD        ; scaled up by 2**3
B0123 01FA 2770      LAC        ; multiply fudge factor
B0124 01FB 6021      MPY        ; mult mant, add 48, fetch shift fac
B0125 01FC 6C80      AND        ; mult mant, add 48, fetch shift fac
B0126 01FD 796E      AND        ; mult mant, add 48, fetch shift fac
B0127 01FE 5021      AND        ; mult mant, add 48, fetch shift fac
B0128 01FF 6021      MPY        ; apply shift factor = f(exp)
B0129 0200 FF00      BLZ        ; exp >= 26
B0130 0201 0405      SACL      ; check sign of product
B0131 0202 591E      ZAC        ; exp < 26
B0132 0203 660C      CHK4       ; check sign of product
B0133 0204 7857      XOR        ; compute B3*DQ2
B0134 0205 7948      AND        ; ret/w mantissa in TEMPI; exp in ac
B0135 0206 FF00      BZ         ; negate if necessary
B0136 0207 021A      ZAC        ; exp of product offset by table add
B0137 0208 021A      ZAC        ; scaled up by 2**3
B0138 0209 021A      SACL      ; multiply fudge factor
B0139 0210 021A      SACL      ; mult mant, add 48, fetch shift fac
B0140 0211 FF00      BZ         ; mult mant, add 48, fetch shift fac
B0141 0212 021A      ZAC        ; exp of product offset by table add
B0142 0213 021A      ZAC        ; scaled up by 2**3
B0143 0214 021A      SACL      ; multiply fudge factor
B0144 0215 2E08      LAC        ; mult mant, add 48, fetch shift fac
B0145 0216 F800      CALL       ; mult mant, add 48, fetch shift fac
B0146 0217 040E      ADD        ; exp of product offset by table add
B0147 0218 0016      DQ1EXP    ; scaled up by 2**3
B0148 0219 6916      DQ1EXP    ; multiply fudge factor
B0149 0220 501F      SACL      ; mult mant, add 48, fetch shift fac
B0150 0221 381F      LAR        ; exp of product offset by table add
B0151 0222 2770      LAC        ; scaled up by 2**3
B0152 0223 6021      MPY        ; multiply fudge factor
B0153 0224 6C80      LTA        ; mult mant, add 48, fetch shift fac
B0154 0225 796E      AND        ; mult mant, add 48, fetch shift fac
B0155 0226 5021      AND        ; mult mant, add 48, fetch shift fac
B0156 0227 6021      MPY        ; apply shift factor = f(exp)
B0157 0228 7F8E      PAC        ; exp of product offset by table add

```

```

B0107 01F0 6C80      LTA        ; mult mant, add 48, fetch shift fac
B0108 01F1 796E      AND        ; mult mant, add 48, fetch shift fac
B0109 01F2 5021      SACL      ; apply shift factor = f(exp)
B0110 01F3 6021      MPY        ; apply shift factor = f(exp)
B0111 01F4 7F8E      PAC        ; exp >= 26
B0112 01F5 FAD0      BLZ        ; exp < 26
B0113 01F6 5920      SACH       ; check sign of product
B0114 01F7 660F      CHK3       ; check sign of product
B0115 01F8 7858      XOR        ; compute B3*DQ2
B0116 01F9 7948      AND        ; ret/w mantissa in TEMPI; exp in ac
B0117 01FB FF00      BZ         ; negate if necessary
B0118 01FC 0200      ZAC        ; negate if necessary
B0119 01FD 7F89      NEG3       ; negate if necessary
B0120 01FE 1025      SUB        ; compute B3*DQ2
B0121 0200 2E0C      LAC        ; ret/w mantissa in TEMPI; exp in ac
B0122 0201 F800      CALL       ; compute B3*DQ2
B0123 0202 040E      ADD        ; exp of product offset by table add
B0124 0203 0017      DQ2EXP    ; scaled up by 2**3
B0125 0204 6917      DQ2EXP    ; multiply fudge factor
B0126 0205 501E      SACL      ; mult mant, add 48, fetch shift fac
B0127 0206 381E      LAR        ; exp of product offset by table add
B0128 0207 2770      LTD        ; scaled up by 2**3
B0129 0208 6021      LAC        ; multiply fudge factor
B0130 0209 6C80      AND        ; mult mant, add 48, fetch shift fac
B0131 020A 796E      AND        ; mult mant, add 48, fetch shift fac
B0132 020B 5021      AND        ; mult mant, add 48, fetch shift fac
B0133 020C 5021      SACL      ; apply shift factor = f(exp)
B0134 020E 7F8E      PAC        ; apply shift factor = f(exp)
B0135 0210 FAD0      BLZ        ; exp >= 26
B0136 0211 591E      SACH       ; negative if necessary
B0137 0212 660C      CHK4       ; negative if necessary
B0138 0213 7857      XOR        ; compute B2*DQ1
B0139 0214 7948      AND        ; compute B2*DQ1
B0140 0215 FF00      BZ         ; ret/w mantissa in TEMPI; exp in ac
B0141 0216 021A      ZAC        ; negative if necessary
B0142 0217 021A      ZAC        ; negative if necessary
B0143 0218 021A      SACL      ; negative if necessary
B0144 021A 2E08      LAC        ; compute B2*DQ1
B0145 021B F800      CALL       ; ret/w mantissa in TEMPI; exp in ac
B0146 021C 040E      ADD        ; negative if necessary
B0147 021E 6916      DQ1EXP    ; negative if necessary
B0148 021F 501F      SACL      ; negative if necessary
B0149 0220 381F      LAR        ; negative if necessary
B0150 0221 685C      LTD        ; negative if necessary
B0151 0222 2770      LAC        ; negative if necessary
B0152 0223 6021      MPY        ; negative if necessary
B0153 0224 6C80      LTA        ; negative if necessary
B0154 0225 796E      AND        ; negative if necessary
B0155 0226 5021      AND        ; negative if necessary
B0156 0227 6021      MPY        ; negative if necessary
B0157 0228 7F8E      PAC        ; negative if necessary

```



```

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B0263 0273 5021      SACL      TEMPI      ; apply shift factor = f(exp)
B0264 0274 6021      MPY      TEMPI
B0265 0275 7F9E      PLZ      RS21      ; exp >= 26
B0266 0276 FA00      BCL      RS21
B0267 0277 0409      SACH      SUM8.1      ; exp < 26
B0268 0278 5928      CHKZ1  DMOV      SR
B0269 0279 6913      ZALS      SR      ; check sign of product
B0270 027A 6613      XOR      A1
B0271 027B 7811      AND      K32768
B0272 027C 7948      AND      K32768
B0273 027D FF00      BZ      P0521
B0274 027E 0282      NEG21  ZAC      ; negate if necessary
B0275 027F 7F89      SUB      SUM8
B0276 0280 1058      SACL      SUM8
B0277 0281 5021      EQU      $
B0278 0282 0282      POS21  EQU
B0279 0283 0282      ; *****
B0280 0284 0282      ; ACCUMULATE FILTER TAP OUTPUTS (ACCUM)
B0281 0285 0282      ;
B0282 0286 0282      ; INPUT: FILTER TAP OUTPUTS -- Man & Wbn (SUMm)
B0283 0287 0282      ;
B0284 0288 0282      ; OUTPUT: PARTIAL SUM OF ZEROES FILTER -- SEZ
B0285 0289 0282      ; SIGNAL ESTIMATE -- SE
B0286 0290 0282      ;
B0287 0291 0282      ; NOTATION: SUMm -- 16b TC (Q1)
B0288 0292 0282      ; SEZ -- 15b TC (00) [sign extended]
B0289 0293 0282      ; SE -- 15b TC (00) [sign extended]
B0290 0294 0282      ; *****
B0291 0295 0282      ; LAC      SUM6.15      ; accumulate products
B0292 0296 0282      ; ADD      SUM5.15
B0293 0297 0282      ; ADD      SUM4.15
B0294 0298 0282      ; ADD      SUM3.15
B0295 0299 0282      ; ADD      SUM2.15
B0296 029A 0282      ; ADD      SUM1.15
B0297 029B 0282      ; SACH      SEZ.1
B0298 029C 5904      ADD      SUM7.15
B0299 029D 0F27      ADD      SUM8.15
B0300 029E 0F28      ADD      SUM8.15
B0301 029F 5903      SACH      SE.1
B0302 029A 0F03      LAC      SE.15
B0303 029B 5803      SACH      SE
B0304 029C 5803      ; *****
B0305 029D 5803      ; limit speed control parameter: AL <= 1.0
B0306 029E 5803      ;
B0307 029F 5803      ; AL = 1      IF APP > 1
B0308 029A 5803      ; AL = APP      IF APP < 1
B0309 029B 5803      ;
B0310 029C 5803      ; INPUT: UNLIMITED SPEED CONTROL -- AP (APP)
B0311 029D 5803      ;
B0312 029E 5803      ; OUTPUT: LIMITED SPEED CONTROL -- AL
B0313 029F 5803      ;
B0314 029A 5803      ; NOTATION: APP -- unsigned 10b (Q8)
B0315 029B 5803      ; AL -- unsigned 7b (Q6)
B0316 029C 5803      ;
B0317 029D 5803      ;

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B0318 029E 5803      ; *****
B0319 029F 5803      ; LAC      ONE.12
B0320 029A 5803      ; SACL      AL
B0321 029B 5803      ; LAC      APP
B0322 029C 5803      ; SUB      ONE.B
B0323 029D 5803      ; BGEZ      MIX
B0324 029E 5803      ; ;APP >= 1
B0325 029F 5803      ;
B0326 029A 5803      ; LAC      APP.4
B0327 029B 5803      ; AND      MPFCO
B0328 029C 5803      ; SACL      AL
B0329 029D 5803      ; ;APP < 1
B0330 029E 5803      ; *****
B0331 029F 5803      ; MIX
B0332 029A 5803      ; form linear combination of fast and slow scale factors
B0333 029B 5803      ;
B0334 029C 5803      ; Y(k) = (1-AL(k))*YL(k-1) + AL(k)*YU(k-1)
B0335 029D 5803      ; INPUT: SLOW QUANTIZER SCALE FACTOR -- YL (YL/YLH)
B0336 029E 5803      ; FAST QUANTIZER SCALE FACTOR -- YU (YL/YLH)
B0337 029F 5803      ; LIMITED SPEED CONTROL -- AL
B0338 029A 5803      ;
B0339 029B 5803      ; OUTPUT: QUANTIZER SCALE FACTOR -- Y
B0340 029C 5803      ; RESEALED QUANTIZER SCALE FACTOR -- YOVER4
B0341 029D 5803      ;
B0342 029E 5803      ; NOTATION: YL -- 19b unsigned (Q15)
B0343 029F 5803      ; stored as: -- YL
B0344 029A 5803      ; low 15b -- YL
B0345 029B 5803      ; 4b -- YLH
B0346 029C 5803      ; YU -- 13b unsigned (Q9)
B0347 029D 5803      ; AL -- 7b unsigned (Q6)
B0348 029E 5803      ; Y -- 13b unsigned (Q9)
B0349 029F 5803      ; YOVER4 -- 11b unsigned (Q7)
B0350 029A 5803      ; *****
B0351 029B 5803      ; ; shift y1 right by 6
B0352 029C 5803      ;
B0353 029D 5803      ; LAC      YLL.10
B0354 029E 5803      ; SACH      TEMP3
B0355 029F 5803      ; LAC      YLH.9
B0356 029A 5803      ; ADD      TEMP3
B0357 029B 5803      ; SACL      TEMP3
B0358 029C 5803      ; LAC      YU
B0359 029D 5803      ; SUB      TEMP3
B0360 029E 5803      ; SACL      TEMP1
B0361 029F 5803      ; MPY      TEMP1
B0362 029A 5803      ; PAC      NONNEG
B0363 029B 5803      ; BGEZ      M4095
B0364 029C 5803      ; ADD      TEMP3.12
B0365 029D 5803      ; NONNEG      ADD
B0366 029E 5803      ; Y.4
B0367 029F 5803      ; SACH      Y.14
B0368 029A 5803      ; LAC      YOVER4
B0369 029B 5803      ; SACH      RET
B0370 029C 5803      ;
B0371 029D 5803      ; compute and save y>>2
B0372 029E 5803      ; ret from sig01f
B0373 029F 5803      ;

```

```
0003 COPY AQUAN,ASM
0001
0002
0003
0004 DIFFERENCE SIGNAL COMPUTATION
0005
0006 INPUT: LINEAR PCM SAMPLE --- SL (SAMPLE)
0007 SIGNAL ESTIMATE --- SE
0008
0009 OUTPUT: DIFFERENCE SIGNAL --- D (accumulator)
0010
0011 NOTATION: SL -- 14b TC (Q0) [sign extended]
0012 SE -- 15b TC (Q0) [sign extended]
0013 D -- 16b TC (Q0)
0014
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```

02AA 2026
02AB 1003

0023 AQUAN LAC SAMPLE ; compute difference sig
0025 AQUAN SUB SE
0026
0027
0028
0029
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0031
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0038
0039
0040
0041
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ADAPTIVE QUANTIZER

Implements the following modules (per CCITT spec):

LOG -- computes log of difference signal
SUBTB -- scales log by subtracting Y
QUAN -- computes 4b output

INPUT: DIFFERENCED PCM SAMPLE --- D (accumulator)
QUANTIZER SCALE FACTOR --- Y (OVER4)

OUTPUT: ADPCM OUTPUT SAMPLE --- I

NOTATION: D -- 16b TC (Q0)
Y -- 11b SM (Q7) POSITIVE VALUE ONLY
I -- 4b SM (Q0)

DS

D --> LOG --> DL --> DLN --> I
SUBTB --> SUBTB --> I
QUAN --> I

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02AC 5824
02AD 7F88
02AE 5021
02AF 184C
02B0 F000
02B1 02E7
02B2 0460
02B3 F000
02B4 0283
02B5 0276
02B6 F000
02B7 02C3
02B8 014C
02B9 F000
02BA 02BF
02BB 7000
02BC 2721
02BD F900
02BE 0321
02BF 7001
02C0 2621
02C1 F900
02C2 0321
02C3 124C
02C4 F000
02C5 02C3
02C6 7002
02C7 2521
02C8 F900
02C9 0321
02CA 7003
02CB 2421
02CC F900
02CD 0321
02CE 1470
02CF F000
02D0 02DC
02D1 054C
02D2 F000
02D3 0208
02D4 0004
02D5 2321
02D6 0207
02D7 0321
02D8 7005
02D9 2221
02DA F900
02DB 0321

SACH
ABS
SACL
GETEXP SUB
BGEZ
C0T07 ADD
BGEZ
C0T03 ADD
BGEZ
C0T01 ADD
BGEZ
EXP0 LARK
LAC
B
EXP1 LARK
LAC
B
C2T03 SUB
BGEZ
EXP2 LARK
LAC
B
EXP3 LARK
LAC
B
C4T07 SUB
BGEZ
C4T05 ADD
BGEZ
EXP4 LARK
LAC
B
EXP5 LARK
LAC
B

TEMP4 ; -1 if neg: 0 if positive (DS)
TEMP1 ; binary search to get exponent
ONE:8
C8T01:4
M15:4 ; TEMP1-16 exp = 0-7
C4T07
THREE:2 ; TEMP1-4 exp = 0-3
C2T03
ONE:1 ; TEMP1-2 exp = 0-1
EXP1
0:0 ; exp = 0
TEMP1:7
GETMAN ; save exponent and get mantissa
B
0:1 ; exp = 1
TEMP1:6
GETMAN
ONE:2 ; TEMP1-8 exp = 2-3
EXP3
0:2 ; exp = 2
TEMP1:5
GETMAN
0:3 ; exp = 3
TEMP1:4
GETMAN
THREE:4 ; TEMP1-64 exp = 4-7
C6T07
ONE:5 ; TEMP1-32 exp = 4-5
EXP5
0:4 ; exp = 4
TEMP1:3
GETMAN
0:5 ; exp = 5
TEMP1:2
GETMAN

```

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C6T07 SUB      ONE,6      ; TEMP1-128      exp = 6-7
BGEZ      EXP7

EXP6 LARK      0,6      ; exp = 6
EXP6 LAC      TEMP1,1
EXP6 B      GETMAN

EXP7 LARK      0,7      ; exp = 7
EXP7 LAC      TEMP1
EXP7 B      GETMAN

C8T014 SUB      M15,8      ; TEMP1-4096      exp = 8-14
BGEZ      CCTOE

C8T011 ADD      THREE,10 ; TEMP1-1024      exp = 8-11
BGEZ      CATOB

C8T09 ADD      ONE,9      ; TEMP1-512      exp = 8-9
BGEZ      EXP9

EXP8 LARK      0,8      ; exp = 8
EXP8 LAC      TEMP1,15
EXP8 SACH      TEMP1
EXP8 B      GETMAN

EXP9 LARK      0,9      ; exp = 9
EXP9 LAC      TEMP1,14
EXP9 SACH      TEMP1
EXP9 B      GETMAN

CATOB SUB      ONE,10     ; TEMP1-2048      exp = 10-11
BGEZ      EXP11

EXP10 LARK      0,10     ; exp = 10
EXP10 LAC      TEMP1,13
EXP10 SACH      TEMP1
EXP10 B      GETMAN

EXP11 LARK      0,11     ; exp = 11
EXP11 LAC      TEMP1,12
EXP11 SACH      TEMP1
EXP11 B      GETMAN

CCTOE SUB      THREE,12  ; TEMP1-16384      exp = 12-14
BGEZ      EXP14

CCT00 ADD      ONE,13    ; TEMP1-8192      exp = 13-14
BGEZ      EXP13

EXP12 LARK      0,12     ; exp = 12
EXP12 LAC      TEMP1,11
EXP12 SACH      TEMP1
EXP12 LAC      TEMP1

```

```

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C0145 0315 F900      B      GETMAN
C0116 0321          EXP13 LARK      0,13      ; exp = 13
C0146 0317 7000      LAC      TEMP1,10
C0147 0318 2A21      SACH      TEMP1
C0148 0319 5821      LAC      TEMP1
C0149 031A 2021      LAC      TEMP1
C0150 031B F900      B      GETMAN
C0151 031C 0321      EXP14 LARK      0,14      ; exp = 14
C0152 031D 700E      LAC      TEMP1,9
C0153 031E 2921      SACH      TEMP1
C0154 031F 5821      LAC      TEMP1
C0155 0320 2021      LAC      TEMP1
C0156 0321 796F      GETMAN AND M127
C0157 0322 3021      SAR      0,TEMP1
C0158 0323 0721      ADD      TEMP1,7 ; DL 4e...7m (sign=SGN(0))
C0159          ;
C0160          ;
C0161          ;
C0162          ;
C0163          ;
C0164          ;
C0165 0324 0B4C      SUBTB ADD      ONE,11    ; offset by 2K
C0166 0325 1029      SUB      YOVR4
C0167          ;
C0168          ;
C0169          ;
C0170          ;
C0171          ;
C0172          ;
C0173          ;
C0174          ;
C0175 07F9          TAB1 EQU      2041      ; bottom of level 1
C0176 097B          TAB2 EQU      2161      ; bottom of level 2
C0177 09C3          TAB3 EQU      2265      ; bottom of level 3
C0178 0905          TAB4 EQU      2309      ; bottom of level 4
C0179 0936          TAB5 EQU      2358      ; bottom of level 5
C0180 0964          TAB6 EQU      2404      ; bottom of level 6
C0181 0995          TAB7 EQU      2453      ; bottom of level 7
C0182          ;
C0183 0326 107C      QUAN SUB      K2309     ; TEMP2-2309
C0184 0327 F000      BGEZ      C14T07
C0185 0328 033E      C10T03 ADD      K138     ; TEMP2-2171 I = 0-3
C0186 032A F000      BGEZ      C12T03
C0187 032C 007A      C10T01 ADD      K130     ; TEMP2-2041 I = 0-1
C0188 032D F000      BGEZ      IEQ1
C0189 032F 0332      IEQ0 LACK      0
C0190 0330 F900      B      GETIM
C0191 0331 0351      IEQ1 LACK      1
C0192 0332 7E01      LAC      B
C0193 0333 F500      GETIM
C0194 0334 0351      C12T03 SUB      K79      ; TEMP2-2250 I = 2-3
C0195 0335 1078      LAC      IEQ3
C0196 0336 F000

```



```

00170      Y  -- 13b unsigned (Q9)
00171      YU -- 13b unsigned (Q9)
00172
00173
00174
00175      FILTD      Y,12      ; Y (Q21)
00176      SUB       Y,7       ; Y/32 (Q21)
00177      ADD       W1,12      ; W1/32 (Q21)
00178      SACH      YU,4       ; YU (Q9)
00179
00180      ; limit quant scale factor 1.06 <= YU <= 10.0
00181
00182      LIMB      SUB      K544,12 ; check lo threshold
00183      BGEZ     CHKHI
00184
00185      LAC      K544
00186      STRLIM   B
00187
00188      CHKHI    SUB      K4576,12 ; check hi threshold
00189      BLEZ     FILTE
00190
00191      LAC      K5120
00192      STRLIM   SACH      YU
00193
00194      ; Update slow adaptation scale factor
00195
00196      YL(k) = (1-2**(-6))*YL(k-1) + 2**(-6) * YU(k)
00197
00198      INPUT: SLOW QUANTIZER SCALE FACTOR -- YL (YLL/YLH)
00199      FAST QUANTIZER SCALE FACTOR -- YU
00200
00201      OUTPUT: SLOW QUANTIZER SCALE FACTOR -- YL (YLL/YLH)
00202
00203      NOTATION: YU -- 13b unsigned (Q9)
00204      YL -- 19b unsigned (Q15)
00205      stored as:
00206      low 15b -- YLL
00207      hi 4b -- YLH
00208
00209      FILTE      YLH,6      ; shift y1 left by 6
00210      SACH      TEMPI,15   ; YL (Q21)
00211      ADD      YLL,6
00212      SUB      YLH,15
00213      SACH      YU,6
00214      ADD      YU,6
00215      SACH      TEMPI,1
00216      AND      M32757
00217      SACH      TEMPI,2
00218      LAC      TEMPI,10
00219      SACH      TEMPI,9
00220      ADD      TEMPI,9
00221      SACH      YLH,1
00222
00223
00224      ; ADAPTATION SPEED CONTROL
00225
00226      INPUT: ADPCM SAMPLE -- I
00227
00228      OUTPUT: UNLIMITED SPEED CONTROL -- AP (APP)
00229
00230      NOTATION: I -- 4b SM (Q0)
00231      APP -- 10b unsigned (Q8)
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00224      00224 039A 7974
00225      00225 039B 504A
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CCITT      32010 FAMILY MACRO ASSEMBLER      PC2.1 84.107      16:36:03 03-20-85
                                           PAGE 0037

D0502 0415 7F88 LIMC ABS
D0503 0416 1C70 SUB THREE.12
D0504 0417 FB00 BLEZ LIMD
D0505 0418 0410
D0506 0419 2C70 LAC THREE.12
D0507 041A 7821 XOR ; 1's complement if negative
D0508 041B 1021 SUB ; 2's complement if negative
D0509 041C 5012 DONEC SACL A2 ; Q14
D0510
D0511 ; limit A1(k) to +/- [1-2**4 - A2(k)]
D0512 LIMD LAC M15.10 ; 1-2**4 (Q14)
D0513 041E 1012 SUB A2
D0514 041F 5021 SACL TEMP1 ; 1-2**4-A2P (Q14)
D0515 0420 2011 LAC A1
D0516 0421 5824 SACH TEMP4 ; save sign to make +/- LIMIT
D0517 0422 7F88 ABS
D0518 0423 1021 SUB
D0519 0424 FB00 BLEZ FLTSR
D0520 0425 042A
D0521 0426 2021 AILIM LAC
D0522 0427 7824 XOR TEMP4 ; ABS value of LIMIT
D0523 0428 1024 SUB TEMP4 ; 1's complement if negative
D0524 0429 5011 SACL A1 ; 2's complement if negative
D0525
D0526 ; COMPUTE RECONSTRUCTED SIGNAL
D0527
D0528 ; INPUT: QUANTIZED DIFFERENCE SIGNAL -- DQ
D0529 ; SIGNAL ESTIMATE -- SE
D0530
D0531 ; OUTPUT: RECONSTRUCTED SIGNAL -- SR
D0532
D0533 ; NOTATION: DQ -- 15b TC (00) [sign extended]
D0534 ; SE -- 15b TC (00) [sign extended]
D0535 ; SR -- 16b TC (00)
D0536
D0537 ; FLOAT SR -- convert 2's comp number to floating
D0538 ; INPUT: accumulator
D0539
D0540 ; OUTPUT: --4b exponent left in SREXP
D0541 ; --6b mantissa*8 left in SRMAN
D0542 ; --sign preserved in SR
D0543
D0544 ;
D0545 ;
D0546 ;
D0547
D0548 042A 2010 FLTSR LAC ; compute reconstructed signal
D0549 042B 0003 ADD SE
D0550 042C 5013 SACL SR
D0551 042D 7F88 ABS
D0552 042E 5052 SACL SRMAN ; convert to floating point notation
D0553 042F 174C SUB ONE.7 ; binary search to get exponent
D0554 0430 F000 BGEZ DBTOF
D0555 0431 0469
D0556 0432 0360 D01T07 ADD M15.3 ; TEMP1-8 -- exp = 0-7

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CCITT      32010 FAMILY MACRO ASSEMBLER      PC2.1 84.107      16:36:03 03-20-85
                                           PAGE 0038

D0556 0433 FD00 BGEZ D4T07
D0557 0434 044A D0T03 ADD THREE.1 ; TEMP1-2 -- exp = 0-3
D0558 0436 FD00 BGEZ D2T03
D0559 0438 2052 D0T01 LAC SRMAN ; exp = 0-1
D0560 0439 501C SACL SREXP
D0561 043A 284C LAC ONE.8
D0562 043B 5052 SACL SRMAN
D0563 043C 7F8D RET
D0564 043D 114C D2T03 SUB ONE.1 ; TEMP1-4 -- exp = 2-3
D0565 043E FD00 BGEZ EXX3
D0566 0440 2752 EXX2 LAC SRMAN.7 ; exp=2
D0567 0441 5052 SACL SACL 2
D0568 0442 7E02 LACK SACL SREXP
D0569 0443 501C SACL SREXP
D0570 0444 7F8D RET
D0571 0445 2652 EXX3 LAC SRMAN.6 ; exp=3
D0572 0446 5052 SACL SACL 3
D0573 0447 7E03 LACK SACL SREXP
D0574 0448 501C SACL SREXP
D0575 0449 7F8D RET
D0576 044A 137D D4T07 SUB THREE.3 ; TEMP1-32 -- exp = 4-7
D0577 044B FD00 BGEZ D6T07
D0578 044D 045A D4T05 ADD ONE.4 ; TEMP1-16 -- exp = 4-5
D0579 044E FD00 BGEZ EXX5
D0580 0450 2352 EXX4 LAC SRMAN.5 ; exp=4
D0581 0451 5052 SACL SACL 4
D0582 0452 7E04 LACK SACL SREXP
D0583 0453 501C SACL SREXP
D0584 0454 7F8D RET
D0585 0455 2452 EXX5 LAC SRMAN.4 ; exp=5
D0586 0456 7E02 SACL SACL 5
D0587 0457 7E03 LACK SACL SREXP
D0588 0458 501C SACL SREXP
D0589 0459 7F8D RET
D0590 045A 154C D6T07 SUB ONE.5 ; TEMP1-64 -- exp = 6-7
D0591 045B FD00 BGEZ EXX7
D0592 045D 2352 EXX6 LAC SRMAN.3 ; exp=6
D0593 045E 5052 SACL SACL 6
D0594 045F 7E06 LACK SACL SREXP
D0595 0460 501C SACL SREXP
D0596 0461 7F8D RET
D0597 0462 2F52 EXX7 LAC SRMAN.15
D0598 0463 5852 SACH SRMAN
D0599 0464 2352 LAC SRMAN.3
D0600 0465 5052 SACL SRMAN
D0601 0466 7E07 LACK SACL 7
D0602 0467 501C SACL SREXP
D0603 0468 7F8D RET
D0604 0469 1177 D8TOF SUB K960.1 ; TEMP1-2048 -- exp = 8-15
D0605 046A FD00 BGEZ DCTOF
D0606 046B 0491

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; TEMPI-16384 -- exp=14-15

D0606	046C	097D	D8T0B	ADD	BGEZ	THREE,9 ;	TEMP1-512 --	exp = 8-11	CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0039	
D0607	046D	F000	D8T0B	ADD	BGEZ	DAT0B	THREE,9 ;	TEMP1-512 --	exp = 8-11	CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0039
D0608	046E	084C	D8T09	ADD	BGEZ	ONE,8 ;	TEMP1-256 --	exp = 8-9	CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0609	046F	094C	D8T09	ADD	BGEZ	EXX9	ONE,8 ;	TEMP1-256 --	exp = 8-9	CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040
D0610	0471	0479	EXX8	LAC	SRMAN,14 ;	exp=8	SRMAN,14 ;	exp=8	CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0611	0472	2E52	LAC	SACH	SRMAN		SRMAN		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0612	0473	2352	LAC	SRMAN,3	SRMAN,3		SRMAN,3		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0613	0475	5052	SACL	SRMAN	SRMAN		SRMAN		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0614	0476	7E08	LACK	8	SRMAN		SRMAN		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0615	0477	501C	SACL	SREXP	SRMAN		SRMAN		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0616	0478	7F80	RET	SRMAN,13 ;	exp=9	SRMAN,13 ;	exp=9		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0617	0479	2D52	LAC	SRMAN	SRMAN		SRMAN		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0618	047A	5852	SACH	SRMAN,3	SRMAN,3		SRMAN,3		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0619	047B	2352	LAC	SRMAN	SRMAN		SRMAN		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0620	047C	5052	SACL	SRMAN	SRMAN		SRMAN		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0621	047D	7E09	LACK	9	SRMAN		SRMAN		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0622	047E	501C	SACL	SREXP	SRMAN		SRMAN		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0623	047F	7F80	RET	ONE,9 ;	TEMP1-1024 --	exp=10-11	ONE,9 ;	TEMP1-1024 --	exp=10-11	CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040
D0624	0480	194C	SUB	EXX11			EXX11		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0625	0481	F000	BGEZ	LAC	SRMAN,12 ;	exp=10	SRMAN,12 ;	exp=10	CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0626	0482	2D52	EXX10	LAC	SRMAN		SRMAN		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0627	0483	2D52	SACH	SRMAN	SRMAN		SRMAN		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0628	0485	2352	LAC	SRMAN,3	SRMAN,3		SRMAN,3		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0629	0486	5052	SACL	SRMAN	SRMAN		SRMAN		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0630	0487	7E0A	LACK	10	SRMAN		SRMAN		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0631	0488	501C	SACL	SREXP	SRMAN		SRMAN		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0632	0489	7F80	RET	SRMAN,11 ;	exp=11	SRMAN,11 ;	exp=11		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0633	048A	2B52	LAC	SRMAN	SRMAN		SRMAN		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0634	048B	5852	SACH	SRMAN,3	SRMAN,3		SRMAN,3		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0635	048C	2352	LAC	SRMAN	SRMAN		SRMAN		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0636	048D	5052	SACL	SRMAN	SRMAN		SRMAN		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0637	048E	7E0B	LACK	11	SRMAN		SRMAN		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0638	048F	501C	SACL	SREXP	SRMAN		SRMAN		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0639	0490	7F80	RET	THREE,11 ;	TEMP1-8192 --	exp=12-15	THREE,11 ;	TEMP1-8192 --	exp=12-15	CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040
D0640	0491	1B7D	SUB	DETOF			DETOF		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0641	0492	F000	BGEZ	ONE,12 ;	TEMP1-4096 --	exp=12-13	ONE,12 ;	TEMP1-4096 --	exp=12-13	CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040
D0642	049A	0C4C	ADD	EXX13			EXX13		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0643	0494	F000	BGEZ	SRMAN,10 ;	exp=12	SRMAN,10 ;	exp=12		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0644	0497	2A52	LAC	SRMAN	SRMAN		SRMAN		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0645	0498	5852	SACH	SRMAN,3	SRMAN,3		SRMAN,3		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0646	0499	2352	LAC	SRMAN	SRMAN		SRMAN		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0647	049A	5052	SACL	SRMAN	SRMAN		SRMAN		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0648	049B	7E0C	LACK	12	SRMAN		SRMAN		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0649	049C	501C	SACL	SREXP	SRMAN		SRMAN		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0650	049D	7F80	RET	SRMAN,9 ;	exp=13	SRMAN,9 ;	exp=13		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0651	049E	2952	LAC	SRMAN	SRMAN		SRMAN		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0652	049F	5852	SACH	SRMAN,3	SRMAN,3		SRMAN,3		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0653	04A0	2352	LAC	SRMAN	SRMAN		SRMAN		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0654	04A1	5052	SACL	SRMAN	SRMAN		SRMAN		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0655	04A2	7E0D	LACK	13	SRMAN		SRMAN		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0656	04A3	501C	SACL	SREXP	SRMAN		SRMAN		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0657	04A4	7F80	RET	ONE,13 ;	TEMP1-16384 --	exp=14-15	ONE,13 ;	TEMP1-16384 --	exp=14-15	CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040
D0658	04A5	1D4C	DETOF	SUB	BGEZ	ONE,13 ;	TEMP1-16384 --	exp=14-15	CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0659	04A6	F000	BGEZ	EXX15			EXX15		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0660	04A8	2B52	LAC	SRMAN,8 ;	exp=14	SRMAN,8 ;	exp=14		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0661	04A9	5852	SACH	SRMAN	SRMAN		SRMAN		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0662	04AA	2352	LAC	SRMAN,3	SRMAN,3		SRMAN,3		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0663	04AB	5052	SACL	SRMAN	SRMAN		SRMAN		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0664	04AC	7E0E	LACK	14	SRMAN		SRMAN		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0665	04AD	501C	SACL	SREXP	SRMAN		SRMAN		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0666	04AE	7F80	RET	SRMAN,7 ;	exp=15	SRMAN,7 ;	exp=15		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0667	04AF	2752	LAC	SRMAN	SRMAN		SRMAN		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0668	04B0	5852	SACH	SRMAN	SRMAN		SRMAN		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0669	04B1	2352	LAC	SRMAN,3	SRMAN,3		SRMAN,3		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0670	04B2	5052	SACL	SRMAN	SRMAN		SRMAN		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0671	04B3	7E0F	LACK	15	SRMAN		SRMAN		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0672	04B4	501C	SACL	SREXP	SRMAN		SRMAN		CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040	
D0673	04B5	7F80	RET	ONE,15 ;	TEMP1-16384 --	exp=16-19	ONE,15 ;	TEMP1-16384 --	exp=16-19	CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03	03-20-85	PAGE 0040

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COPY      UTILITY.ASM
*;* code to do left shifts for SEZ/SE calculations
*;*
RS1  ABS      04B6 7F8B      ; make positive before mask
AND    M32767      ; keep lower 15 bits
SACL   SUM1      ; save result
B      CHK1      ; return

RS2  ABS      04B8 7F8B
AND    M32767
SACL   SUM2
B      CHK2

RS3  ABS      04C0 7F8B
AND    M32767
SACL   SUM3
B      CHK3

RS4  ABS      04C5 7F8B
AND    M32767
SACL   SUM4
B      CHK4

RS5  ABS      04CA 7F8B
AND    M32767
SACL   SUM5
B      CHK5

RS6  ABS      04CF 7F8B
AND    M32767
SACL   SUM6
B      CHK6

RS11 ABS      04D4 7F8B
AND    M32767
SACL   SUM7
B      CHK11

RS21 ABS      04D9 7F8B
AND    M32767
SACL   SUM8
B      CHK21

04DD 0279

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*;*-----convert 2's comp number to floating
*;* INPUT: accumulator
*;* OUTPUT:
*;*      --4b exponent left in accum
*;*      --6b mantissa left in TEMP1
*;*      --sign preserved in original number
*;*-----
*;*      ; address of shift multipliers
002A  FLTSFT EQU 42
*;*
*;*      TEMP1
*;*      LAC SACH
*;*      TEMP1
*;*      ABS
*;*      SACL
*;*      TEMP1
*;*      ONE,6      ; binary search to get exponent
*;*      SUB
*;*      BGEZ E7T00
*;*
*;*      ADD
*;*      K56      ; TEMP1-8 --- exp = 0-6
*;*      E4T06
*;*      BGEZ
*;*
*;*      ADD
*;*      THREE,1 ; TEMP1-2 --- exp = 0-3
*;*      E2T03
*;*
*;*      LAC
*;*      TEMP1 ; exp = 0-1
*;*      BNZ E1
*;*
*;*      ONE,5      ; exp=0
*;*      LAC
*;*      TEMP1
*;*      FLTSFT+0
*;*      LACK
*;*      RET
*;*
*;*      TEMP1,5 ; exp=1
*;*      LAC
*;*      TEMP1
*;*      FLTSFT+1
*;*      LACK
*;*      RET
*;*
*;*      ONE,1 ; TEMP1-4 --- exp = 2-3
*;*      E3
*;*      E2T03
*;*      SUB
*;*      BGEZ
*;*
*;*      TEMP1,4 ; exp=2
*;*      LAC
*;*      TEMP1
*;*      FLTSFT+2
*;*      LACK
*;*
*;*      TEMP1,3 ; exp=3
*;*      RET
*;*      LAC
*;*      TEMP1
*;*      FLTSFT+3
*;*      LACK
*;*      RET
*;*
*;*      ONE,3 ; TEMP1-16 --- exp = 4-6
*;*      E5T06
*;*      BGEZ
*;*
*;*      TEMP1,2 ; exp=4
*;*      LAC
*;*      TEMP1
*;*      FLTSFT+4
*;*      LACK
*;*
*;*      ONE,4 ; TEMP1-32 --- exp = 5-6
*;*      E6
*;*      E5T06
*;*      SUB
*;*      BGEZ

```

CCITT	32010	FAMILY	MACRO_ASSEMBLER	PC2.1	84.107	16:36:03	03-20-86	PAGE	0043
E5	050A	050F							
	EO088	050B	2121	LAC	TEMP1,1 ; exp=5				
	EO089	050C	5021	SACL	TEMP1				
	EO090	050D	7E2F	LACK	FLTSFT+5				
	EO091	050E	7F80	RET					
	EO092	050F	7E30	LACK	FLTSFT+6 ; exp=6				
	EO093	0510	7F80	RET					
	EO094	0511	1077	ET700	SUB	K960 ; TEMP1-1024 -- exp = 7-13			
	EO095	0512	F000	BGEZ	EBT00				
	EO096	0514	0870	ADD	THREE,8 ; TEMP1-256 -- exp = 7-10				
	EO097	0515	F000	BGEZ	E9T0A				
	EO098	0517	074C	ADD	ONE,7 ; TEMP1-128 -- exp = 7-8				
	EO099	0518	F000	BGEZ	EB				
	EO100	0519	051E						
	EO101	051A	2F21	LAC	TEMP1,15 ; exp=7				
	EO102	051B	5821	SACH	TEMP1				
	EO103	051C	7E31	LACK	FLTSFT+7				
	EO104	051D	7F80	RET					
	EO105	051F	5821	LAC	TEMP1,14 ; exp=8				
	EO106	0520	7E32	SACH	TEMP1				
	EO107	0521	7F80	LACK	FLTSFT+8				
E9	EO108	0522	184C	RET					
	EO109	0523	F000	SUB	ONE,8 ; TEMP1-512 -- exp = 9-10				
	EO110	0524	0529	BGEZ	E10				
	EO111	0525	2021	LAC	TEMP1,13 ; exp=9				
	EO112	0526	5821	SACH	TEMP1				
	EO113	0527	7E33	LACK	FLTSFT+9				
	EO114	0528	7F80	RET					
	EO115	0529	2C21	LAC	TEMP1,12 ; exp=10				
	EO116	052A	5821	SACH	TEMP1				
	EO117	052C	7E34	LACK	FLTSFT+10				
	EO118	052D	1A70	RET					
	EO119	052E	F000	SUB	THREE,10 ; TEMP1-4096 -- exp=11-13				
	EO120	0530	0538	BGEZ	EDT0E				
	EO121	0531	F000	ADD	ONE,11 ; TEMP1-2048 -- exp=11-12				
	EO122	0532	2027	BGEZ	E12				
	EO123	0533	5821	LAC	TEMP1,11 ; exp=11				
	EO124	0535	7E35	SACH	TEMP1				
	EO125	0536	7E80	LACK	FLTSFT+11				
	EO126	0537	2A21	RET					
	EO127	0538	5821	LAC	TEMP1,10 ; exp=12				
	EO128	0539	7E36	SACH	TEMP1				
	EO129	053A	7F80	LACK	FLTSFT+12				
E13	EO130	053B	1C4C	RET					
	EO131	053C	F000	SUB	ONE,12 ; TEMP1-8192 -- exp=0				
	EO132	053D	04E	BGEZ	E0				
	EO133	053E	2921	LAC	TEMP1,9 ; exp=13				
	EO134	053F	5821	SACH	TEMP1				
	EO135	0540	7E37	LACK	FLTSFT+13				
	EO136	0541	7F80	RET					

```

0006          COPY      INIT,ASM
F0001          *;*****
F0002          *; SYSTEM INITIALIZATION
F0003          *;*****
F0004          004A      NOCONS EQU 74
F0005          0036      PTCONS EQU 54
F0006          *;
F0007          0542 7F81 RESET DINT
F0008          F0008 0543 6E00 ; Disable interrupts
F0009          *; ; Initialize data page
F0010          0544 7035 SETPAC LARK 0.53
F0011          0545 6880 LARP 0
F0012          0546 7F89 ZAC
F0013          0547 5080 ZRAHA *0.0
F0014          0548 F400 BANZ
F0015          0549 0547 *;
F0016          054A 7E01 LACK
F0017          054B 504C SACL
F0018          054C 6A4C LT ONE
F0019          054D 8598 MPYK CONS
F0020          054E 7F8E PAC
F0021          054F 7136 LARK
F0022          0550 7049 LARK
F0023          0551 6881 NXCONS
F0024          0552 67A0 TBLR
F0025          0553 004C ADD *+,0
F0026          0554 F400 BANZ
F0027          0555 0551 *;
F0028          0556 4021 IN
F0029          0557 2021 LAC
F0030          0558 F400 BLZ
F0031          0559 055E MULAW
F0032          055A FF00 BZ
F0033          055B 0020 B
F0034          055C F000
F0035          055D 00F9
F0036          055E 7974 ALAW
F0037          055F FF00 AND
F0038          0560 004E BZ
F0039          0561 F900 B
F0040          0562 0184 *;
F0041          *;
F0042          *;
F0043          *;
F0044          *;
F0045          *;
F0046          *;
F0047          *;
F0048          *;
F0049          *;
F0050          *;
F0051          *;
F0052          *;
F0053          *;
F0054          *;
F0055          *;
F0056          *;
F0057          *;
F0058          *;
F0059          *;
F0060          *;
F0061          *;
F0062          *;
F0063          *;
F0064          *;
F0065          *;
F0066          *;
F0067          *;
F0068          *;
F0069          *;
F0070          *;
F0071          *;
F0072          *;
F0073          *;
F0074          *;
F0075          *;
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F0078          *;
F0079          *;
F0080          *;
F0081          *;
F0082          *;
F0083          *;
F0084          *;
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F0087          *;
F0088          *;
F0089          *;
F0090          *;
F0091          *;
F0092          *;
F0093          *;
F0094          *;
F0095          *;
F0096          *;
F0097          *;
F0098          *;
F0099          *;
F0100          *;
F0101          *;
F0102          *;
F0103          *;
F0104          *;
F0105          *;
F0106          *;
F0107          *;
F0108          *;
F0109          *;
F0110          *;
F0111          *;
F0112          *;
F0113          *;
F0114          *;
F0115          *;
F0116          *;
F0117          *;
F0118          *;
F0119          *;
F0120          *;
F0121          *;
F0122          *;
F0123          *;
F0124          *;
F0125          *;
F0126          *;
F0127          *;
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F0134          *;
F0135          *;
F0136          *;
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F0144          *;
F0145          *;
F0146          *;
F0147          *;
F0148          *;
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F0150          *;
F0151          *;
F0152          *;
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F0158          *;
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F0160          *;
F0161          *;
F0162          *;
F0163          *;
F0164          *;
F0165          *;
F0166          *;
F0167          *;
F0168          *;
F0169          *;
F0170          *;
F0171          *;
F0172          *;
F0173          *;
F0174          *;
F0175          *;
F0176          *;
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F0179          *;
F0180          *;
F0181          *;
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F0187          *;
F0188          *;
F0189          *;
F0190          *;
F0191          *;
F0192          *;
F0193          *;
F0194          *;
F0195          *;
F0196          *;
F0197          *;
F0198          *;
F0199          *;
F0200          *;
F0201          *;
F0202          *;
F0203          *;
F0204          *;
F0205          *;
F0206          *;
F0207          *;
F0208          *;
F0209          *;
F0210          *;
F0211          *;
F0212          *;
F0213          *;
F0214          *;
F0215          *;
F0216          *;
F0217          *;
F0218          *;
F0219          *;
F0220          *;
F0221          *;
F0222          *;
F0223          *;
F0224          *;
F0225          *;
F0226          *;
F0227          *;
F0228          *;
F0229          *;
F0230          *;
F0231          *;
F0232          *;
F0233          *;
F0234          *;
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F0257          *;
F0258          *;
F0259          *;
F0260          *;
F0261          *;
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F0266          *;
F0267          *;
F0268          *;
F0269          *;
F0270          *;
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F0275          *;
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F0292          *;
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F0295          *;
F0296          *;
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F0299          *;
F0300          *;
F0301          *;
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F0303          *;
F0304          *;
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F0312          *;
F0313          *;
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F0318          *;
F0319          *;
F0320          *;
F0321          *;
F0322          *;
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F0327          *;
F0328          *;
F0329          *;
F0330          *;
F0331          *;
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F0333          *;
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F0336          *;
F0337          *;
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F0381          *;
F0382          *;
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F0388          *;
F0389          *;
F0390          *;
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F0397          *;
F0398          *;
F0399          *;
F0400          *;
F0401          *;
F0402          *;
F0403          *;
F0404          *;
F0405          *;
F0406          *;
F0407          *;
F0408          *;
F0409          *;
F0410          *;
F0411          *;
F0412          *;
F0413
```



```
0007      COPY      ROMRAN.ASM
00001      *;
00002      *; *****
00003      *; *****
00004      *; *****
00005      *; *****
00006      *; *****
00007      *; *****
00008      *; *****
00009      *; *****
00010      *; *****
00011      *; *****
00012      *; *****
00013      *; *****
00014      *; *****
00015      *; *****
00016      *; *****
00017      *; *****
00018      *; *****
00019      *; *****
00020      *; *****
00021      *; *****
00022      *; *****
00023      *; *****
00024      *; *****
00025      *; *****
00026      *; *****
00027      *; *****
00028      *; *****
00029      *; *****
00030      *; *****
00031      *; *****
00032      *; *****
00033      *; *****
00034      *; *****
00035      *; *****
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00037      *; *****
00038      *; *****
00039      *; *****
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00041      *; *****
00042      *; *****
00043      *; *****
00044      *; *****
00045      *; *****
00046      *; *****
00047      *; *****
00048      *; *****
00049      *; *****
00050      *; *****
00051      *; *****
00052      *; *****
00053      *; *****
00054      *; *****
00055      *; *****
00056      *; *****
```

```
00057 058F 0062      DATA 98
00058 0590 00B8      DATA 184
00059 0591 0154      DATA 340
00060 0592 0454      DATA 1108
00061      *; FI TABLE
00062      FITABL BSS 0
00063 0593      BSS 0
00064 0594      BSS 0
00065 0594 0000      DATA 0
00066 0595 0000      DATA 0
00067 0596 0010      DATA 16
00068 0597 0010      DATA 16
00069 0598 0010      DATA 16
00070 0599 0030      DATA 48
00071 059A 0070      DATA 112
00072      *; misc constants to be initialized
00073      *;
00074      *;
00075 059B 0002      BSS 0
00076 059B 0002      DATA 2
00077 059C 0004      DATA 4
00078 059D 0008      DATA 8
00079 059E 0010      DATA 16
00080 059F 0020      DATA 32
00081 05A0 0040      DATA 64
00082 05A1 0080      DATA 128
00083 05A2 0100      DATA 192
00084 05A3 0200      DATA 384
00085 05A4 0400      DATA 768
00086 05A5 0800      DATA 1536
00087 05A6 1600      DATA 3072
00088 05A7 2000      DATA 4096
00089 05A8 4000      DATA 8192
00090 05A9 FFFF      DATA 16384
00091 05AA FFFF      DATA -1
00092 05AB FFFF      DATA -2
00093 05AC FFFF      DATA -4
00094 05AD 00FF      DATA 255
00095 05AE 8000      DATA 32768
00096 05AF 0800      DATA 1
00097 05B0 FFFF      DATA 2048
00098 05B1 0001      DATA -1
00099 05B2 0021      DATA 1
00100 05B3 0020      DATA 33
00101 05B4 0200      DATA 544
00102 05B5 0200      DATA 512
00103 05B6 0200      DATA 512
00104 05B7 0100      DATA 256
00105 05B8 0100      DATA 256
00106 05B9 0800      DATA 2048
00107 05BA 0800      DATA 2048
00108 05BB 0800      DATA 2048
00109 05BC 0800      DATA 2048
00110 05BD 0800      DATA 2048
00111 05BE 0800      DATA 2048
00112 05BF 0800      DATA 2048
00113 05C0 0100      DATA 256
```

CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03 03-20-85	PAGE 0047
G0114 05C1 0100	:DQJMAN			
G0115 05C2 0100	:DQZMAN			
G0116 05C3 0100	:DQJMAN			
G0117 05C4 0100	:DQJMAN			
G0118 05C5 0100	:DQJMAN			
G0119 05C6 11E0	:K4576			
G0120 05C7 3FFE	:K16382			
G0121 05C8 C002	:M16382			
G0122 05C9 002E	:K46			
G0123 05CA 0031	:K49			
G0124 05CB 0563	:SHIFT			
G0125 05CC 003F	:K63			
G0126 05CD 0000	:SHIFT			
G0127 05CE 0000	:FI			
G0128 05CF 0583	:IQTAB			
G0129 05D0 0220	:K544			
G0130 05D1 1400	:K5120			
G0131 05D2 000F	:M15			
G0132 05D3 FF80	:KFF80			
G0133 05D4 007F	:K127			
G0134 05D5 FFC0	:MFFC0			
G0135 05D6 1080	:BIAS*2**7			
G0136 05D7 0FFF	:M4095			
G0137 05D8 0000	:spare			
G0138 05D9 7FFF	:K32767			
G0139 05DA FF00	:KFF00			
G0140 05DB 0038	:K56			
G0141 05DC 0040	:K580			
G0142 05DD 004F	:K79			
G0143 05DE 005F	:K95			
G0144 05DF 0082	:K130			
G0145 05E0 008A	:K138			
G0146 05E1 0905	:K2309			
G0147 05E2 0003	:THREE			
G0148 05E3 0000	:spare			
G0149 05E4 0080	:M0080			
	128			

CCITT	32010 FAMILY MACRO ASSEMBLER	PC2.1 84.107	16:36:03 03-20-85	PAGE 0048
G0151	:RAM			
G0152	:RAMLOC BSS			
G0153	:DORG			
G0154 05E5	:RAM Location # 000			
G0155	:DATA			
G0156	:RAM Location # 001			
G0157	:DATA			
G0158 0000 0000	:RAM Location # 002			
G0159	:DATA			
G0160	:RAM Location # 003			
G0161 0001 0000	:DATA			
G0162	:RAM Location # 004			
G0163	:DATA			
G0164 0002 0000	:RAM Location # 005			
G0165	:DATA			
G0166	:RAM Location # 006			
G0167 0003 0000	:DATA			
G0168	:RAM Location # 007			
G0169	:DATA			
G0170 0004 0000	:RAM Location # 008			
G0171	:DATA			
G0172	:RAM Location # 009			
G0173 0005 0000	:DATA			
G0174	:RAM Location # 010			
G0175	:DATA			
G0176 0006 0000	:RAM Location # 011			
G0177	:DATA			
G0178	:RAM Location # 012			
G0179 0007 0000	:DATA			
G0180	:RAM Location # 013			
G0181	:DATA			
G0182 0008 0000	:RAM Location # 014			
G0183	:DATA			
G0184	:RAM Location # 015			
G0185 0009 0000	:DATA			
G0186	:RAM Location # 016			
G0187	:DATA			
G0188 000A 0000	:RAM Location # 017			
G0189	:DATA			
G0190	:RAM Location # 018			
G0191 000B 0000	:DATA			
G0192	:RAM Location # 019			
G0193	:DATA			
G0194 000C 0000	:RAM Location # 020			
G0195	:DATA			
G0196	:RAM Location # 021			
G0197 000D 0000	:DATA			
G0198	:RAM Location # 022			
G0199	:DATA			
G0200 000E 0000	:RAM Location # 023			
G0201	:DATA			
G0202	:RAM Location # 024			
G0203 000F 0000	:DATA			
G0204	:RAM Location # 025			
G0205	:DATA			
G0206 0010 0000	:RAM Location # 026			
G0207	:DATA			

```

G0208      ; RAM Location # 017
G0209 A1 DATA 0 ; coefficients of 2nd order predictor
G0210 ;
G0211 ; RAM Location # 018
G0212 A2 DATA 0 ; coefficients of 2nd order predictor
G0213 ;
G0214 ; RAM Location # 019
G0215 S1 DATA 0 ; reconstructed signal frame k
G0216 ;
G0217 ; RAM Location # 020
G0218 S1 DATA 0 ; reconstructed signal frame k
G0219 ;
G0220 ; RAM Location # 021
G0221 DQEXP DATA 0 ; exponent of DQ
G0222 ;
G0223 ; RAM Location # 022
G0224 DQ1EXP DATA 0 ; exponent of DQ1
G0225 ;
G0226 ; RAM Location # 023
G0227 DQ2EXP DATA 0 ; exp of DQ2
G0228 ;
G0229 ; RAM Location # 024
G0230 DQ3EXP DATA 0 ; exp of DQ3
G0231 ;
G0232 ; RAM Location # 025
G0233 DQ4EXP DATA 0 ; exp of DQ4
G0234 ;
G0235 ; RAM Location # 026
G0236 DQ5EXP DATA 0 ; exp of DQ5
G0237 ;
G0238 ; RAM Location # 027 ; scratch variable
G0239 ;
G0240 ; RAM Location # 028 ; exp of SR
G0241 ;
G0242 SREXP DATA 0 ; exp of SR
G0243 ;
G0244 ; RAM Location # 029 ; exp of SRI
G0245 SRIEXP DATA 0 ; exp of SRI
G0246 ;
G0247 ; RAM Location # 030 ; temp
G0248 SUM4 DATA 0 ; temp
G0249 ;
G0250 ; RAM Location # 031 ; temp
G0251 SUM5 DATA 0 ; temp
G0252 ;
G0253 ; RAM Location # 032 ; temp
G0254 SUM6 DATA 0 ; temp
G0255 ;
G0256 ; RAM Location # 033 ; temp
G0257 TEMP1 DATA 0 ; temp
G0258 ;
G0259 ; RAM Location # 034 ; temp
G0260 SUM1 BSS 0 ; temp
G0261 TEMP2 DATA 0 ; temp
G0262 ;
G0263 ; RAM Location # 035 ; temp
G0264 SUM2 BSS 0 ; temp

```

```

G0265 0023 0000 TEMP3 DATA 0 ; temp
G0266 ;
G0267 ; RAM Location # 036
G0268 TEMP4 DATA 0 ; temp
G0269 ;
G0270 ; RAM Location # 037
G0271 SUM3 DATA 0 ; temp
G0272 ;
G0273 ; RAM Location # 038 ; Linear sample
G0274 SAMPLE DATA 0 ; Linear sample
G0275 ;
G0276 ; RAM Location # 039 ; temp storage of SRI*A1 tap
G0277 SUM7 DATA 0 ; temp storage of SRI*A1 tap
G0278 ;
G0279 ; RAM Location # 040 ; temp storage of SR2*A2 tap
G0280 SUM8 DATA 0 ; temp storage of SR2*A2 tap
G0281 ;
G0282 ; RAM Location # 041 ; Y>>2
G0283 YOVER4 DATA 0 ; Y>>2
G0284 ;
G0285 ; RAM Location # 042 ; first location of shift table
G0286 002A 0000 DATA 0 ; first location of shift table
G0287 ;
G0288 ; RAM Location # 043
G0289 DATA 0 ;
G0290 ;
G0291 ; RAM Location # 044
G0292 DATA 0 ;
G0293 ;
G0294 ; RAM Location # 045
G0295 DATA 0 ;
G0296 ;
G0297 ; RAM Location # 046
G0298 DATA 0 ;
G0299 ;
G0300 ; RAM Location # 047
G0301 DATA 0 ;
G0302 ;
G0303 ; RAM Location # 048
G0304 DATA 0 ;
G0305 ;
G0306 ; RAM Location # 049
G0307 DATA 0 ;
G0308 ;
G0309 ; RAM Location # 050
G0310 DATA 0 ;
G0311 ;
G0312 ; RAM Location # 051
G0313 DATA 0 ;
G0314 ;
G0315 ; RAM Location # 052
G0316 DATA 0 ;
G0317 ;
G0318 ; RAM Location # 053
G0319 DATA 0 ;
G0320 ;
G0321 ; RAM Location # 054

```

```

G0322 0036 0000      DATA 0
G0323      *; RAM Location # 055
G0324      *; DATA 0
G0325 0037 0000      DATA 0
G0326      *; RAM Location # 056
G0327      *; EIGHT DATA 0
G0328 0038 0000      DATA 0
G0329      *; RAM Location # 057
G0330      *; DATA 0
G0331 0039 0000      DATA 0
G0332      *; RAM Location # 058
G0333      *; DATA 0
G0334 003A 0000      DATA 0
G0335      *; RAM Location # 059
G0336      *; DATA 0
G0337 003B 0000      DATA 0
G0338      *; RAM Location # 060
G0339      *; DATA 0
G0340 003C 0000      DATA 0
G0341      *; RAM Location # 061
G0342      *; DATA 0
G0343 003D 0000      DATA 0
G0344      *; RAM Location # 062
G0345      *; DATA 0
G0346 003E 0000      DATA 0
G0347      *; RAM Location # 063
G0348      *; DATA 0
G0349 003F 0000      DATA 0
G0350      *; RAM Location # 064
G0351      *; DATA 0
G0352 0040 0000      DATA 0
G0353      *; RAM Location # 065
G0354      *; DATA 0
G0355 0041 0000      DATA 0
G0356      *; RAM Location # 066
G0357      *; DATA 0
G0358 0042 0000      DATA 0
G0359      *; RAM Location # 067
G0360      *; DATA 0
G0361 0043 0000      DATA 0
G0362      *; RAM Location # 068
G0363      *; DATA 0
G0364 0044 0000      DATA 0
G0365      *; RAM Location # 069
G0366      *; DATA 0
G0367 0045 0000      DATA 0
G0368      *; RAM Location # 070
G0369      *; DATA 0
G0370 0046 0000      DATA 0
G0371      *; RAM Location # 071
G0372      *; M255 DATA 0
G0373 0047 0000      DATA 0
G0374      *; RAM Location # 072
G0375      *; K32768 DATA 0
G0376 0048 0000      DATA 0
G0377      *; RAM Location # 073

```

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G0379 0049 0000      YLH DATA 0      ; fast quant scale factor (hi word)
G0380      *; RAM Location # 074
G0381      *; YLL DATA 0      ; slow quant scale factor (lo word)
G0382 004A 0000      YLL DATA 0
G0383      *; RAM Location # 075
G0384      *; MINUS DATA 0      ; -1
G0385 004B 0000      MINUS DATA 0
G0386      *; RAM Location # 076
G0387      *; ONE DATA 0      ; 1
G0388 004C 0000      ONE DATA 0
G0389      *; RAM Location # 077
G0390      *; BIAS DATA 0      ; constant for mulaw conversions
G0391 004D 0000      BIAS DATA 0
G0392      *; RAM Location # 078
G0393      *; YU DATA 0      ; fast quant scale factor
G0394 004E 0000      YU DATA 0
G0395      *; RAM Location # 079
G0396      *; PK0 DATA 0      ; sign of p(k)
G0397 004F 0000      PK0 DATA 0
G0398      *; RAM Location # 080
G0399      *; PK1 DATA 0      ; sign of p(k-1)
G0400 0050 0000      PK1 DATA 0
G0401      *; RAM Location # 081
G0402      *; PK2 DATA 0      ; sign of p(k-2)
G0403 0051 0000      PK2 DATA 0
G0404      *; RAM Location # 082
G0405      *; SRMAN DATA 0      ; mantissa of SR
G0406 0052 0000      SRMAN DATA 0
G0407      *; RAM Location # 083
G0408      *; SRIMAN DATA 0      ; mantissa of SRI
G0409 0053 0000      SRIMAN DATA 0
G0410      *; RAM Location # 084
G0411      *; SDQ DATA 0      ; sign DQ(k)
G0412 0054 0000      SDQ DATA 0
G0413      *; RAM Location # 085
G0414      *; SDQ1 DATA 0      ; sign DQ(k-1)
G0415 0055 0000      SDQ1 DATA 0
G0416      *; RAM Location # 086
G0417      *; SDQ2 DATA 0      ; sign DQ(k-2)
G0418 0056 0000      SDQ2 DATA 0
G0419      *; RAM Location # 087
G0420      *; SDQ3 DATA 0      ; sign DQ(k-3)
G0421 0057 0000      SDQ3 DATA 0
G0422      *; RAM Location # 088
G0423      *; SDQ4 DATA 0      ; sign DQ(k-4)
G0424 0058 0000      SDQ4 DATA 0
G0425      *; RAM Location # 089
G0426      *; SDQ5 DATA 0      ; sign DQ(k-5)
G0427 0059 0000      SDQ5 DATA 0
G0428      *; RAM Location # 090
G0429      *; SDQ6 DATA 0      ; sign DQ(k-6)
G0430 005A 0000      SDQ6 DATA 0
G0431      *; RAM Location # 091
G0432      *; DQMAN DATA 0      ; mantissa of DQ
G0433 005B 0000      DQMAN DATA 0
G0434      *; RAM Location # 092
G0435      *;

```

; last loc of table (42-70)

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G0436 005C 0000 DQ1MAN DATA 0 ; mantissa of DQ1
G0437
G0438 *; RAM Location # 093
G0439 005D 0000 DQ2MAN DATA 0 ; mantissa of DQ2
G0440
G0441 *; RAM Location # 094
G0442 005E 0000 DQ3MAN DATA 0 ; mantissa of DQ3
G0443
G0444 *; RAM Location # 095
G0445 005F 0000 DQ4MAN DATA 0 ; mantissa of DQ4
G0446
G0447 *; RAM Location # 096
G0448 0060 0000 DQ5MAN DATA 0 ; mantissa of DQ5
G0449
G0450 *; RAM Location # 097
G0451 0061 0000 K4576 DATA 0 ; 4576
G0452
G0453 *; RAM Location # 098
G0454 0062 0000 K16382 DATA 0 ; +16382
G0455
G0456 *; RAM Location # 099
G0457 0063 0000 M16382 DATA 0 ; -16382
G0458
G0459 *; RAM Location # 100 ; 46
G0460 0064 0000 K46 DATA 0
G0461
G0462 *; RAM Location # 101
G0463 0065 0000 K49 DATA 0 ; 49
G0464
G0465 *; RAM Location # 102
G0466 0066 0000 SHIFT DATA 0 ; SHIFT table address
G0467
G0468 *; RAM Location # 103
G0469 0067 0000 K63 DATA 0 ; 63
G0470
G0471 *; RAM Location # 104
G0472 0068 0000 FI DATA 0 ; FI value
G0473
G0474 *; RAM Location # 105
G0475 0069 0000 WI DATA 0 ; WI value
G0476
G0477 *; RAM Location # 106
G0478 006A 0000 INQTAB DATA 0 ; Inverse quan table address
G0479
G0480 *; RAM Location # 107 ; 544
G0481 006B 0000 K544 DATA 0
G0482
G0483 *; RAM Location # 108 ; 5120
G0484 006C 0000 K5120 DATA 0
G0485
G0486 *; RAM Location # 109 ; 15
G0487 006D 0000 M15 DATA 0
G0488
G0489 *; RAM Location # 110
G0490 006E 0000 KFF80 DATA 0 ; >FF80
G0491
G0492 *; RAM Location # 111

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G0493 006F 0000 M127 DATA 0 ; 127
G0494
G0495 *; RAM Location # 112
G0496 0070 0000 MFFC0 DATA 0 ; -64
G0497
G0498 *; RAM Location # 113
G0499 0071 0000 BIASA DATA 0 ; 33*128
G0500
G0501 *; RAM Location # 114
G0502 0072 0000 M4095 DATA 0 ; 4095
G0503
G0504 *; RAM Location # 115
G0505 0073 0000 DATA 0 ; spare
G0506
G0507 *; RAM Location # 116
G0508 0074 0000 M32767 DATA 0 ; 32767
G0509
G0510 *; RAM Location # 117
G0511 0075 0000 KFF00 DATA 0 ; >FF00
G0512
G0513 *; RAM Location # 118
G0514 0076 0000 K56 DATA 0 ; 56
G0515
G0516 *; RAM Location # 119
G0517 0077 0000 K960 DATA 0 ; 960
G0518
G0519 *; RAM Location # 120
G0520 0078 0000 K79 DATA 0 ; constants used for quantizing table
G0521
G0522 *; RAM Location # 121
G0523 0079 0000 K95 DATA 0 ; constants used for quantizing table
G0524
G0525 *; RAM Location # 122
G0526 007A 0000 K130 DATA 0 ; constants used for quantizing table
G0527
G0528 *; RAM Location # 123
G0529 007B 0000 K138 DATA 0 ; constants used for quantizing table
G0530
G0531 *; RAM Location # 124
G0532 007C 0000 K2309 DATA 0 ; constants used for quantizing table
G0533
G0534 *; RAM Location # 125
G0535 007D 0000 THREE DATA 0 ; 3
G0536
G0537 *; RAM Location # 126
G0538 007E 0000 DATA 0 ; spare
G0539
G0540 *; RAM Location # 127
G0541 007F 0000 M0080 DATA 0 ; allow mask
G0542

```

NO ERRORS, NO WARNINGS

32010 FAMILY				16:36:03 03-20-85			
MACRO ASSEMBLER		PC2.1 84.107		PAGE 0055			
CCITT LABEL	VALUE	DEFN	REFERENCES				
A1	0011	G0209	B0252 B0270 D0431 D0456 D0458 D0464 D0515 D0523				
A11M	0426	D0520					
A2	0012	G0212					
ADC	0001	A0031	A0556 A0126				
ADD018	0003	D0336					
ADDA	035C	D0085					
ADDC	03E1	D0413					
ADONE	01A8	A0566	A0562				
ADDSGN	036C	D0104	B0321 B0327 B0361				
AL	0006	F0076	F0030				
ALAM	055E	F0033	A0512 F0035				
ALAMR	0184	A0511	A0173 F0034				
ALAWX	004E	A0172					
ALOG	035E	D0090					
ANOMLE	019F	A0559	A0557				
ANOMLY	01AF	A0572	A0564				
APP	0005	G0173	B0322 B0325 D0323 D0324 D0325 D0336 D0338				
APRED	0386	D0345	D0335				
AQUAN	02AA	C0024	A0099 A0168 A0351 A0504				
B1	00008	G0188	B0167 B0183 D0396 D0398 D0402				
B2	0000C	G0191	B0144 B0160 D0389 D0391 D0395				
B3	0000C	G0194	B0121 B0137 D0382 D0384 D0388				
B4	0000D	G0197	B0098 B0114 D0375 D0377 D0381				
B5	0000E	G0200	B0075 B0091 D0368 D0370 D0374				
B6	0000F	G0203	B0082 B0088 D0361 D0363 D0367				
BIAS	00040	G0391	A0082 A0089 A0253 A0264 A0272 A0282 A0290 A0302 A0310 A0320 A0334 A0346 A0426 A0436 A0444 A0456 A0464 A0474 A0488 A0489 A0490 A0492 A0504				
BIASA	00771	G0499	A0180 A0184 A0188 A0192 A0196 A0200 A0204				
C0T01	02B8	C0073					
C0T03	02B5	C0075					
C0T07	02B2	C0071					
C2T03	02C3	C0083	C0074				
C4T05	02C1	C0093					
C4T07	02CE	C0091	C0072				
C6T07	02DC	C0101	C0092				
C8T011	02EA	C0111	C0070				
C8T014	02E7	C0109					
C8T09	02ED	C0113					
CAT08	02FC	C0125	C0112				
CATT	0002	A0033	A0101 A0170 A0210 A0364				
CCITD	030E	C0139					
CCTOE	030B	C0137	C0110				
CHK1	01C4	B0068	E0007				
CHK11	025F	B0245	E0031				
CHK2	01DE	B0091	E0011				
CHK21	027A	B0260	E0095				
CHK3	01F8	B0114	E0114				
CHK4	0212	B0137	E0119				
CHK5	022C	B0160	E0023				
CHK6	0246	B0183	E0027				
CHKH1	0386	B0186	D0183				
C10T01	032C	C0187					
C10T03	0329	C0185					
C12T03	0335	C0193	C0186				
C14T07	033E	C0199	C0184				
C15T06	0341	C0201					

32010 FAMILY				16:36:03 03-20-85			
MACRO ASSEMBLER		PC2.1 84.107		PAGE 0056			
CCITT LABEL	VALUE	DEFN	REFERENCES				
C16T07	034A	C0207	C0200				
CLNUP	00EA	A0342	A0330				
CLNUPA	0176	A0496	A0484				
CMPSA	010B	A0405					
CMPSU	007F	A0251					
CMS	005B	C0075	F0019				
CTL	00B0	A0034	F0028				
D0T01	0438	D0559					
D0T03	0435	D0557					
D0T07	0432	D0555					
D2T03	043D	D0564	D0558				
D2T05	0440	D0578					
D4T07	044A	D0576	D0556				
D6T07	045A	D0590	D0577				
D6T09	046F	D0608					
D8T08	046C	D0606					
D8T0F	0469	D0604	D0554				
DAC	0001	A0032	A0357 A0510				
DAT08	0480	D0624	D0607				
DCT00	0494	D0642					
DCT0F	0491	D0640	D0605				
DETOF	04A5	D0658	D0641				
DHL	0008	G0182	D0293 D0294 D0295 D0329 D0332				
DMS	0007	G0179	D0273 D0274 D0275 D0331				
DNEC	0106	A0376	A0369				
DQ1EX	007A	A0222	A0215				
DQ1EX	041C	D0508					
DQ1EX	03F9	D0442	D0437				
DQ1EX	0010	G0205	D0103 D0110 D0111 D0416 D0548				
DQ1EX	0016	G0224	B0146 B0147				
DQ1MAN	005C	G0436	B0150				
DQ2EXP	0017	G0227	B0123 B0124				
DQ2MAN	0050	G0439	B0127				
DQ3EXP	0018	G0230	B0100 B0101				
DQ3MAN	005E	G0442	B0104				
DQ4EXP	0019	G0233	B0077 B0078				
DQ4MAN	005F	G0445	B0081				
DQ5EXP	001A	G0236	B0055				
DQ5MAN	0060	G0448	B0058				
DQEXP	0015	G0221	B0169 B0170 D0091 D0095				
DQMAN	005B	G0433	B0173 D0094 D0101 D0126 D0127 D0128 D0130				
E0	04EE	E0062	E0131				
E0T01	04EB	E0060					
E0T03	04EB	E0058					
E1	04F2	E0066	E0061				
E110	0529	E0114	E0109				
E12	0537	E0122					
E13	053E	E0132	E0121				
E2	04F9	E0072					
E2T03	04F6	E0070	E0059				
E3	04FD	E0076	E0071				
E4	0504	E0082					
E4T06	0501	E0080	E0057				
E5	050B	E0088					
E5T06	0508	E0086	E0081				

[illegible]