TEXAS INSTRUMENTS

Application Report
SPRA478

TMS320C6000 EVM Daughterboard Interface

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Abstract

This application note provides information on how to interface a daughterboard to the TMS320C62x EVM, TMS320C62x McEVM, and TMS320C67x EVM. An introduction on the daughterboard concept is provided identifying the advantages of using this approach for rapid prototyping and accelerated product developments. Details on the daughterboard design are provided including identification of the memory and peripheral interfaces' signals, buffering considerations, power budget and mechanical and connector information.

A list of potential daughterboards is presented to reinforce the point that when they are used with the EVM, a wide range of applications can be addressed. By designing daughterboards based on the information in this application note, a standardized, modular approach can be used that allows system designers to concentrate on system-specific issues rather than the core DSP and memory design. By using the low-cost EVM to address a wide range of applications, by simply exchanging daughterboards, users do not have to learn a new platform or write new utilities and board support software for every project.

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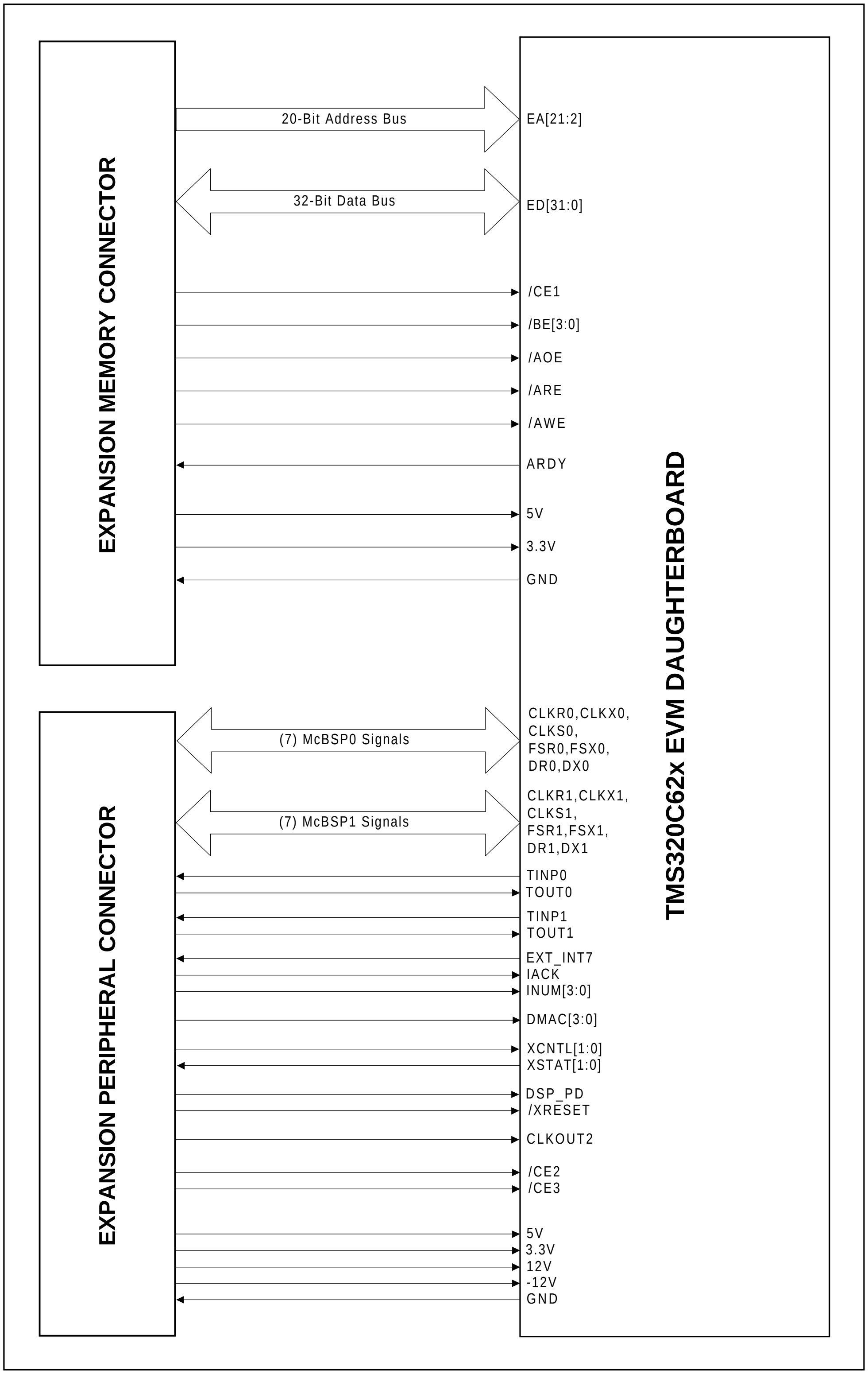
Introduction

The EVM provides two expansion connectors that allow its functionality to be extended to address application-specific requirements. The expansion connectors provide a daughterboard with access to DSP signals that enable peripheral devices with memory-mapped and serial interfaces to be used with the EVM. These direct, high-speed connections to the DSP, which are critical for real-time processing, do not depend on host processor interaction or PCI bus transfers. Daughterboards can provide both analog and digital capabilities, giving the low-cost EVM flexibility to be used in a variety of applications. Users can design their own custom EVM daughterboards or obtain them from other vendors.

EVM daughterboards present a modular approach to interface design that can support a wide range of applications. With this modular approach, the core DSP and memory design of the EVM can be leveraged across several applications, with daughterboards providing functions to meet unique requirements. This protects a user's investment in the EVM platform, including all the tools and software that are developed for it, since it can be used for multiple applications. Future design efforts only need to focus on new interface requirements and related support software, rather than the complete DSP processing system. This incremental design paradigm lends itself well to rapid prototyping and product development acceleration.

The EVM's two expansion connectors provide access to the DSP's asynchronous external memory interface (EMIF) and its on-chip peripheral and control/status signals. Both connectors also provide multiple voltages to supply power to the daughterboard. Each of the expansion connectors is a low-profile, 80-pin, 0.050"-pitch connector designed to support high-speed board interconnections. Mating connectors for the daughterboard are available in several mating heights which all meet the maximum height requirement defined in the PCI Local Bus Specification Revision 2.1[4]. Two standard sizes of EVM daughterboards are defined. A small size is intended for applications that do not require an I/O connection on the mounting bracket. A large size is intended for applications that require an I/O connection on the mounting bracket or need more board space for implementation. Figure 1 shows the daughterboard interface including DSP signals provided by the expansion connectors.

Figure 1. TMS320C62x EVM Daughterboard Interface



Expansion Memory Interface

The EVM's expansion memory interface provides the DSP's asynchronous EMIF signals to a daughterboard. External asynchronous memories and memory-mapped peripherals can be interfaced to the EVM, including nonvolatile memory that could be used to boot the EVM upon reset. Since the expansion memory interface provides a parallel, 32-bit data interface, it provides the fastest data transfer mechanism with the DSP. The expansion memory interface can only be mastered by the DSP, so the memory-mapped devices on a daughterboard are always slave devices.

The expansion memory interface includes:

20 external address signals (EA[21:2]). All of the DSP's 20 external address signals are available on the expansion memory interface, allowing up to 4M bytes of external memory to be addressed. However, because the CE1 space must be shared with onboard EVM peripherals, only the lower 3M bytes are available to the daughterboard. If CE2 or CE3 is used for external asynchronous memory instead of SDRAM, an additional 4M bytes in each of these memory spaces can be addressed. Therefore a total of 11M bytes of asynchronous memory is directly addressable on a daughterboard. A memory page register could be used to enable a very large memory space on a daughterboard.

32 external data signals (ED[31:0]). All of the DSP's 32 external data signals are available on the expansion memory interface to support full 32-bit word accesses to the daughterboard.

CE1 memory space enable (/CE1). The DSP's CE1 memory space enable is available on the expansion memory interface to allow asynchronous accesses to daughterboard memory and memory-mapped devices. The CE2 and CE3 memory space enables are provided on the expansion peripheral connector for additional asynchronous memory address spaces.

Four byte enables (/BE[3:0]). The DSP's four byte enables are available on the expansion memory interface to support byte (8-bit), halfword (16-bit) and word (32-bit) daughterboard memory accesses.

Four asynchronous control signals (/AOE, /ARE, /AWE and ARDY). The DSP's asynchronous EMIF control signals are provided to control memory accesses to the daughterboard. These signals indicate the direction of the data transfer and allow the daughterboard to add wait states to memory accesses.

Power signals. The expansion memory interface also provides ground, 5-V and 3.3-V voltages to the daughterboard.

The expansion memory interface supports both 3.3-V and 5-V devices since it uses low-voltage translation buffers that have 5-V tolerant inputs. The expansion memory interface is provided by a dual-row, 80-pin surface-mount connector. This connector has a low profile with 0.050" (1.27 mm) pitch. The recommended mating connector provides up to 0.465" board spacing, allowing ample space for daughterboard components.

Table 1 identifies the pinout of the expansion memory interface connector. Note that table shows the actual connector pin names which may vary slightly from the DSP pin names.

Table 1. EVM Daughterboard Expansion Memory Connector Pin List

Pin #	Signal Name	Type	Pin #	Signal Name	Type
1	5 V	O	2	5 V	O
3	XA21	O	4	XA20	O
5	XA19	O	6	XA18	O
7	XA17	O	8	XA16	O
9	XA15	O	10	XA14	O
11	GND	-	12	GND	-
13	XA13	O	14	XA12	O
15	XA11	O	16	XA10	O
17	XA9	O	18	XA8	O
19	XA7	O	20	XA6	O
21	5 V	O	22	5 V	O
23	XA5	O	24	XA4	O
25	XA3	O	26	XA2	O
27	/XBE3	O	28	/XBE2	O
29	/XBE1	O	30	/XBE0	O
31	GND	-	32	GND	-
33	XD31	I/O/Z	34	XD30	I/O/Z
35	XD29	I/O/Z	36	XD28	I/O/Z
37	XD27	I/O/Z	38	XD26	I/O/Z
39	XD25	I/O/Z	40	XD24	I/O/Z
41	3.3 V	O	42	3.3 V	O
43	XD23	I/O/Z	44	XD22	I/O/Z
45	XD21	I/O/Z	46	XD20	I/O/Z
47	XD19	I/O/Z	48	XD18	I/O/Z
49	XD17	I/O/Z	50	XD16	I/O/Z
51	GND	-	52	GND	-
53	XD15	I/O/Z	54	XD14	I/O/Z
55	XD13	I/O/Z	56	XD12	I/O/Z
57	XD11	I/O/Z	58	XD10	I/O/Z
59	XD9	I/O/Z	60	XD8	I/O/Z
61	GND	-	62	GND	-
63	XD7	I/O/Z	64	XD6	I/O/Z
65	XD5	I/O/Z	66	XD4	I/O/Z
67	XD3	I/O/Z	68	XD2	I/O/Z
69	XD1	I/O/Z	70	XD0	I/O/Z
71	GND	-	72	GND	-
73	/XRE	O	74	/XWE	O
75	/XOE	O	76	XRDY	I
77	SPARE (N/C)	-	78	/XCE1	O
79	GND	-	80	GND	-

Memory Decoding

The expansion memory interface provides a CE1 memory space enable that should be used by the daughterboard for memory decoding. The CE1 asynchronous memory space is shared with the EVM's onboard peripherals, so the first 3M bytes of the 4M bytes space are available to the daughterboard. This memory space is indicated by /CE1 being asserted with either EA21 or EA20 being low. Onboard peripherals are addressed when both EA21 and EA20 is high. If one or both banks of SDRAM on the EVM are not required by an application, then the CE2 and CE3 memory spaces can be used to provide 4M bytes of additional memory each. If this is done, then the respective memory space control register should be configured for asynchronous memory, and the EVM's CPLD register SDCNTL should disable the desired SDRAM bank(s).

Buffer Characteristics

The DSP's EMIF address, data and control signals brought to the expansion memory interface are buffered on the EVM for several reasons:

- ❑ Preserve signal integrity
- ❑ Distribute loads efficiently
- ❑ Isolate daughterboard interface during onboard memory cycles
- ❑ Eliminate problems due to daughterboard device relinquish time
- ❑ Provide 5-V to 3.3-V voltage translation to support 5-V devices on daughterboard
- ❑ Provide sufficient current sink and source for the daughterboard interface

The designer of a daughterboard should be aware that due to the signal buffering on the EVM board, there are additional signal delays from the specified TMS320C6201 DSP timing parameters. The buffering also provides a defined current sink and source capabilities. These buffer characteristics must be accounted for during the design of a daughterboard. Table 2 summarizes the characteristics of the buffers used for the various expansion memory interface signals including maximum delay and sink/source current.

Table 2. Expansion Memory Interface Buffer Characteristics

Signal Type	Buffer Type	Max Delay	Max I_{OL}	Max I_{OH}
Address	SN74ALB16244	2 ns	25 mA	-25 mA
Data	SN74LVTH162245	4.1 ns	64 mA	-32 mA
Control	SN74ALB16244	2 ns	25 mA	-25 mA

Wait States

The expansion memory interface supports wait state control by the daughterboard through the use of the DSP’s ARDY ready signal. The EVM includes a 10K pull-up resistor on the external ARDY signal (XRDY) from the daughterboard, so it defaults to zero wait states. If wait states are required for daughterboard device operation, then logic on the daughterboard should clear XRDY until the device is ready to complete the data transfer, at which time XRDY should be set high. In order to support wait states, the DSP requires that the memory space’s read/write strobe fields be initialized to a minimum of three CLKOUT1 cycles. The values of the memory space’s setup and strobe periods may need to be adjusted to account for the response time of the daughterboard’s logic. For example, if the logic cannot clear XRDY before the DSP begins to sample it, the DSP will end the cycle before the device is ready.

Expansion Peripheral Interface

The EVM’s expansion peripheral interface provides the DSP’s on-chip peripheral signals to a daughterboard. This peripheral interface allows synchronous serial devices, such as codecs and communication controllers, to be added to the EVM via a daughterboard. The expansion peripheral interface includes:

Seven signals for each of the serial ports (McBSP0 / McBSP1). The DSP’s seven McBSP1 signals are available on the expansion peripheral interface. These signals are buffered by a TI ’CBT3384 device to support both 5-V and 3.3-V serial devices using McBSP1 on the daughterboard.

The DSP’s seven McBSP0 signals are also available when the DSP software controls onboard TI ’CBT3257 multiplexers that connect them to the expansion connector rather than the onboard audio codec. This architecture provides a daughterboard with access to both of the DSP’s serial ports, which is useful in many DSP applications. Because the ’CBT3257 multiplexer is used, both 5-V and 3.3-V serial devices can use McBSP0 on a daughterboard.

Both serial ports allow full-duplex connections between the DSP and the daughterboard consisting of separate data, frame sync and clock signals for the receive and transmit paths.

Two input/output signals for each of the DSP timers (timer 0 / timer 1). The expansion peripheral interface includes each of the DSP timers’ input and output signals. This allows timer signals to be sent to the daughterboard, or timer input or events to be counted to come from the daughterboard. Each timer has one input and one output signal.

Interrupt, interrupt acknowledge, and identification signals. A DSP external interrupt (EXT_INT7) is included on the expansion peripheral interface to allow the daughterboard to interrupt the DSP to notify it of data transfers and other significant events. This interrupt is pulled down on the EVM, so the daughterboard must drive it high to interrupt the DSP (rising edge). Additionally, the DSP’s interrupt acknowledge (IACK) and interrupt identification number signals (INUM[3:0]) are available to the daughterboard.

Four DMA completion flags. The DMA action complete flags (DMAC[3:0) are available to the daughterboard on the expansion peripheral interface. These signals provide a method of feedback to external logic generating an event for each DMA channel. The DMAC signals can also be used for general-purpose output control signals controlled from the DSP’s DMA channel secondary control register.

Four general-purpose input/output flags. Two general-purpose control outputs and status inputs are brought to the expansion peripheral interface to allow the DSP to control and monitor various signals on a daughterboard. The XCNTL[1:0] and XSTAT[1:0] signals can be controlled by DSP software by accessing the CPLD's DSP memory-mapped CNTL and STAT registers respectively.

Power-down signal. The DSP's power-down indication signal (DSP_PD) is also brought to the expansion peripheral interface so that a daughterboard can be powered-down if desired.

Reset signal. The expansion peripheral interface also provides a reset signal that is active low when the board is in the reset state. This allows circuitry on the daughterboard to be set to a known state. The reset signal is asserted for a minimum of 140 ms upon power-up, via a manual reset pushbutton on the EVM or under host or DSP software control. A memory-mapped register bit in the CPLD's CNTL register allows DSP software to directly control this reset signal.

CLKOUT2 clock signal. The DSP's CLKOUT2 signal (CPU clock divided by 2) is brought out to the expansion peripheral interface for synchronization needs on daughterboards.

Buffered CE2 and CE3 signals. The DSP's CE2 and CE3 memory space enables are brought out to the expansion peripheral interface to support additional fast memory decoding. This can be useful on daughterboards that have multiple devices that need memory decodes. The CE2 and CE3 are dedicated to SDRAM use on the EVM board, but the EMIF control registers can be initialized for asynchronous operation, which disables the respective SDRAM banks and allows expansion asynchronous memory to be used instead. The CE2 and CE3 SDRAM enable bits in the CPLD's SDCNTL register must be disabled to allow CPLD logic to enable the external data transceivers for CE2/CE3 daughterboard accesses.

Power signals. The expansion peripheral interface also provides ground, 12-V, -12-V, 5-V and 3.3-V power signals to the daughterboard.

The serial synchronous ports can run up to 80 Mbits/sec (10 Mbytes/sec) with a 160 MHz DSP, so they are about an order of magnitude slower than the parallel, memory-mapped interface. Serial interfaces do provide the advantage of less complexity, with only a handful of signals being required. Additionally, the serial ports provide a direct data connection to the DSP without contending for EMIF bandwidth. Several industry-standard devices can be directly connected to a DSP's flexible McBSP such as computer telephony switches (MVIP, SCSA, H.110), T1/E1 framers, A/D converters and D/A converters.

The expansion peripheral interface supports both 3.3-V and 5-V devices since it uses low-voltage translation buffers that have 5-V tolerant inputs. The expansion peripheral interface is provided by a dual-row, 80-pin surface-mount connector. This connector has a low profile with 0.050” (1.27 mm) pitch. The recommended mating connector provides up to 0.465” board spacing, allowing ample space for daughterboard components.

Table 3 identifies the pinout of the expansion peripheral interface connector. Note that table shows the actual pin names which may vary slightly from the DSP pin names.

Table 3. EVM Daughterboard Expansion Peripheral Connector Pin List

Pin #	Signal Name	Type	Pin #	Signal Name	Type
1	12 V	O	2	-12 V	O
3	GND	-	4	GND	-
5	5 V	O	6	5 V	O
7	GND	-	8	GND	-
9	5 V	O	10	5 V	O
11	SPARE (N/C)	-	12	SPARE (N/C)	-
13	RSVD (N/C)	-	14	RSVD (N/C)	-
15	RSVD (N/C)	-	16	RSVD (N/C)	-
17	SPARE (N/C)	-	18	SPARE (N/C)	-
19	3.3 V	O	20	3.3 V	O
21	CLKX0	I/O/Z	22	CLKS0	I
23	FSX0	I/O/Z	24	DX0	O
25	GND	-	26	GND	-
27	CLKR0	I/O/Z	28	SPARE (N/C)	
29	FSR0	I/O/Z	30	DR0	I
31	GND	-	32	GND	-
33	CLKX1	I/O/Z	34	CLKS1	I
35	FSX1	I/O/Z	36	DX1	O
37	GND	-	38	GND	-
39	CLKR1	I/O/Z	40	SPARE (N/C)	-
41	FSR1	I/O/Z	42	DR1	I
43	GND	-	44	GND	-
45	TOUT0	O	46	TINP0	I
47	SPARE (N/C)	-	48	SPARE (N/C)	-
49	TOUT1	O	50	TINP1	I
51	GND	-	52	GND	-
53	XEXT_INT7	I	54	IACK	O
55	INUM3	O	56	INUM2	O
57	INUM1	O	58	INUM0	O
59	/XRESET	O	60	DSP_PD	O
61	GND	-	62	GND	-
63	XCTRL1	O	64	XCTRL0	O
65	XSTAT1	I	66	XSTAT0	I
67	SPARE (N/C)	-	68	SPARE (N/C)	-
69	/XCE2	O	70	/XCE3-	O
71	DMAC3	O	72	DMAC2	O
73	DMAC1	O	74	DMAC0	O
75	GND	-	76	GND	-
77	GND	-	78	XCLKOUT2	O
79	GND	-	80	GND	-

Signal and Buffer Characteristics

The DSP's McBSP signals are buffered to enable both 5-V and 3.3-V devices to be used on a daughterboard. The McBSP signals are not buffered with active buffers like the memory interface since they run slower, are typically only connected to a single device, and do not have the high dynamic current requirements. For these reasons, TI 'CBT bus switches and multiplexers are used to provide the voltage translation. These devices exhibit a maximum of 250 ps delay and effectively appear in the circuit as a 5-ohm resistor.

The external interrupt (XEXT_INT7) and timer inputs (TINP0, TINP1) are similarly buffered using a 'CBT device. Since the DSP's output voltages are compatible with 5-V devices, the DSP's timer output signals (TOUT0, TOUT1) are brought directly to the expansion peripheral interface connector.

The DSP's interrupt acknowledge, interrupt and DMA identification codes, power down, and reset signals are brought directly to the expansion connector without buffering.

The general-purpose input/output flags are interfaced directly to the EVM's CPLD that has 5-V tolerant inputs and drives 3.3-V outputs that are compatible with 3.3-V and 5-V devices. The XCNTL[1:0] signals are driven by the Altera EPM7256S CPLD and the XSTAT[1:0] signals from the daughterboard are brought directly to the CPLD.

The CLKOUT2 signal presented to the daughterboard is actually a buffered version of the DSP's SDCLK signal. The SDCLK and CLKOUT2 signals have the same frequency and phase, so either one can be used in applications. The SDCLK was used as the source clock on the EVM because it was already used as an input to a zero-delay clock driver device (Cypress CY2308-1H) that provided multiple outputs. One of these outputs is used to drive the expansion peripheral interface's XCLKOUT2 signal.

The /XCE2 and /XCE3 memory space enable signals are buffered versions of the DSP's /CE2 and /CE3 signals respectively. The buffers that are used on the EVM are the TI SN74ALB16244 which have a maximum propagation delay of 2 ns and have a symmetric drive of +/- 25 mA. These should be the only two signals whose timing delay needs to be considered during daughterboard designs if they use the CE2 or CE3 memory spaces.

Daughterboard Power

The TMS320C62x EVM's two expansion connectors provide 3.3-V, 5-V, 12-V and –12-V power supplies to the daughterboard. Multiple digital grounds are also provided on the expansion connectors.

The 3.3-V power supply is rated at 3A, but can deliver up to 3.6-A before it is shutdown due to current limiting. The 3.3-V power supply is used for buffers, CPLD I/O, DSP I/O and memories on the EVM board. The amount of current available to the daughterboard is application-dependent since the processor's speed, amount of external memory accesses and general board activity influence the amount of 3.3-V current required for onboard devices. Worst case numbers indicate a maximum of 1A being available to the daughterboard on the 3.3-V supply.

The 5-V power supply to the daughterboard is provided directly from the PCI bus during PCI operation, or the external power supply when operated in standalone mode on a desktop. The 5-V power supply to the EVM board is the power source for both the 1.8-/2.5-V and the 3.3-V regulators on the board. The 5-V power supply is also used to power the PCI controller, audio codec, JTAG TBC, voltage translation buffers and the CPLD core. The amount of current available to the daughterboard is application-dependent also since board activity determines the onboard current requirement. The PCI specification limits the maximum 5-V current to 5A for PCI operation. If a maximum of 3A for each voltage regulator is assumed with 85% efficiency, then the available current for the daughterboard would be about 1A. For standalone operation, the only limitation would be the external power supply.

The 12-V power supply to the daughter board is provided directly from the PCI bus during PCI operation, or the external power supply when operated in standalone mode on a desktop. The 12-V power supply to the EVM board is only used as the power source for the analog 5-V voltage regulator. The 12-V current requirement on the board is only about 40 mA. The PCI specification limits the maximum 12-V current to 500 mA, so the daughterboard can draw a maximum of 460 mA in a PCI slot. For standalone operation, the only limitation would be the external power supply.

The –12-V power supply is not used on the EVM board. It is provided directly to the daughterboard from the PCI slot or the external power supply. The PCI specification limits the maximum –12-V current to 100 mA. For standalone operation, the only limitation would be the external power supply.

Table 4 summarizes the current available to the EVM daughterboard on each of the four power supplies.

Table 4. Maximum Daughterboard Current

Power Supply	Maximum Daughterboard Current
3.3-V	1A
5-V	1A
12-V	460 mA (or ext. power supply limit)
-12-V	100 mA (or ext. power supply limit)

Daughterboard Dimensions

Two standard sizes of daughterboards are defined: small and large.

The small daughterboard measures approximately 3.15” by 3.4” and mounts in the center of the EVM board over the CPLD and low-profile buffers and memories. This size is intended for daughterboards that do not require I/O connections on the mounting bracket. A good example of a small daughterboard would be a Flash memory board.

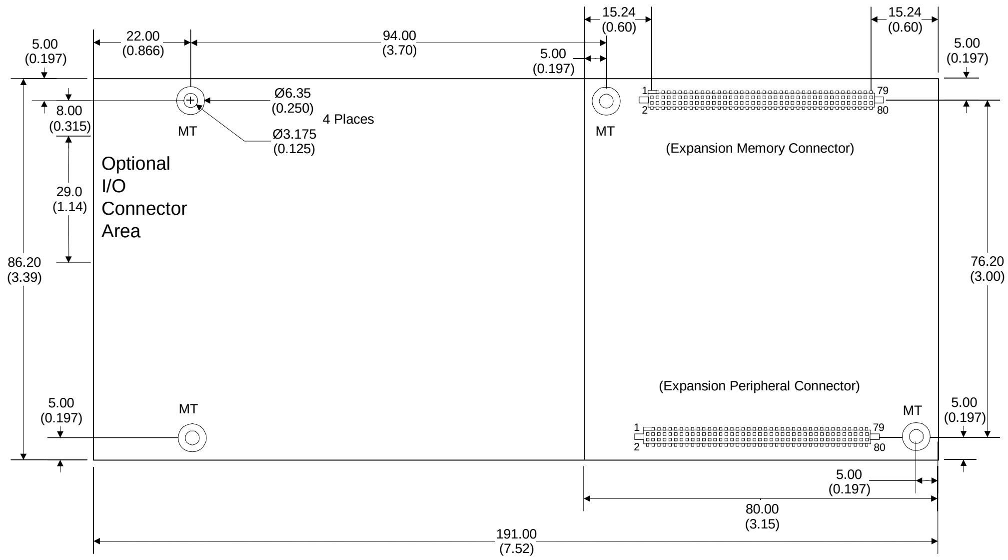
The large daughterboard measures approximately 7.5” by 3.4” and mounts from the center of the board over to the mating connector end of the board, adjacent to the mounting bracket. This size is intended for daughterboards that require an I/O connector on the mounting bracket or need more space for their components. Examples of large daughterboards include T1/E1, SCSI, video, A/D, D/A and Ethernet daughterboards. It is probable that most daughterboards will use the large form factor to support custom I/O connections. However, it is possible that the connections could be brought to the mounting bracket via cables if the circuitry fits in the small form factor.

All daughterboards mount with their component sides down (opposing the EVM components). This ensures that the PCI height requirement is met and no components are exposed to possible damage from an adjacent board due to insertions and extractions.

The EVM provides four standoff mounting holes to support daughterboard connections. Two mounting holes, located adjacent to the external peripheral and external memory connectors are to be used for all daughterboards. Two additional mounting holes are provided near the PC mounting bracket for long daughterboards in order to provide additional stability.

Figure *2* shows the small and large daughterboard envelopes, the relationship between the two expansion connectors, and the relative location of the four mounting holes on the component side of the EVM board.

Figure 2. Daughterboard Envelopes and Connections on the TMS320C6x EVM



NOTES:

1. All dimensions are shown in millimeters. Inch dimensions are shown in
2. Drawing shows daughterboard envelopes and connections on component side of EVM
3. Standard size daughter board is 80.0 x 86.2 mm (3.15 x 3.39
4. Full-size daughter board is 191.0 x 86.2 mm (7.52 x 3.39
5. Daughter board connectors are Samtec .050x.050" Micro Strips (SFM-140-L2-S-D-
6. Daughter board mating connectors are Samtec TFM-140-32-S-D-
7. Mating height is 0.465" (11.81
8. There are four plated holes (denoted MT) on the EVM for standoff

CAUTION***: It is important to note that this figure is showing the top side of the EVM, <u>not</u> the actual daughterboard!***

Daughterboard Connectors and Mating Dimensions

The TMS320C62x EVM uses two 80-pin 0.050” x 0.050” TFM-series connectors from Samtec. The part number is SFM-140-L2-S-D-LC. The recommended mating connector (Samtec part number TFM-140-32-S-D-LC) is a surface-mount connector that provides a 0.465” mated height which meets the PCI’s maximum component height of 0.57”. This mating height allows for passive components on the back-side of the daughterboard.

Figure 3 and Table 5 show the mating dimensions of a daughterboard mounted on an EVM board. It is assumed that a minimum of 0.050” clearance is maintained between EVM and daughterboard components.

Figure 3. Daughterboard Mating Dimensions Illustration

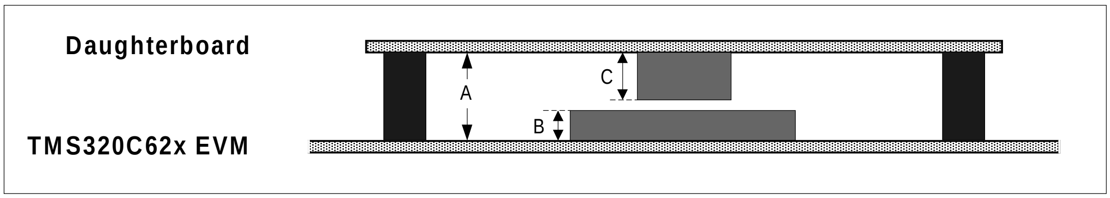


Table 5. Daughterboard Mating Dimensions

Label	Description	Dimension (Small DB)	Dimension (Large DB)
A	Mated Height (Clearance between DB and EVM)	0.465”	0.465”
B	Maximum EVM Component Height	0.150”	0.180”
C	Maximum Daughterboard Component Height	0.265”	0.235”

The dimensions show that the worst case clearance exists above the JTAG TBC (SN74ACT8990) on the EVM board for a large daughterboard. In this worst case, over about a 0.4 square inch area, there is a maximum daughterboard component height of 0.235”. Over the rest of the large daughterboard area, about 25% of which has no EVM has no components at all, allowing a maximum height of 0.415” for daughterboard components.

For a small daughterboard, the JTAG TBC is not in its envelope, so the worst case situation is above the CPLD that has a height of 0.15”. The only other EVM components of interest in the small daughterboard envelope are buffers that have a height of 0.11”, allowing a maximum daughterboard component height of 0.305" in about 75% of its envelope.

The worst case numbers should be used as a general guideline. In special cases, taller daughterboard components can be placed in areas of the EVM that have components with lower profiles or no components at all.

Potential Daughterboards

Since the TMS320C62x EVM expansion interfaces' support both memory-mapped and serial interfaces, daughterboards can be developed using a variety of analog and digital devices. Daughterboards allow the low-cost, standardized EVM board to be used in a wide range of applications, since its functionality and interfaces can be defined by the daughterboards that are used with it.

There are several ongoing EVM daughterboard efforts at Texas Instruments, DNA Enterprises, and other TI third party companies. As new technologies are introduced, they can be showcased with C6x DSP processing power using an application-specific daughterboard.

Some examples of potential daughterboards for the TMS320C62x EVM include:

- T1/E1/ISDN
- MVIP/SCSA/H.100 Telephony Busses
- 10/100 BASE-T Ethernet
- AC97 Multimedia Audio Codec
- High-speed Data Acquisition
- Multi-channel Audio Interfaces
- Non-volatile Memory
- SCSI-2
- IEEE-1394 Firewire
- Fibre Channel
- USB
- RS-232 / RS-485
- Video
- Optical Interface
- Digital Down Converter
- Digital Radio Receiver
- Professional Digital Audio (AES/EBU)
- Image Frame Grabber
- Graphics Accelerator
- Motion Controller
- Multi-channel Digital I/O
- Reconfigurable Computation Engine

- ❑ Prototyping Board

This list of potential daughterboards is only a small sample. EVM users span a wide range of industries and technologies, so they will find other applications for daughterboards that meet their requirements. Additionally, as new markets realize that they can benefit from DSP, and the C62x specifically, they can target their technology on the C62x EVM platform without having to be DSP hardware designers by using daughterboards to provide their required interfaces.

References

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