Application Report
SPRA585

Connecting TMS320C54x DSP with Flash Memory

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Abstract

Flash memory offers better cost per bit than traditional EPROM when storage density increases. Flash memory competes with EPROM with lower power consumption, and smaller package and program content after assembling. These features make flash memory a good selection in applications like GPS receiver, hand-held MP3 player, and Set-Top Boxes. The Texas Instruments (TI™) TMS320C54x family of digital signal processors (DSPs) offers fast operation speed and low power consumption that makes this DSP ideal for portable applications where flash memory also fits. This application report provides a reference on interfacing a DSP with flash memory.

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Introduction to Flash Memory

Many vendors provide flash memory. Although the control logic is not identical, it is similar. This application report uses the Intel™ 28F400B3 that is 4M bits of flash memory.

Control Logic Signals

The control logic signals of the 28F400B3 are carried on six pins as listed in Table 1.

Table 1. Intel 28F400B3 Control Logic Signals

Symbol	Type	Description
/CE	I	Chip enable
/OE	I	Output enable
/WE	I	Write enable
/RP	I	Reset/Deep power down. It is connected to logic high ensuring normal operation.
/WP	I	Write protection. It is connected to logic high to enable programming content.
VPP		Program/Erase power supply. It is connected to Vcc simplifying power design.

When in read mode, the 28F400B3 read timing is compliant with typical memory read timing (that is, /CE and /OE are logic low and /WE is logic high). When in program/erase mode, the 28F400B3 timing is similar to typical memory write time (that is, /CE and /WE are logic low and /OE is logic high).

Command Set

The behavior of flash memory is controlled by a command set. It is the host's responsibility to issue the correct command set that instructs the flash memory into a specific mode. In this application report only a subset of the command set is supported, as listed in Table 2.

Table 2. 28F400B3 Command Set

Code	Device Mode	Description
FF	Read Array	Device is compatible with EPROM
40	Program	Device writes data into specific address
20	Erase	Device erases entire section before program

Program/Erase

Flash memory is organized into several sections. The section size is dependent on specific devices. Before programming flash memory, the entire section should be erased. Therefore, programming flash memory is performed section after section.

Both program and erase are two-bus cycle operations (see Table 3).

Table 3. 28F400B3 Program/Erase Bus Cycles

	1st Bus Cycle			2nd Bus Cycle		
Command	**Operation**	**Address**	**Data**	**Operation**	**Address**	**Data**
Program	Write	X	40H	Write	PA	PD
Erase	Write	X	20H	Write	BA	D0H

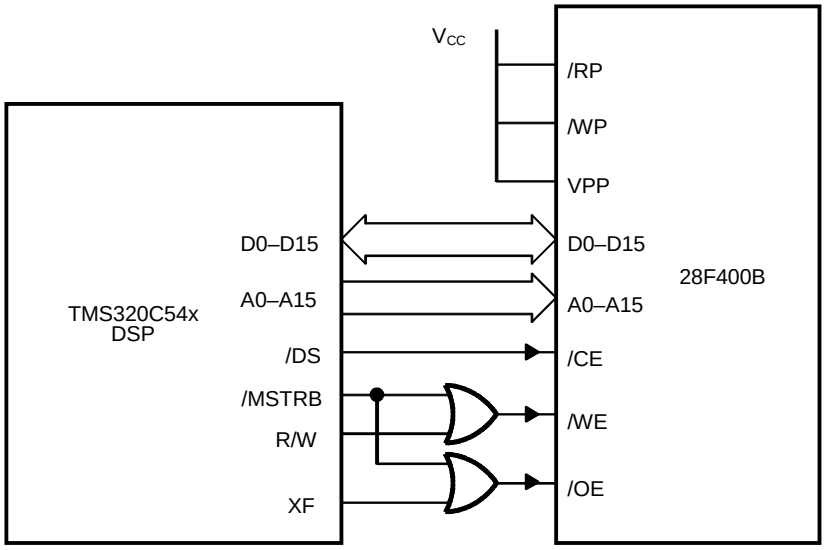
Note: PA = program address, PD = program data, BA = block address

After program/erase is initiated, the read operation can be used to check programming/erasing status. When program/erase is finished, the host should launch a read command to place the flash memory into normal read operation.

Connecting TMS320C54x with Flash Memory

The 28F400B3 is connected to ‘C54x as an external data memory (see Figure 1). The address bus and data bus are connected to the ‘C54x external bus, and /CE is connected to the /DS pin on the ‘C54x. The XF pin on the ‘C54x is used to enable programming. When XF is driven low, the flash memory should be in read mode. When XF is driven high, the flash memory can be erased and programmed. In order to match 28F400B3 timing requirements, XF is ORed with /MSTRB before being connected to /OE. The R/W pin is ORed with /MSTRB before being connected to /WE.

Figure 1. Connections Between TMS320C54x and 28F400B3



Software Design

The program and erase timings are controlled by the ‘C54x. The DSP program is run from on-chip memory. The programming flow chart is shown in Figure 2 and the erasing flow chart is shown in Figure 3.

Figure 2. Programming Flow Chart

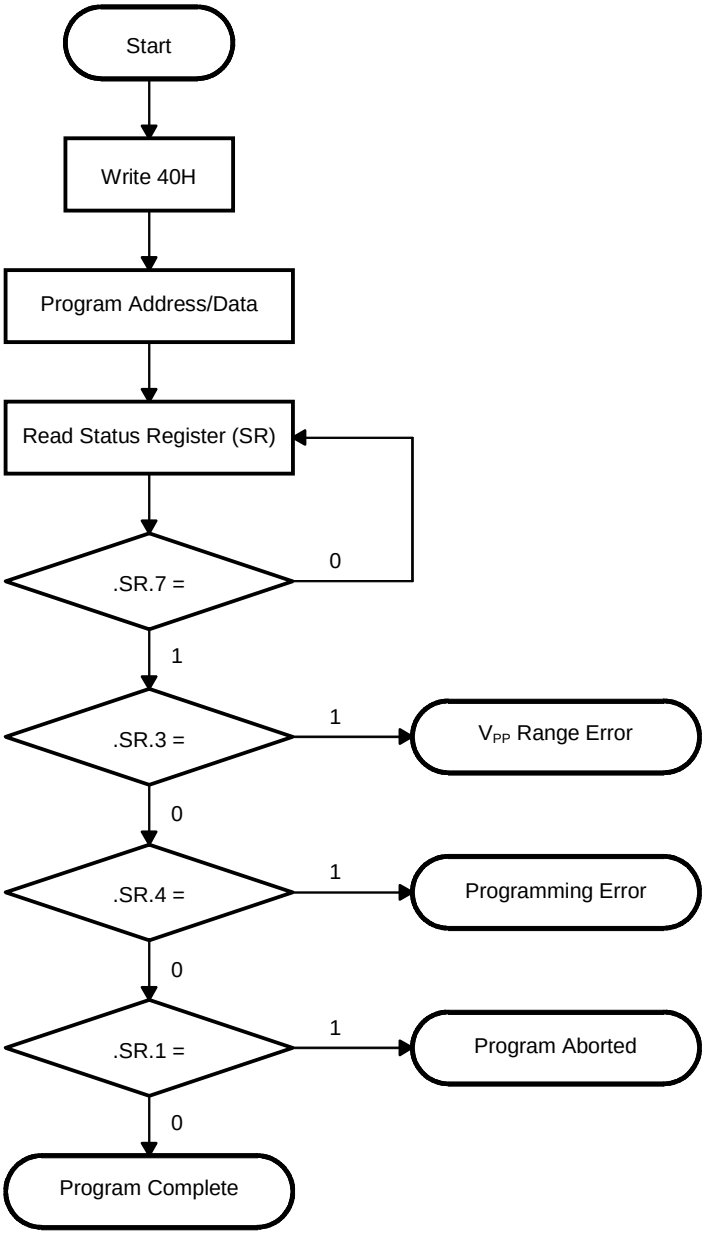
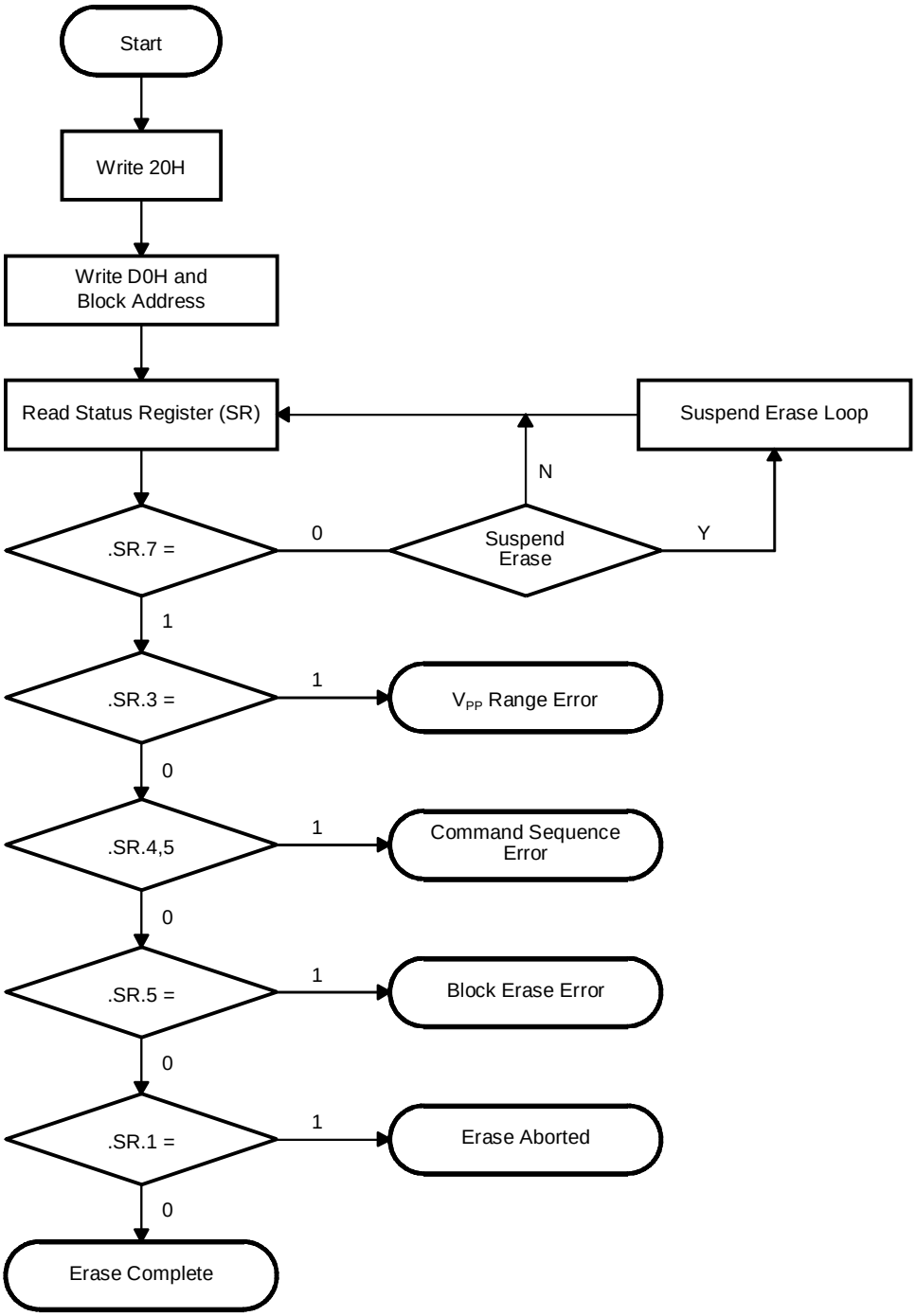


Figure 3. Erasing Flow Chart



References

1) *TMS320C54x Reference Set, Volume 1:CPU and Peripherals*. (SPRU131)

2) Intel SMART 3 Advanced Boot Block 4-Mbit, 8-Mbit, 16-Mbit Flash Memory Family. (290580-003)

Appendix A Assembly Code

```
      .mmregs
      .def    Start
      .text
Start:
      STM     #00FEH, SP
      STM     #03B4H, SWWSR   ;set s/w wait state = 5
      CALL    Set_Read_Mode   ;put into normal read mode
;        .
;        .
      STM     #0, AR1         ;ar1 is set to block address
      CALL    Erase
      STM     #4000H, AR1     ;ar1 is set to data address
      LD      #55AAH, B       ;bl contains data to program
      CALL    Program
      CALL    Set_Read_Mode
;        .
;        .
Set_Read_Mode:
      SSBX    XF              ;enable command write
      LD      #0FFH, A        ;read array command code
      STM     #4000H, AR1     ;any external memory
      STL     A, *AR1         ;write command code
      RPT     #4
      NOP                     ;delay CPU
      RSBX    XF              ;disable command write
      RET
Erase:
      PSHM    AR1             ;save block address
      SSBX    XF              ;enable command write
      LD      #20H, A         ;set command code
      STM     #4000H, AR1     ;any external address
      STL     A, *AR1         ;first byte = 20h
      LD      #0D0H, A        ;second byte = 0d0h
      STL     A, *AR1
      RPT     #4
      NOP                     ;delay CPU
      RSBX    XF              ;disable command write
E_RS:
      LD      *AR1, A         ;get status
      ADD     A, #0, B        ;b=a
      AND     #80H, B         ;test sr.7
      BC      E_SC, BNEQ
      AND     #40H, A         ;erase suspend?
      BC      Error, ANEQ
      B       E_RS            ;read sr again
E_SC:
      AND     #3AH, A         ;mask error bits
      BC      Error, ANEQ
      POPM    AR1             ;restore address
      RET
```

```
Program:
      SSBX    XF              ;enable command write
      LD      #40H, A         ;set program command code
      STL     A, *AR1         ;ar1 point to external address
      RPT     #4
      NOP                     ;delay CPU
      STL     B, *AR1         ;write date
      RPT     #4
      NOP                     ;delay CPU
      RSBX    XF              ;disable command write
P_RS:
      LD      *AR1, A         ;get status
      ADD     A, #0, B        ;b=a
      AND     #80h, B         ;test sr.7
      BC      P_RS, BNEQ      ;read sr again
P_SC:
      AND     #1AH, A         ;mask error bits
      BC      Error, ANEQ
      RET

Error:
      B       $               ;self loop

      .sect   ".vec"
      B       Start

      .end
```

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