Migrating from TMS320VC549 to TMS320VC5409

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ABSTRACT

This document describes issues of interest related to migration from the TMS320VC549 to the TMS320VC5409. The objective of this document is to indicate differences between the two devices. Functions that are identical between the two devices are not included. For detailed information on the specific functions of either device, refer to the device data sheets and/or the *TMS320C54x DSP CPU and Peripherals, Reference set, Volume 1* (SPRU131).

Migration issues from the VC549 to VC5409 are indicated with the following symbols, which are included at the beginning of each section:

[S] means software modification is required.

[H] means hardware modification is required.

[D] means the VC549 and VC5409 are different (usually due to added features on the VC5409), but no modification is necessary for migration (that is, the devices are different but compatible).

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1 Package and Pinout Compatibility [D]

The PGE package is pin compatible (same footprint) with the VC549. The VC5409 uses the TEST1 pin for HPI16 operation. Previously, this VC549 pin was reserved.

The VC5409 is available in two package types:

- 144-pin PGE thin quad flat pack (TQFP)
- 144-pin GGU ball grid array MicroStar BGA™

2 Power Supply [H]

The VC5409 CVdd operates at 1.8 V and DVdd is operated at 3.3 V. The VC549 CVdd is 2.5 V and DVdd operate at 3.3 V.

3 Software Wait State Generator [D]

3.1 Wait State Generation

The VC549 is capable of generating up to 7 wait states. The VC5409 is capable of generating up to 14 software wait states. This is achieved with the software wait state multiplier (SWSM) bit which, when set to 1, multiplies the programmed number of software wait states by a factor of two.

The location and field definitions of the software wait state register (SWWSR) are identical on the VC549 and VC5409.

The SWSM bit is located in the software wait state control register (SWCR) at address 0x2B in data space. The structure of this register is shown below.

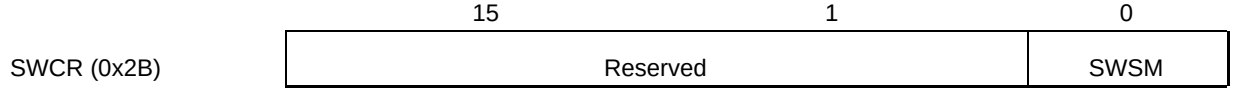

Figure 1. SWCR

SWSM multiplies the number of software wait state set in the SWWSR by 2. Therefore, the VC5409 can be programmed to generate 0, 1, 2, 3, 4, 5, 6, 7, 8, 10, 12 or 14 wait states.

The SWSM bit is cleared at reset. Consequently, the wait state generation scheme on the VC5409 is fully compatible with the VC549.

4 Bank Switching Control Register Differences [D]

The Bank Switching Control Registers (BSCR) on the VC549 and VC5409 are different. The BSCRs for both devices are shown below.

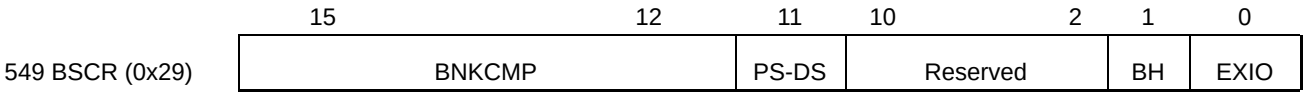

Figure 2. VC549 BSCR

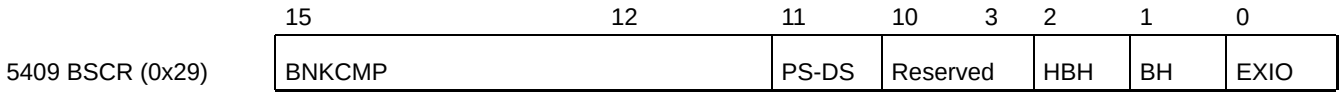

Figure 3. VC5409 BSCR

New field in the VC5409 BSCR:

HBH enables/disables the HPI data bus holders

On the VC5409, the bank size options are 64K, 32K, 16K, 8K, and 4K. An additional bank switching cycle is added when the following conditions occur:

- A memory read followed by another memory read from a different bank.
- A program memory read followed by a data memory read.
- A data memory read followed by a program memory read.
- A program memory read followed by another program memory read from a different page.

5 PLL Clocking Options [H]

The PLL programming and operation on the VC5409 is identical to the VC549. The pin settings CLKMD1, CLKMD2, and CLKMD3 (0/1/1) are still reserved on the VC5409 (similar to the VC549). The VC549 clock mode settings (1/1/1) at reset are no longer reserved on the VC5409. The clock mode changes will dramatically effect hardware designs.

Table 1. VC5409 Clock Mode Settings at Reset

CLKMD1	CLKMD2	CLKMD3	CLKMD RESET VALUE	CLOCK MODE
0	0	0	E007h	PLL x15
0	0	1	9007h	PLL x10
0	1	0	4007h	PLL x5
1	0	0	1007h	PLL x2
1	1	0	F007h	PLL x1
1	1	1	0000h	½ (PLL disabled)
1	0	1	F000h	¼ (PLL disabled)
0	1	1	—	RESERVED (bypass mode)

Table 2. VC549 Clock Mode Settings at Reset

CLKMD1	CLKMD2	CLKMD3	CLKMD RESET VALUE	CLOCK MODE
0	0	0	0000h	Divide-by-two, with external source
0	0	1	1000h	Divide-by-two, with external source
0	1	0	2000h	Divide-by-two, with external source
1	0	0	4000h	Divide-by-two, internal oscillator enabled
1	1	0	6000h	Divide-by-two, with external source
1	1	1	7000h	RESERVED
1	0	1	0007h	PLL x 1 with external clock
0	1	1	—	RESERVED

6 Multichannel Buffered Serial Port (McBSP) [H/S]

On the VC5409, the McBSP has replaced all of the serial ports available on the VC549.

6.1 Register Subaddressing [S]

The entire set of control registers for the McBSPs are dramatically different from the previous BSP. This change was necessary to create greater flexibility on the McBSPs. All of the control registers on the McBSP are now accessed through a register subaddressing scheme. Only the data receive registers (DRR1 and DRR2) and the data transmit registers (DXR1 and DXR2) are directly accessed (not subaddressed).

DRR1 on each McBSP is still mapped to the same location as the VC549 DRRs.

DXR1 on each McBSP is still mapped to the same location as the VC549 DXRs.

Due to these differences, software modification is necessary to configure the McBSPs properly. Software references to DRR and DXR will still work correctly as long as the word length used on the McBSP is 16 bits or less (because DRR2 and DXR2 are only used for word lengths greater than 16 bits).

6.2 McBSP External Interface [D]

The external signals associated with the McBSP (BCLKX, BCLKR, BFSX, BFSR, BDX, BDR) are the same as those on the previous ’C54x serial ports.

6.3 Triple Buffered Receive Path [D]

The receive path on the McBSP is now triple buffered compared to the double buffered paths of the previous ’C54x serial ports.

VC549 receive path: Receive shift register (RSR) Data receive register (DRR)

VC5409 receive path: (RSR) Receive buffer register (RBR) (DRR)

This structural change will manifest itself in two main ways:

- The time delay between the data being shifted in and the data becoming available in the DRR will be different. This will have no impact on applications that either use the receive interrupt or poll the RRDY flag to determine when data is ready.
- The McBSP receiver can receive an additional word (compared to the VC549 serial ports) before overflow occurs. The RFULL flag is now triggered when DRR and RBR are full and DRR is not read before the end of the third word being shifted into RSR.

These differences will generally not affect the operation of most applications.

6.4 TDM Port to McBSP Migration [H/S]

The VC5409 has no dedicated TDM serial port. The McBSP can be programmed to perform a multichannel function similar to the TDM port but it is not identical. The McBSP cannot generate a signal comparable to the TADD signal on the TDM port. Consequently, both hardware and software changes will be necessary to migrate the VC549 TDM port function to the VC5409 McBSP.

6.5 Buffered Serial Port (BSP) to McBSP Migration [S]

The VC5409 McBSP has replaced the VC549 BSP. The data buffering function provided by the BSP autobuffering unit is now accomplished by using the DMA in conjunction with the McBSP. The McBSP performs the serial port function and the DMA controller performs the autobuffering function. Software modifications are required to configure the McBSP and the DMA to operate in this manner.

No hardware changes are necessary to transition from the BSP to the McBSP because the set of externals signals associated with the two ports are the same.

7 VC549 HPI to VC5409 HPI8/16 Migration

7.1 Enhanced HPI8 [H]

The VC5409 HPI in standard 8-bit mode is similar to the VC549 HPI. When the HPI8 mode is not in use, pins HD0–HD7 can be used as general purpose I/O. The HPI8 mode is controlled via the HPI16 pin. This pin must be low for HPI8 operation. The HPI16 pin replaces the no connect pin on the VC549. Hardware modification will need to be considered to insure correct HPI operation.

7.2 HPI8/16 Does not Support Host-only Mode (HOM) [H/S]

The HPI8/16 no longer supports HOM. Data can not be loaded via the HPI during reset.

7.3 Expanded Memory Map [D]

The host port interface of the VC5409 (HPI8/16) is not limited to a 2K block of internal memory. The HPI8/16 uses the DMA controller to gain access to the entire on-chip memory, eliminating the 2K limitation.

7.4 HPI16 Mode [D]

The VC5409 HPI supports 16-bit accesses in non-multiplexed mode. The HPI16 pin controls the 16-bit mode. The HPI16 mode was not available on the VC549. No hardware migration issues are associated with this mode.

8 Memory Map [D]

The memory map of the VC5409 is similar to the VC549 with the following exception:

- 32K of on-chip DARAM is available on the VC5409. 24K of DARAM and 8K SARAM on the VC549.

9 Bootloader/ROM Contents [H/S]

The bootloader options available on the VC5409 are similar but not identical to the VC549.

- **HPI8/16 boot**. In standard 8-bit mode the VC5409 bootloader supports the HPI boot differently from that of the VC549. In the VC5409 bootloader, the HOST must download code into the internal memory of the VC5409 after RESET. Upon completion, the HOST must write the start address of the bootloaded section to 007Fh.

  The bootloader performs an HPI boot only when the memory location at 007Fh has been changed by the HOST. The location 007Fh serves as a pre-initialized pointer to the start address of the bootloaded code. Although the use of the INT2 pin is optional, the INT2 pin is NOT used to indicate an HPI boot.

  – When the INT2 pin is used, the bootloader waits only for the memory location at 007Fh to change. This is to ensure that the other bootload modes are not selected while the HOST is loading on-chip RAM.

  – When the INT2 is not used, all bootmodes, including the HPI address 007Fh, are checked.

- **Parallel boot**. The VC5409 bootloader supports the same parallel boot mode as the VC549 with the following exception. On the VC549, when the location of the boot table is read from I/O address 0FFFFh, the bootloader uses the least significant six bits of the word read as the most significant six bits of the boot table address with the lower bits forced to zeroes. On the VC5409, the word read from I/O space is used without modification as the address of the boot table.

- **Serial boot**. The VC5409 bootloader supports serial boot through the McBSPs. McBSP0 is dedicated to 16-bit data loads. McBSP1–2 are dedicated to 8-bit data loads. McBSP2 can also be used to bootload in SPI EEPROM mode. The SPI boot mode allows the VC5409 to boot from an 8-bit serial EEPROM using the SPI protocol. The mode is selected after reset via the INT3 external interrupt. Proper selection of the boot mode requires high to low

transition on the INT3 pin within 30 CPU cycles after the VC5409 is reset. TDM boot mode is not supported on the VC5409. The McBSPs are configured to boot in the manner of the standard ’C54x serial port.

- **I/O boot**. The VC5409 support for this mode is identical to the VC549.

The VC5409 standard ROM contents other than the bootloader are RESERVED.

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