Migrating from TMS320VC5410 to TMS320VC5409

Philip M. Jones *C5000 Applications Team*

ABSTRACT

This document describes issues of interest related to migration from the TMS320VC5410 to the TMS320VC5409. The objective of this document is to indicate differences between the two devices. Functions that are identical between the two devices are not included. For detailed information on the specific functions of either device, refer to the device data sheets and/or the *TMS320C54x DSP CPU and Peripherals, Reference Set, Volume 1* (SPRU131).

Migration issues from the ’VC5410 to ’VC5409 are indicated with the following symbols:

[S] means software modification is required

[H] means hardware modification is required

[D] means the ’VC5410 and ’VC5409 are different (usually due to added features on the ’VC5409), but no modification is necessary for migration (that is, the devices are different but compatible).

These symbols are included at the beginning of each section.

Contents

Package and Pinout Compatibility 2
Power Supply 2
Memory Map 2
Multichannel Buffered Serial Port (McBSP) 2
DMA Extended Addressing 2
Bank Switching Control Register Differences 4
External Parallel Interface (XIO) 5
CLKOUT Division 5
PLL Clocking Options 5
’VC5410 HPI8 to ’VC5409 HPI8/16 Migration 6
Bootloader/ROM Contents 7

Package and Pinout Compatibility [D]

The ’VC5409 144-pin PGE package has the same footprint as the 5410 PGE.

The test pin, NC pin, has been replaced with an HPI16 pin. This pin controls the function of the HPI8/16 modes. In standard HPI8 mode, HPI16 pin = 0, the ‘5409 Host Port Interface (HPI) is an 8-bit parallel port for inter-processor communication. The default HPI 8-bit mode is controlled by an internal pull down of the HPI16 pin. When in HPI16 mode, HPI16 pin = 1, data pins D0–D15 are internally muxed with the HPI to read/write data from/to internal memory. Address pins A0–A15 are internally muxed to the HPI and used to address the internal memory.

The ’VC5410 is available in two package types:

- 144-pin PGE thin quad flat pack (TQFP)
- 176-pin GGW ball grid array MicroStar BGA™

The ’VC5409 is available in two package types:

- 144-pin PGE thin quad flat pack (TQFP)
- 144-pin GGU ball grid array MicroStar BGA™

Power Supply [H]

The ’VC5410 CVdd operates at 2.5 V and DVdd is 3.3 V. The ’VC5409 CVdd operates at 1.8 V and DVdd is 3.3 V.

Memory Map [S]

The memory map of the ’VC5409 is different from the ’VC5410 memory configuration.

- The ’VC5409 has 32K of on-chip DARAM mapped into addresses 0080h–08000h. The ’VC5410 has 8K of DARAM (0080h–01FFFH) and 24K of SARAM (2000h–7FFFh).
- Setting the DROM bit on the ’VC5409 maps ROM into data space instead of mapping the SARAM2 into data space as on the ’VC5410.
- The ’VC5410 has a 32K SARAM block (018000–01FFFF) of internal extended program memory. Internal extended program memory is not available on the ’VC5409.

Multichannel Buffered Serial Port (McBSP) [D/S]

The ’VC5409 McBSP slightly differs from that of the ’VC5410.

The ABIS modes featured on the ’VC5410 are not available on the ’VC5409. The corresponding DMA ABIS synchronization events are consequently RESERVED on the ’VC5409.

DMA Extended Addressing [S]

The ’VC5409 DMA has extended external memory access that is implemented differently from the ’VC5410. It is imperative that users understand the issues associated with migration from the ’VC5410 DMA to the ’VC5409 DMA.

The ’VC5409 DMA controller has the ability to perform transfers to and from three extended spaces: program, data, and I/O memory space. The destination address space select (DMD) and source address space select (DMS) are used to indicate the space to which data is to be transferred as listed in Table 1 and Table 2.

Table 1. Destination Address Space (DMD)

Name	Reset Value	Description
DMD	0	DMA Destination Address Space Select Bit SIND = 00 Program SIND = 01 Data SIND = 10 I/O SIND = 11 Reserved

Table 2. Source Address Space (DMS)

DMS	0	DMA Source Address Space Select Bit DIND = 00 Program DIND = 01 Data DIND = 10 I/O DIND = 11 Reserved

Two bits fields, SLAXS and DLAXS (Figure 1), in the DMA transfer mode control register (DMMCRn), are used to select DMA external access.

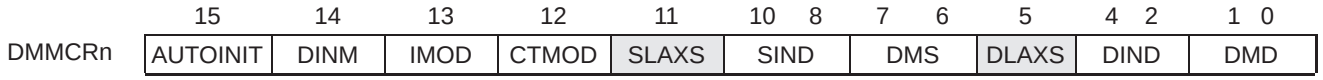

Figure 1. DMA Transfer Mode Control Register. (DMMCRn)

The source look ahead external space is used to indicate the source page is external to the device, SLAXS = 1 (Table 3).

Table 3. Source Look Ahead External Space

Name	Reset Value	Description
SLAXS	0	SLAXS = 0 Source page internal SLAXS = 1 Source page external

The destination look ahead external space is used to indicate that the destination page is external to the device, DLAXS = 1 (Table 4).

Table 4. Destination Look Ahead External Space

Name	Reset Value	Description
DLAXS	0	DLAXS = 0 Destination page internal DLAXS = 1 Destination page external

Setting the bit fields SLAXS and DLAXS does not globally apply to all DMA channels. When these bits are cleared, the DMA controller assumes internal transfers.

Four subaddressed registers are also employed to provide external DMA capabilities:

- The DMA source program page address register (DMSRCP)
- The DMA destination program page register (DMDSTP)
- The DMA global extended source register (XSRCDP)
- The DMA global extended destination register (XDSTDP).

The DMSRCP and DMDSTP contain the 7-bit extended program page number for the source and destination location, respectively. The XSRCDP and XDSTDP contain the 7-bit source and destination addresses for external data and I/O spaces. These registers apply to all DMA channels programmed for external transfers. The least significant seven bits are used to store the extended address page of the source and destination address as shown in Figure 2. Following reset, these registers are initialized to 0000h, or program, data, I/O page 0. The reserved bit locations are always read as 0.

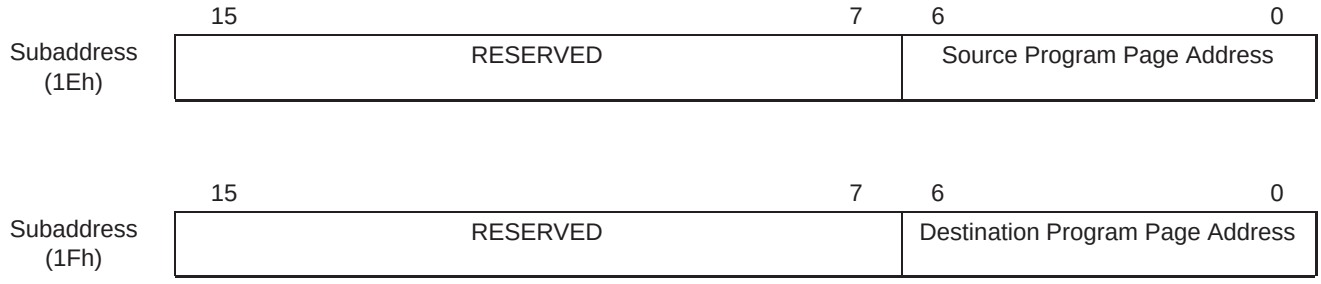

Figure 2. DMA Source and Destination Page Address Register DMSRCP/ DMDSTP. (Program)

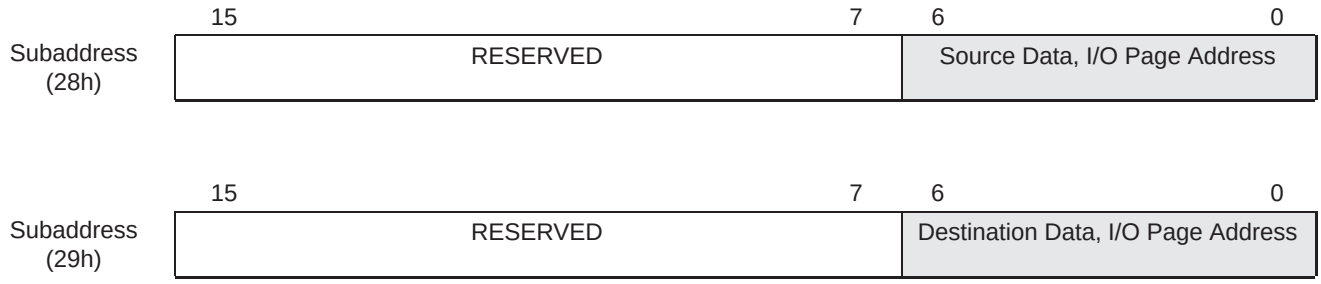

Figure 3. DMA Source and Destination Page Address Register XSRCDP/ XDSTDP. (Data, I/O)

Bank Switching Control Register Differences [S]

The Bank Switching Control Registers (BSCR) on the ’VC5410 and ’VC5409 are different. The BSCRs for both devices are shown in Figure 4.

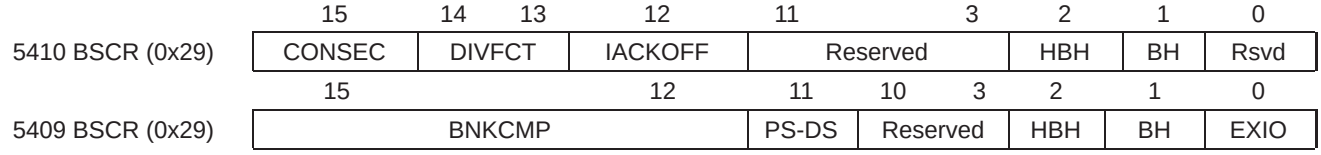

Figure 4. Bank Switching Control Registers

Due to the differences between the two versions of the BSCR, software modification is necessary.

The CONSEC field of the 5410 BSCR is replaced functionally with the BNKCMP and PS-DS fields of the ’VC5409 BSCR. The ’VC5410 has a different external parallel interface from the ’VC5409. The signals are identical but the operation of the signals is different. The BNKCMP determines the external memory bank size. The ’VC5409 supports 4K to 64K word bank sizes. The program read and data read fields (PS-DS) insert an extra cycle between consecutive program reads and data reads. EXIO, external-bus-off function, gates the external address and data bus signals after completing the current bus cycle.

New fields in the ’VC5409 BSCR are listed in Table 5.

Table 5. New Fields in the ’VC5409 BSCR

BNKCMP	Controls the external memory bank size. Additional cycles are added when: • A memory read followed by another memory read from a different bank. • A program memory read followed by another program memory read from a different page.
–	Controls the external timing between program/data reads. An additional cycle is added when: • A data memory read is followed by a program memory read. • A program memory read is followed by a data memory read.
EXIO	Controls the address and data bus signals activity after completing the current bus cycle.

The DIVFCT and IACKOFF fields and functions in the ’VC5410 BSCR no longer exist on the 5409.

External Parallel Interface (XIO) [D]

The signals on the ’VC5409 external parallel interface are not identical to all modes on the ’VC5410.

The timing of the external parallel interface signals are different on the ’VC5409. The ’VC5409 interface does not support additional leading and trailing cycles on external accesses. This is generally a compatibility issue with the ’VC5409. External accesses now take a different amount of time than before. This difference should be considered if the application to be migrated is highly bandwidth-limited based on the operation of the external parallel interface. Otherwise, the ’VC5409 interface is compatible.

CLKOUT Division [H/S]

The DIVFCT field in the BSCR on the ’VC5410 controls whether the CLKOUT represents the CPU clock divided by 1, 2, 3 or 4. On the ’VC5409, CLKOUT always represents the CPU clock. The DIVFCT field and function are not available on the ’VC5409.

PLL Clocking Options [H]

The PLL programming and operation on the ’VC5409 is identical to the ’VC549. The pin settings CLKMD1, CLKMD2, and CLKMD3 (0/1/1) are reserved on the ’VC5409 (different from the ’VC5410). The ’VC5410 clock mode settings (1/1/1) at reset are no longer reserved on the ’VC5409. The clock mode changes will dramatically effect hardware designs.

Table 6. 5409 Clock Mode Settings at Reset

CLKMD1	CLKMD2	CLKMD3	CLKMD RESET VALUE	CLOCK MODE
0	0	0	E007h	PLL x15
0	0	1	9007h	PLL x10
0	1	0	4007h	PLL x5
1	0	0	1007h	PLL x2
1	1	0	F007h	PLL x1
1	1	1	0000h	½ (PLL disabled)
1	0	1	F000h	¼ (PLL disabled)
0	1	1	—	RESERVED (bypass mode)

Table 7. 5410 Clock Mode Settings at Reset

CLKMD1	CLKMD2	CLKMD3	CLKMD RESET VALUE	CLOCK MODE
0	0	0	0000h	Divide-by-two, with external source
0	0	1	1000h	Divide-by-two, with external source
0	1	0	2000h	Divide-by-two, with external source
1	0	0	4000h	Divide-by-two, internal oscillator enabled
1	1	0	6000h	Divide-by-two, with external source
1	1	1	7000h	RESERVED
1	0	1	0007h	PLL x 1 with external clock
0	1	1	—	Stop Mode

’VC5410 HPI8 to ’VC5409 HPI8/16 Migration

The enhanced 8-bit host port interface (HPI8) on the ’VC5410 is similar in some functions to the standard ’VC5409 HPI.

Expanded memory map [S]

The HPI8 can access the ’VC5410 on-chip memory on program page 1 by setting the XHPIA field in the HPIC to one. The ’VC5409 does not have extended internal program memory; therefore, the XHPIA field and function is not present on the ’VC5409. For this reason, some host software modification may be required. The external signals associated with the HPI8 are identical to those on the standard HPI so no hardware modification is necessary.

The HPI can be used as a 16-bit HPI in nonmultiplexed mode (HPI16=1). The HPI-16 nonmultiplexed mode does not support the use of the HPID, HPIA registers. Host-to-DSP and DSP-to-Host interrupts are also not supported in HPI16 mode. When in the HPI16 mode, pins HD0–HD7 can be used as general purpose I/O. Without configuring the HPI16 pin correctly, the external memory interface is not compatible to the ’VC5410.

The ’VC5409 does not support HOM during reset.

Bootloader/ROM Contents [H]

The bootloader options available on the ’VC5409 are similar but not identical to the ’VC5410.

- **HPI8 boot**. The ’VC5409 does not support host access during reset. In the ’VC5409 bootloader, the HOST must download code into the internal memory of the ’VC5409 after RESET. Upon completion, the HOST must write the start address of the bootloaded section to 007Fh.

  The bootloader performs an HPI boot only when the memory location at 007Fh has been changed by the HOST. The location 007Fh serves as a pre-initialized pointer to the start address of the bootloaded code. Although the use of the INT2 pin is optional, the INT2 pin is NOT used to indicate an HPI boot.

  – When the INT2 pin is used, the bootloader waits only for the memory location at 007Fh to change. This is to ensure that the other bootload modes are not selected while the HOST is loading on-chip RAM.

  – When the INT2 is not used, all bootmodes, including the HPI address 007Fh, are checked.

- **Parallel boot**. The ’VC5409 bootloader support for this mode is identical to the ’VC5410.

- **Serial boot**. The ’VC5409 bootloader supports serial boot through the McBSPs. McBSP0 is dedicated to 16-bit data loads and McBSP1/2 are dedicated to 8-bit data loads. McBSP2 also is reserved for SPI mode EEPROM serial boot mode. The McBSPs are configured to boot in the manner of the standard ’C54x serial port.

- **I/O boot**. The ’VC5409 support for this mode is identical to the ’VC5410.

The other standard ROM contents are RESERVED on the ’VC5409.

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