How to Begin Development With the TMS320C6205 DSP

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ABSTRACT

This document highlights the similarities and differences between the TMS320C6205 digital signal processor (DSP) and other TMS320C6000™ devices. The similarities allow Tools designed for other C6000™ DSPs to be used to develop software for the C6205. A listing of these tools and documents that aid in development is presented.

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The TMS320C6205 is one of the devices in the TMS320C6000™ DSP platform of high-performance digital signal processors (DSPs). The C6205 is a version of the original C6000™ DSP device, the C6201B, with the new peripheral interface to the PCI bus in addition to other enhancements. The C6205 is capable of achieving 1600 MIPS (million instructions per second) at 200 MHz.

Introduced in February 1997, the C6000™ DSP platform is based on TI's VelociTI™ architecture, an advanced very long instruction word (VLIW) architecture for DSPs. Figure 1 shows the roadmap for the fixed–point generation of the C6000™ DSP platform.

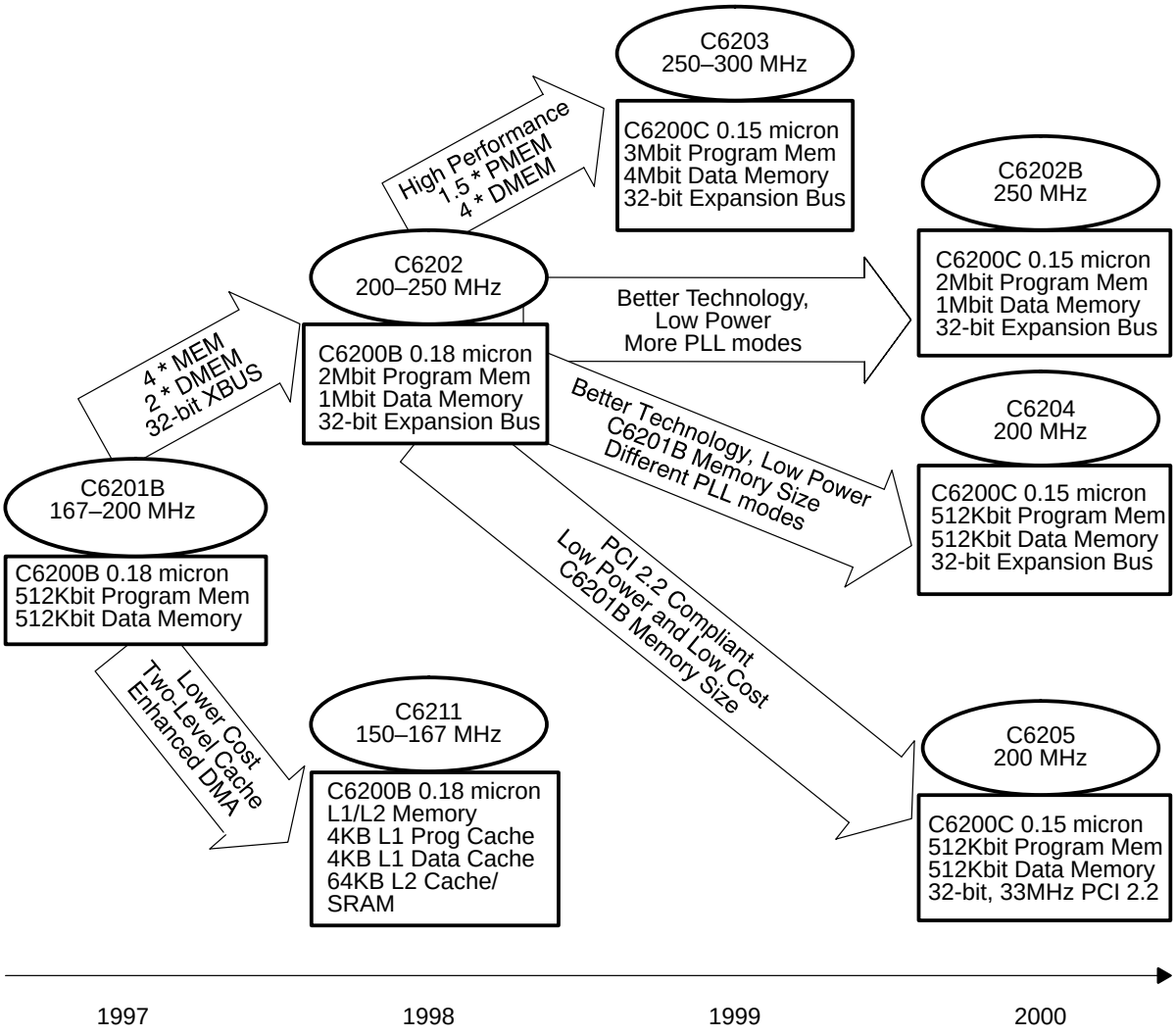

Figure 1. TMS320C6200 Fixed-Point Roadmap

2 TMS320C6000 Compatibility

All C6000™ DSP devices are code-compatible with one another, with the exception that there are some floating–point instructions that are only valid on the floating-point (TMS320C67x™) members. All of the TMS320C62x™ fixed-point devices are based on the same CPU core designed to achieve high performance through increased instruction-level parallelism. Surpassing the throughput of traditional superscalar designs, VelociTI provides eight execution units, including two multipliers and six arithmetic logic units (ALUs). These units operate in parallel and can perform up to eight instructions during a single clock cycle-up to 1600 MIPS at 200 MHz.

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VelociTI's advanced features include instruction packing, conditional branching, variable-width instructions, and prefetched branching, all of which eliminate problems that were previously associated with VLIW implementations. The architecture is highly deterministic, with few restrictions on how or when instructions are fetched, executed, or stored. This architectural flexibility is key to the breakthrough efficiency levels of the C6000™ DSP compiler.

This common architecture allows designers to begin development with existing C6000™ DSP software tools for those devices currently in development. This also allows for migration from one C6000™ DSP processor to another, as design requirements require.

In addition to the CPU, many of the on-chip peripherals are common between C6000™ DSP devices. Figure 2 shows a block diagram of the C6205. The blocks in gray are shared between the C6201 and C6205. It is important to note that the PCI module is the only truly different aspect of the C6205.

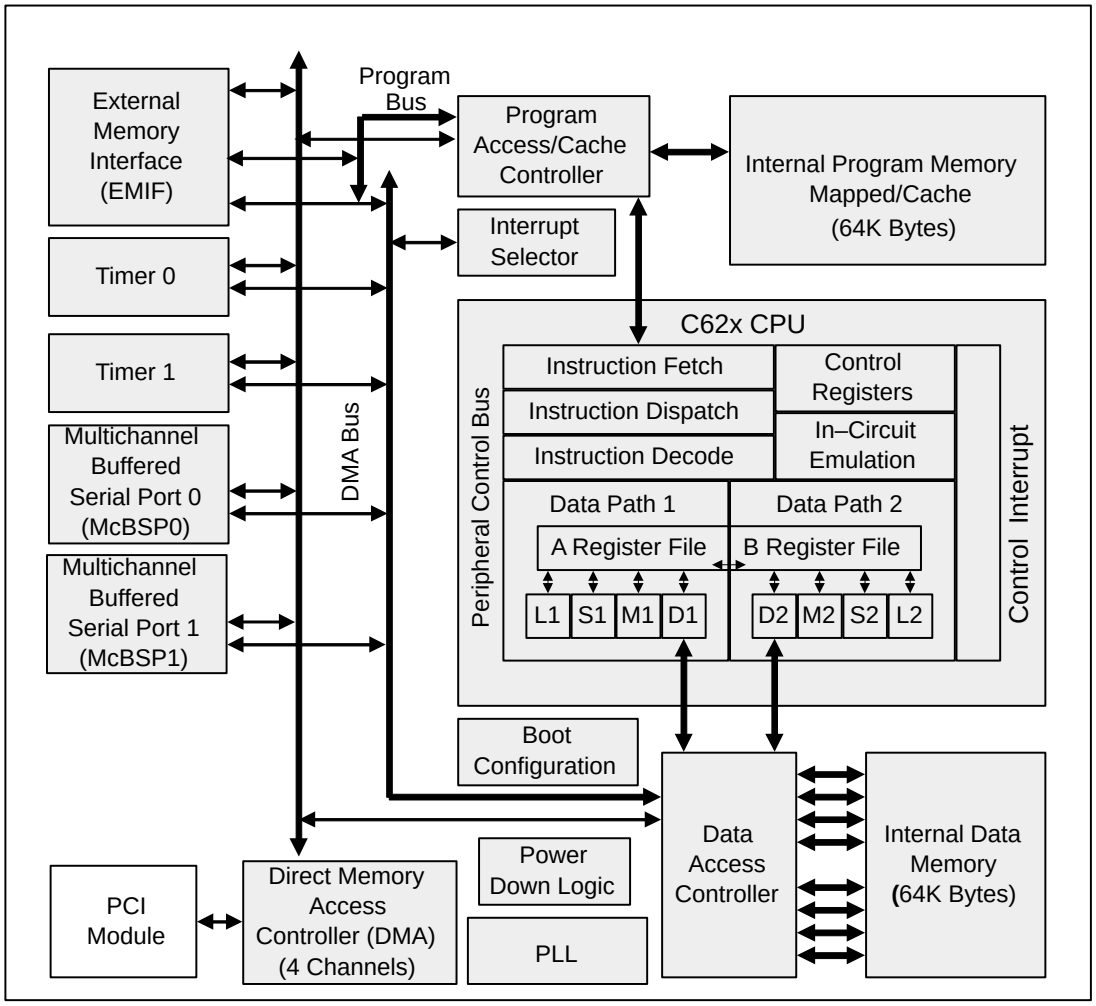

Figure 2. TMS320C6205 DSP Block Diagram

2.1 Similarities Between C6205 and C6201B DSPs

The C6205 is highly-compatible with the first C6000™ DSP device, the C6201 and C6201B. The following device components are identical between the devices:

- **CPU:** The CPU of the C6205 is identical to that of the C6201B, which means that code written for the C6201 will run unmodified on the C6205.
- **Multichannel Buffered Serial Ports (McBSPs):** The McBSPs are unchanged on the C6205.
- **32-bit timers:** Two timers are on the C6205.
- **Interrupt selection:** There are 16 interrupt sources that may be used to interrupt the CPU or send an event to the DMA.
- **Internal memory spaces:** Both have 64K bytes each of program and data memory.

2.2 Differences Between the C6205 and C6201B DSPs

Several enhancements have been made to allow the C6205 greater performance capability. These include:

- **External Memory Interface (EMIF):** The EMIF has been modified slightly to reduce the pin count of the C6205. Synchronous DRAM (SDRAM) and Sync-Burst SRAM (SBSRAM) share control signals on the EMIF bus. The two are mutually exclusive, so only one of the two memory types is permissible in a system.
- **Direct Memory Access (DMA) controller:** Throughput enhancements have been made to the 4–channel DMA controller. Each channel now has a dedicated 9-deep FIFO; thus, avoiding arbitration for a single FIFO. More information is available in the *How to Begin Development and Migrate Across the TMS320C6202/C6202B/C6203/C6204 DSPs* application report (SPRA603).
- **PCI module:** The PCI module has been added to the C6205 to replace the Host Port Interface (HPI) of the C6201B. The PCI module functions as a high performance 32-bit Master/Slave PCI Plug-and-Play interface supporting 33 MHz for desktop applications. The PCI interface is compatible with the Revision 2.2 PCI Local Bus Specification. It implements PCI master and slave targets at 33 MHz, with 32-bit data and address. The module contains the requisite configuration registers, parity generation, parity- and system-error detection and reporting (PERR#, SERR#), and power management capabilities.
- **4–Wire EEPROM serial port interface:** TMS320C6205 allows the PCI configuration space registers to be loaded from an external serial EEPROM. The PCI module without DSP intervention performs the autoinitialization process.
- **PLL modes:** The TMS320C6205 PLL has x1, x4, x6, x7, x8, x9, x10, and x11 multiply options configured using CLKMODE0 pin and pullup/down resistor on the EMIF data pins.
- **Better process technology:** The C6205 uses 15C05 (0.15μm) process technology; thereby, providing lower core voltage and lower power.
- **Boot–Mode configuration:** The TMS320C6205 is configured using pullup/down resistors on the EMIF data bus.

3 Begin Writing Code for the C6205

The identical CPUs in the C6205 and C6201 devices allow for code to be written for the C6205 using existing C6000™ DSP tools. C6201 code will require no modification to use on the C6205. All peripheral-specific code, with the exception of the PCI module, will also be able to run unchanged on the C6205.

The C6000™ DSP compiler may be used for all members of the C6000™ DSP device platform. Fixed–point devices are object-code-compatible, so code written for the C6201 may be used by the C6205.

Code development for the C6205 may begin using the C6000™ DSP fast simulator. The simulator provides a cycle-accurate account of device performance, assuming that all on-chip memory is used for code and data. The simulator provides a good environment to learn the C6000™ DSP VLIW architecture.

The standard C6000™ DSP simulator may be used to incorporate peripheral support. C6205 designs may be worked out in detail on the simulator prior to purchasing actual silicon, with cycle-accurate accounts of peripherals performance.

For a development start in hardware, the C6201 EVM may be used to understand the C6000™ DSP functionality. With the exception of the PCI module, all of the peripherals on the C6205 are identical to those of the C6201, so the EVM is a good tool to understand how to incorporate the peripherals into a real-time system.

3.1 C6000 Tools Support

C6000™ DSP tools are available now for use in all C6000™ DSP designs. The C6000™ DSP development tools available are:

- Code Composer Studio™ IDE, which includes Code Composer Studio-Compile Tools and Code Composer Studio-Debug Tools
- C6000™ DSP Simulator Software
- C6000 DSP Optimizing C Compiler/Assembler
- XDS510 C6000 C Source Debugger Software
- XDS510 Emulator Hardware with JTAG Emulation Cable
- TMS320C6201 Evaluation Module (EVM)
- TMS320C6201 Multichannel Evaluation Module (McEVM)
- TMS3206211 DSP Starter Kit (DSK)

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4 References

1. *TMS320C6000 CPU and Instruction Set Reference Guide* (SPRU189).
2. *TMS320C6000 Peripherals Reference Guide* (SPRU190).
3. *TMS320C6000 Technical Brief* (SPRU197).
4. *TMS320C6000 Programmer's Guide* (SPRU198).
5. *TMS320C6201/6701 Evaluation Module Reference Guide* (SPRU269).
6. *TMS320C6x Peripheral Support Library Programmer's Reference* (SPRU273).
7. *TMS320C6x Assembly Language Tools User's Guide* (SPRU186).
8. *TMS320C6x Optimizing C Compiler User's Guide* (SPRU187).
9. *TMS320C6x C Source Debugger User's Guide* (SPRU188).
10. *TMS320C6x C Source Debugger For SPARCstations* (SPRU224).

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