Using Boundary Scan on the TMS320VC5421 DSP

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ABSTRACT

The TMS320VC5421 DSP (hereafter referred to as VC5421) is a dual-core processor implementing standard IEEE 1149.1 boundary scan capability. This application report contains a description of the VC5421 boundary scan implementation and information about how to use it with other boundary scan tools and devices.

The material covered in this application report assumes the reader is familiar with the boundary scan concepts defined by IEEE Standard 1149.1. An overview of these concepts is presented in the IEEE Std 1149.1 (JTAG) Testability Primer (literature number SSYA002). For detailed information on the operation and requirements for boundary scan, refer to the IEEE standard itself. Copies of the standard are available from IEEE at 1-800-678-IEEE.

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1.1 VC5421 Silicon Revision Requirements

The VC5421 boundary scan implementation described in this document applies to all silicon revisions.

1.2 Full Observe and Control Capability

Unlike the VC5420, the VC5421 implements standard observe and control capability with respect to the IEEE Standard 1149.1. This means all pins with input functions (input or I/O pins) have observe capability and all pins with output functions (outputs and I/O pins) have control capability. Consequently, there are no testability limitations due to limited control capability as was present on the VC5420.

1.3 VC5421 Hardware Requirements for Boundary Scan Test

Boundary scan test requires control of the five test access port signals (TMS, TCK, TDI, TDO and $\overline{\text{TRST}}$) as described in IEEE standard 1149.1. Two additional signals, EMU0 and EMU1/$\overline{\text{OFF}}$, are used by TI DSPs to provide emulation debug capability through the JTAG test access port. These signals are also used by TI for scan-based factory tests.

During boundary scan tests, EMU0 and EMU1/$\overline{\text{OFF}}$ must be held high while $\overline{\text{TRST}}$ is transitioned from low to high. This operation sets the correct internal test mode for boundary scan test to be performed. EMU0 and EMU1/$\overline{\text{OFF}}$ should be pulled high through 4.7k ohm pullup resistors on each pin. The pullup resistors are connected to the DVdd power supply for the VC5421.

Boundary scan ATPG tools should be configured to cycle $\overline{\text{TRST}}$ prior to beginning boundary scan tests to ensure that the device is in the proper test mode.

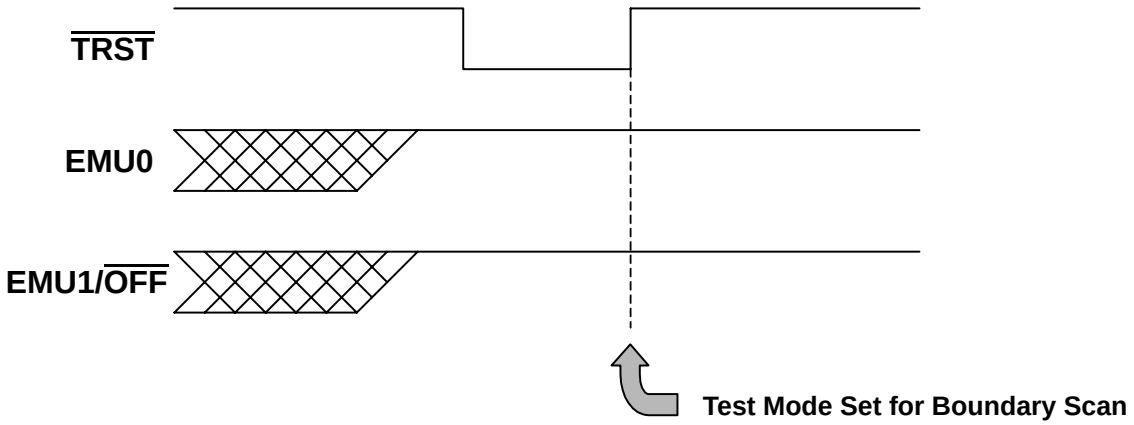

Figure 1. Initialization for Boundary Scan Test Mode using TRST, EMU0 and EMU1/OFF

1.4 VC5421 Boundary Scan Pin Coverage

All digital pins (102 pins) on the VC5421 have boundary scan cells for test with the following exceptions. The device pins not testable through boundary scan are shown below in Table 1.

Table 1. Device Pins Not Testable Through Boundary Scan

Pin	Pin Function
DVdd, CVdd, Vss, AVdd, Vssa	Power supply pins
TEST	Factory test pins
TMS, TCK, TDI, TDO, $\overline{\text{TRST}}$	JTAG test access pins
EMU0, EMU1/$\overline{\text{OFF}}$	Emulation test pins

1.5 VC5421 Boundary Scan Description Language (BSDL) Implementation

A representation of the internal structure of the VC5421 with respect to boundary scan is shown in Figure 2. The VC5421 is composed of two internal processors called subsystems. Each subsystem has its own independent TAP controller to provide boundary scan test and emulation capability. The device signals TMS, TCK and $\overline{\text{TRST}}$ are connected to each subsystem in parallel. The device TDI is connected to subsystem A. The internal equivalent of TDO for subsystem A is connected to the internal TDI for subsystem B. The output of the chain from subsystem B is connected to the device TDO. To a boundary scan test system, this structure is equivalent to treating the subsystems as independent devices.

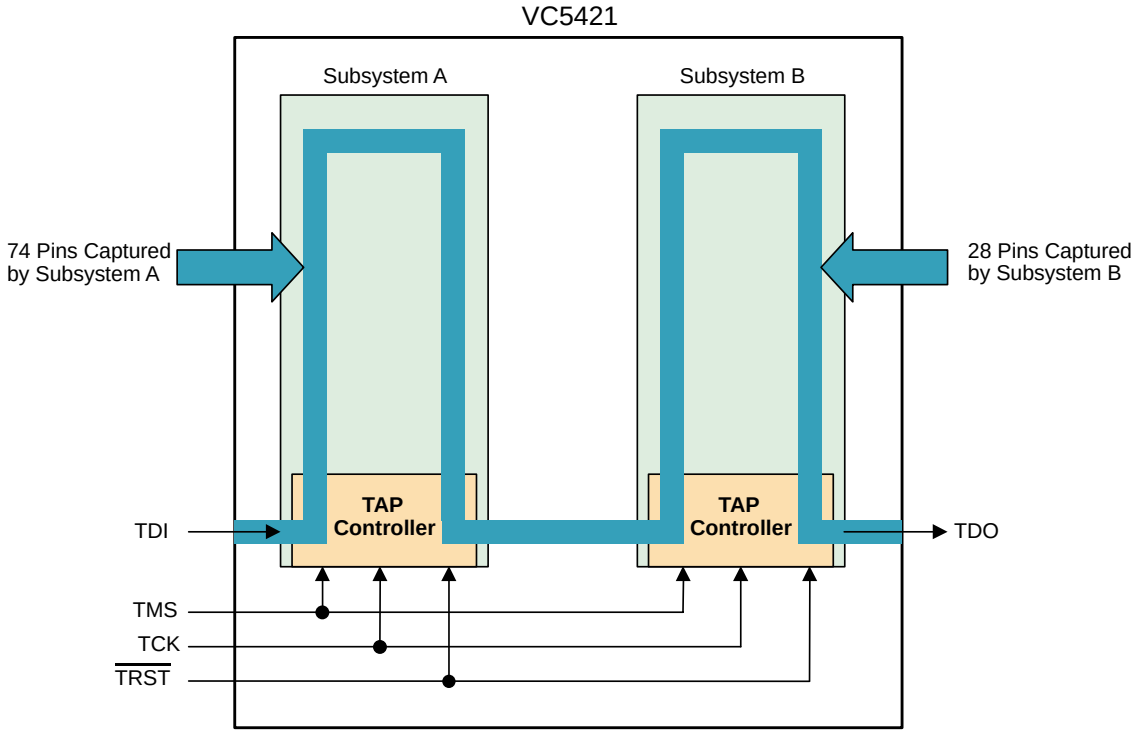

Figure 2. Boundary Scan Structure of the VC5421

The two subsystems have the ability to capture unique groups of pins on the device. Subsystem A captures 74 pins which include the pins associated uniquely with subsystem A and the device pins that are common to both subsystems. Subsystem B captures only the device pins associated with subsystem B. The pins captured by each subsystem are listed in Table 2.

Table 2. Pins Captured by each VC5421 Subsystem During Boundary Scan Test

Subsystem	Pins			Description
A	A_BCLKR [0:2] A_BCLKX [0:2]	A_BDR [0:2] A_BDX [0:2]	A_FSR [0:2] A_FSX [0:2]	McBSP signals
	A_CLKOUT	CLKIN		Clock signals
	A_GPIO[0:3]	A_XF		General Purpose I/O signals
	$\overline{\text{A\_INT}}$[0:1]	$\overline{\text{A\_NMI}}$	$\overline{\text{A\_RS}}$	Interrupt signals
	$\overline{\text{HOLD}}$	$\overline{\text{HOLDA}}$		Bus Hold Signals
	XIO	SELA/B		Mode control signals
	$\overline{\text{HCS}}$ HMODE HR/$\overline{\text{W}}$	$\overline{\text{HDS1}}$ HPIRS	$\overline{\text{HDS2}}$ HRDY	HPI-16 signals
	HA[0:17] / PPA[17:0]			Address bus
	HD[0:15] / PPD [15:0]			Data bus
B	B_BCLKR [0:2] B_BCLKX [0:2]	B_BDR [0:2] B_BDX [0:2]	B_FSR [0:2] B_FSX [0:2]	McBSP signals
	B_CLKOUT			Clock signals
	B_GPIO[0:3]	B_XF		General Purpose I/O signals
	$\overline{\text{B\_INT}}$[0:1]	$\overline{\text{B\_NMI}}$	$\overline{\text{B\_RS}}$	Interrupt signals

Although ATPG tools vary in how they describe system level structure, all tools provide a method to describe the order of the devices in the scan chain. The BSDL description of the VC5421 is implemented as 2 BSDL files, one for each subsystem. These two boundary scan objects must always be paired and described to the ATPG tools in the proper order. Subsystem B must be described as the subsystem closer to TDO. If the order is reversed, tests generated by the ATPG tools will be incorrect.

Since the connection between the scan chains of the two subsystems is internal to the device, some ATPG tools may issue a warning or error indicating that the TDO-TDI connection between the two subsystem objects is not present. In this case, the device can be modeled as a multi-chip module using the hierarchical capabilities of the ATPG tool. Many boundary scan systems have hierarchical scan chain descriptions where, for example, a plug-in module may be described as a sub-chain to the main boundary scan chain. The model for the sub-chain is generated separately, and then referenced in the description of the main boundary scan chain. The same approach can be used to model the VC5421 as a single object if necessary. The device can be modeled as a sub-chain composed of subsystem A and subsystem B, shown in Figure 3. Then, the VC5421 can be referenced in the main description of the scan chain as a single device “module”. Since the methods to describe hierarchical and modular systems are tool dependent, a single method cannot be described here. It will be necessary to contact the ATPG tool vendor regarding how this procedure is done on their tool. Given the BSDL files for each subsystem and the information in this document, a model can be generated.

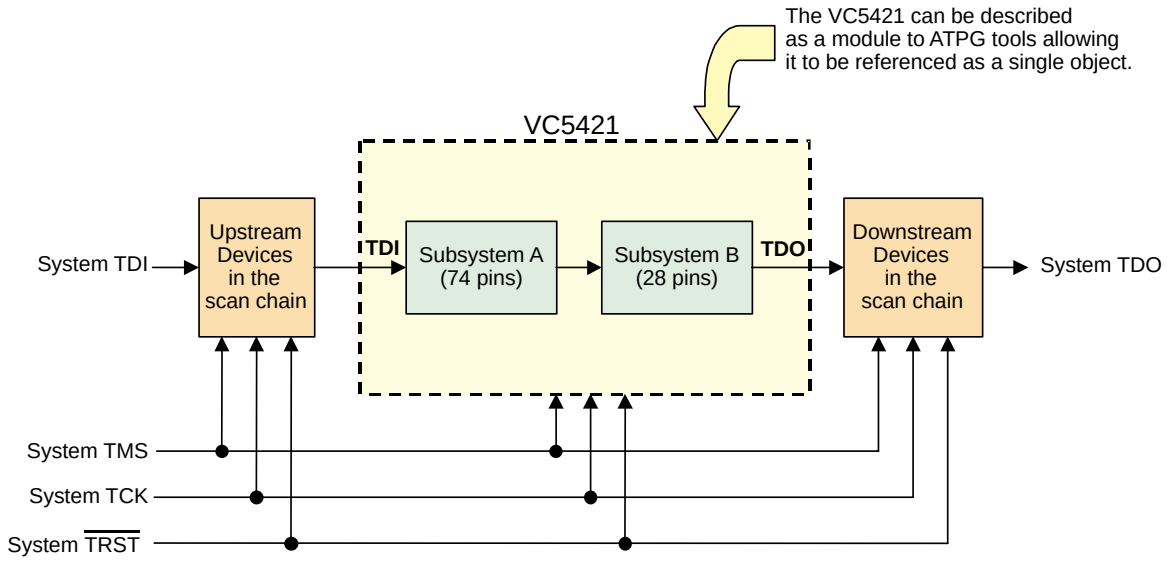

Figure 3. The VC5421 Subsystems Modeled as a “Module” in the Scan Chain

Separate BSDL files are provided for subsystem A and subsystem B. Current VC5421 BSDL files and information are available on the web at:

http://www.ti.com/sc/docs/tools/dsp/ftp/c54x.htm

1.6 VC5421 Boundary Scan Instruction Implementation

The VC5421 implements the following instructions for boundary scan:

- SAMPLE/PRELOAD
- EXTEST
- BYPASS
- HIGHZ

IEEE standard 1149.1 specifies that the SAMPLE/PRELOAD instruction samples inputs and preloads but does not drive outputs. During the SAMPLE/PRELOAD instruction, the device pins maintain their normal functional behavior. The behavior of the VC5421 during execution of this instruction is consistent with the specification in the standard.

IEEE standard 1149.1 specifies that the EXTEST instruction samples inputs, and loads and drives outputs. During the EXTEST instruction, all device pins function as boundary scan inputs or outputs depending on their function. The behavior of the VC5421 during execution of this instruction is consistent with the specification in the standard.

IEEE standard 1149.1 specifies that the BYPASS instruction maps a one-bit bypass register between TDI and TDO (to minimize the chain length when a device is not being tested) and the device pins operate in their normal functional (non-test) mode. The behavior of the VC5421 during execution of this instruction is consistent with the specification in the standard. Note that the VC5421 has one bypass bit for each subsystem (since there is a TAP controller for each subsystem) for a total of two bits between the device TDI and TDO. This behavior is accounted for (and maintains compliance with IEEE standard 1149.1) through the use of separate BSDL files for each subsystem.

IEEE standard 1149.1 specifies that the HIGHZ instruction places the bypass register in the scan chain and causes all output pins (either dedicated outputs or I/O pins) to enter a high-impedance state. The behavior of the VC5421 during execution of this instruction is consistent with the specification in the standard.

None of the other boundary scan instructions specified as optional in IEEE standard 1149.1 are implemented on the VC5421.

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