Migrating from TMS320VC5409 to TMS320VC5416

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ABSTRACT

This document describes issues of interest related to migration from the TMS320VC5409 to the TMS320VC5416. The objective of this document is to indicate differences between the two devices. Functions that are identical between the two devices are not included. For detailed information on the specific functions of either device, refer to the following data sheets and reference guides: TMS320VC5409 (SPRS082), TMS320VC5416 (SPRS095), the *TMS320C54x DSP CPU and Peripherals, Reference Set, Volume 1* (SPRU131) and the *TMS320C54x DSP Enhanced Peripherals, Reference Set, Volume 5* (SPRU302).

Migration issues from the TMS320VC5409 to TMS320C5416 are indicated with the following symbols:

[S] means software modification is required.

[H] means hardware modification is required.

[D] means the VC5409 and VC5416 are different (usually due to added features on the VC5416) but no modification is necessary for migration (i.e. different but compatible).

These symbols are included at the beginning of each section.

Contents

1 Pin and Package Compatibility

The VC5409 and the VC5416 are pin compatible.

The VC5409 is available in two package types:

- 144-pin PGE thin quad flat pack (TQFP)
- 144-pin GGU ball grid array MicroStar BGA

The VC5416 is available in two package types:

- 144-pin PGE thin quad flat pack (TQFP)
- 144-pin GGU MicroStar BGA

2 Power Supply [H]

The VC5409 CVdd operates at 1.8V and DVdd operates at 3.3V.
The VC5416 CVdd operates at 1.5V and DVdd operates at 3.3V.

There is no hard restriction on the power-up/down sequencing. Either CVdd or DVdd can be powered up first.

3 Clock Mode Settings at Reset [D]

The programming and operation of the VC5409 PLL is similar to the VC5416. However, the clock mode settings at device reset are different for the two devices, specifically at the CLKMD1, CLKMD2, and CLKMD3 setting of ’0–0–0’. Refer to the data sheets on VC5409 (SPRS082) and VC5416 (SPRS095) for more details.

Note that the VC5416 does not support the clock mode of internal oscillator with external crystal.

4 Multichannel Buffered Serial Port (McBSP) [H/S]

The VC5416 McBSP differs from the McBSP on the VC5409. The VC5416 McBSP has been enhanced:

- To allow all 128 channels of a 128-channel bit stream to be enabled simultaneously
- To enable the receive clock pin (BCLKR) or the transmit clock pin (BCLKX) to be configured as the input clock to the sample rate generator.

Three control bits and twelve registers have been added to enable the 128 channel selection.

Refer to the VC5416 data sheet (SPRS095) for more details.

5 Host Port Interface (HPI) [H/S]

The HPI units on both VC5409 and VC5416 devices are functionally identical in their interface to 16-bit host devices.

6 DMA External and Extended Memory Transfer [S]

The VC5409 and VC5416 DMA controllers are very similar. The DMA on the VC5416 has one improvement over the VC5409 DMA, as listed below.

6.1 Auto-initialization [S]

TheVC5416 has been enhanced to include one set of independent global reload registers per DMA channel. Each DMA channel now has its own global reload register set. For example, the DMA channel 1 has DMGSA1, DMGDA1, DMGCR1, and DMGFR1 registers as its global registers. Refer to the VC5416 datasheet for more details.

7 Memory Map [D]

The on-chip memory map of the VC5416 is similar to the VC5409 with the following exceptions:

- 64Kw of additional on-chip SARAM is mapped into addresses 028000h–02FFFFh, and 038000h–03FFFh in program space when the VC5416 is in the microcomputer mode.
- The VC5416 has a total of 64Kw (8–8Kw blocks) DARAM while the VC5409 has 32Kw (4–8Kw blocks) DARAM.

8 CLKOUT and External Memory Access Timing [H/S]

The VC5409 is available as an 80MHz and 100MHz part with cycle times of 12.5ns and 10ns, respectively. The V5416 is available as a 160MHz part with a 6.5ns cycle time.

On the VC5409, CLKOUT always represents the CPU clock. On the VC5416, the DIVFCT field in the BSCR controls whether the CLKOUT represents the CPU clock divided by 1, 2, 3 or 4.

Differences in processor speed rating will have a direct effect on access times that need to be considered when interfacing with external memory devices. Access time information will also determine the need for introducing software wait states. Please check the external memory timing information in the datasheets for both processors for more specific details on external memory access times.

9 Bootloader/ROM Contents [H]

The bootloader options available on the VC5416 are similar to the VC5409 with the following exception:

- **HPI boot:** The C5409 HPI boot mode does not require the setting of the interrupt 2 (INT2) flag for selection. If INT2 is not active, the bootloader periodically checks various boot sources, including the polling for HPI boot described above, until a boot condition is detected.

Refer to the TMS320VC5416 and TMS320VC5409 Bootloader application reports (literature number SPRA602 and SPRA627, respectively) for more details.

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