Solano™ Communications IC Enables TMS320C6000 DSP Multiprocessing

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ABSTRACT

Spectrum Signal Processing's Solano™ Communications IC provides high-bandwidth communication paths for multiple processors and I/O modules. Solano's four full-duplex, high-speed LVDS links provide an aggregate bandwidth of over 13.6 Gbps per node. A network of DSPs implemented using this IC provides system throughput that can be many times higher than that offered by conventional bussed or serial link communications.

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1 Introduction

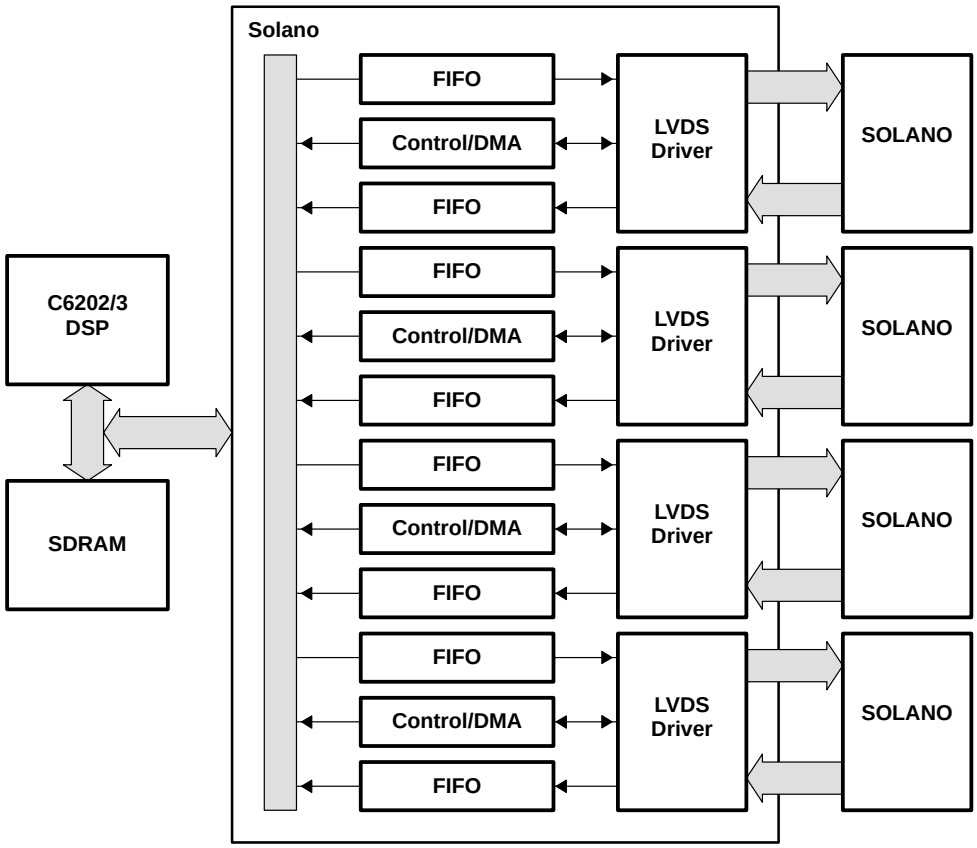
The Solano Communications IC is a high throughput, off-the-shelf solution for the telecommunications infrastructure marketplace. Mobile phone users around the globe want wireless access not only to superior voice communications, but also to broadband "wireless web" Internet services, videoconferencing, high data rate multimedia services, and corporate intranets. These 3G demands exceed the limits of traditional wireless base station processing architectures. In addition, flexible software defined radio architectures are required for dealing with the multiple air-interface standards proliferating throughout the industry, including Wideband Code Division Multiple Access (W-CDMA), cdma2000, and the existing 2G standards.

The new wireless environment calls for base stations transceivers equipped with a mix of signal processing devices, including DSPs and Application Specific Integrated Circuits (ASICs). To alleviate the challenge of integrating this multitude of processors in a base-station architecture, Spectrum is offering the Solano IC directly to telecommunications infrastructure providers.

The Solano Communications IC provides flexible, high-bandwidth communication paths for multiple processors and I/O modules. A data network implemented using this IC provides system throughput that can be many times higher than that offered by conventional bussed or serial link communications. In addition, the Solano IC's small footprint and low power requirements, together with Texas Instruments' high-performance, low-power, and small-package TMS320C6000™ DSPs, allow for high-density network implementations.

1.1 Basic Architecture

A network of multiple Solano ICs facilitates FIFO communication paths between multiple DSPs (8 FIFOs seen by each processor). At the core of a single Solano IC are four banks of FIFOs, each bank containing a transmit and a receive FIFO. It interfaces to the Host DSP or I/O module on one side, and a set of LVDS links on the other (external link) side. This simple architecture allows the IC to replace bidirectional FIFO communications solutions, while providing greater throughput and flexibility, and reducing board area and power. See Figure 1.



†For a complete list of TMS320C62x™ devices, go to http://www.ti.com.

Figure 1. Implementation of the Solano IC With TMS320C620x (C620x) DSP†

TMS320C6000 and TMS320C62x are trademarks of Texas Instruments.

1.2 Host Interface

The Solano Communications IC is typically connected to the external memory interface (EMIF) of a DSP. Solano's host interface can operate in one of three possible modes: EMIF bus mastering, asynchronous slave, or pipelined synchronous slave.

In the case of a Texas Instruments C620x DSP, the Solano IC's direct EMIF bus mastering capability moves data to and from the DSP's external memory (SDRAM) at up to 600 MBps (32-bit word at 150MHz), with processor overhead limited to setup of Solano's embedded DMA controller. The DMA engine relieves the communications burden placed on an external processor, allowing it to spend more time performing useful work. Arriving data is moved directly from a receive FIFO into external SDRAM memory, ready for the DSP task that requires it. Outgoing data is read directly from external SDRAM memory into a transmit FIFO.

The Solano IC's asynchronous slave interface allows a simple interface to virtually any processor or other device. It is through this interface that the device can access internal control registers and FIFOs.

Alternatively, a pipelined synchronous slave interface is provided which allows for data transfers to or from a device at up to 600 MB/s.

In all three modes of operation, the Solano IC features an advanced embedded interrupt controller that interfaces very efficiently to DSPs.

1.3 High Speed LVDS Link Interface

The Solano IC has four full-duplex LVDS links, each capable of simultaneous transmit and receive speeds up to 213 MB/s, an aggregate bandwidth of over 13.6 Gbps per node. Each full-duplex link has two associated 512 x 32 FIFOs, which provide the communication path to the host interface. These high-speed links can connect to other Solano ICs, I/O modules, or processor nodes that are on or off the carrier board. Note that cable and connector specifications do exist for linking carrier boards together.

1.4 Power/Size Advantage

In addition to its high bandwidth communication paths, the Solano IC features low power and small package size.

The Solano IC is a 16 sq. mm. BGA package with a 0.8 mm ball pitch. This coupled with a glue-less interface to the C620x DSP means very little board area is required for a Solano node. These features make it possible to fit a large Solano data network on a single board. The power consumption of the Solano IC is minimized using specialized design techniques including LVDS link shutdown, clock gating, DMA controller shutdown, and synchronous interface shutdown. For example, if all of the LVDS links are powered down, the standby power is typically 0.3 Watts per device. The typical operating power under maximum throughput conditions is 1.1 Watts per device.

2 Typical Solano/C620x Network Node

A typical Solano network node consists of a C6000™ DSP, the Solano Communications IC, and SDRAM. The remainder of this application note will describe the interface between the C620x processors and the Solano IC, but this does not exclude other C6000 DSPs. The TMS320C67x™ DSPs have a similar interface to the C620x processors with some minor pin-out differences (e.g., EMIF output clock). The TMS320C64x™ DSP has more significant EMIF differences, supporting both a 64-bit and 16-bit EMIF interface. The Solano to C64x™ interface would be application-dependent, and will not be discussed further in this document.

2.1 C620x Node Architecture

The C620x connects through its external memory interface (EMIF) to the Solano Communications IC and SDRAM, as shown in Figure 2.

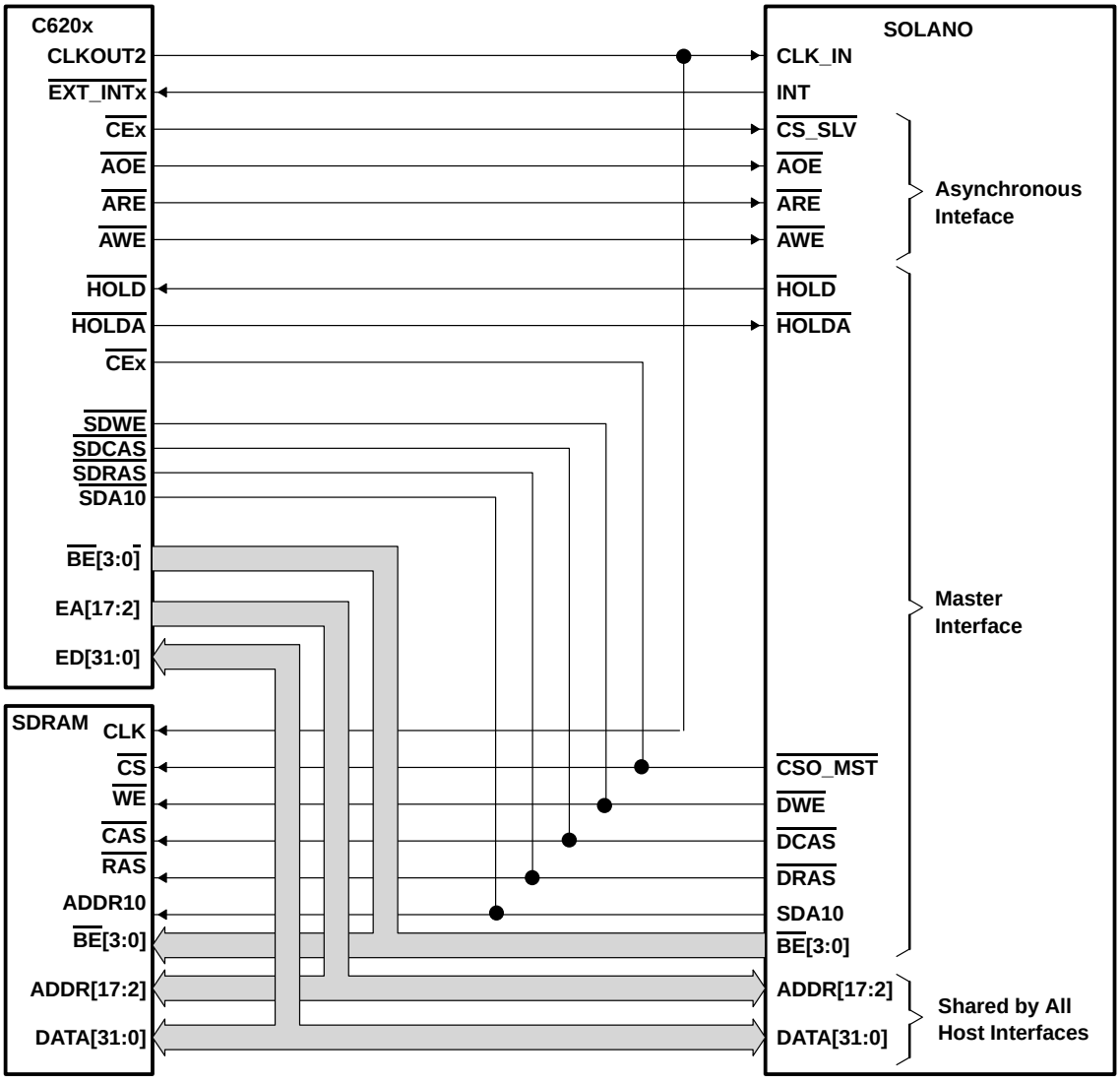


Figure 2. C620x Interface to Solano and SDRAM

C6000, TMS320C67x, TMS320C64x, and C64x are trademarks of Texas Instruments.

The C620x external slave interface is a standard asynchronous slave interface, and the Solano IC will appear to the C620x as an asynchronous RAM. The DSP can access the Solano IC's internal control registers and FIFOs through this interface.

Both the C620x DSP and the Solano IC share the interface to SDRAM. The DSP is the bus arbiter, and grants the Solano IC bus ownership through standard HOLD/HOLDA handshaking.

The Solano IC's host interface and SDRAM are clocked with the CLKOUT2 clock from the C620x DSP, which is half the internal DSP clock speed. The Solano IC must synchronize to this clock in order to perform SDRAM master cycles. This configuration will meet the needs of most applications, but the Solano IC is capable of running off of a separate clock.

This feature, called clock switching, allows the DSP to have a different clock than the Solano IC's host interface. The Solano IC provides clock switching control signals that can be used with minimal glue logic to switch the clock source to SDRAM, depending on whether the DSP or Solano IC is mastering.

A Solano network consists of many such C620x nodes connected together through the Solano LVDS links, as shown in Figure 3. While this application note focuses on the C620x node, such a network could consist of a variety of nodes with different host interfaces, all using the Solano Communications IC as a standard network backbone.

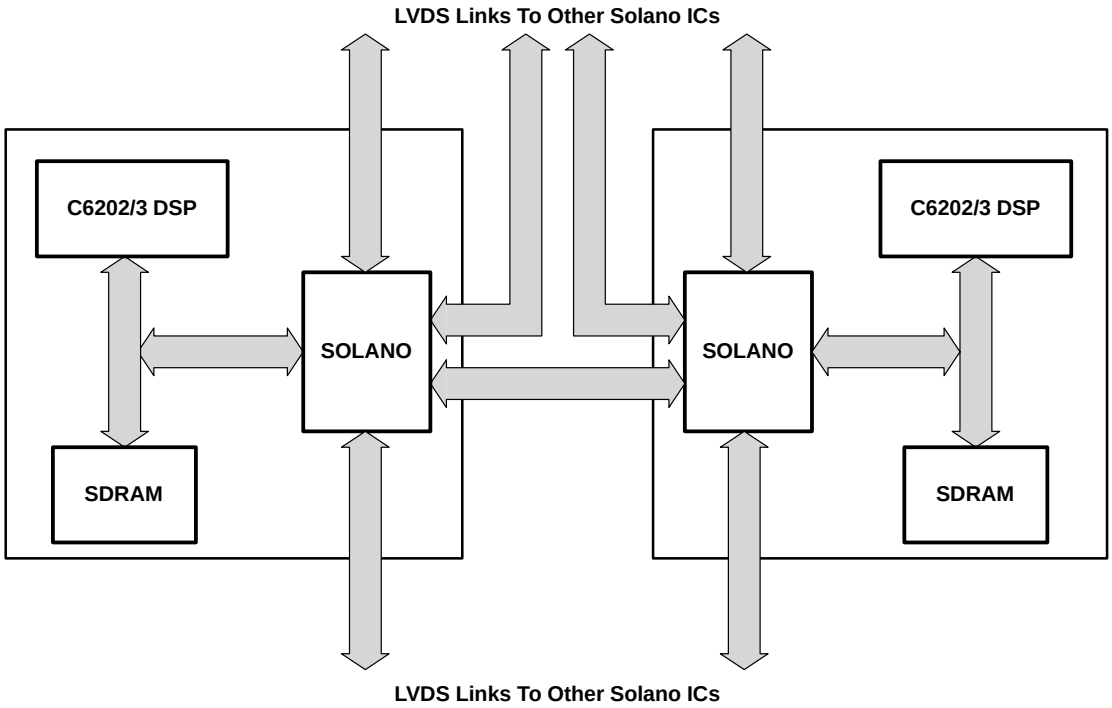


Figure 3. Snapshot of a Typical Solano Network

A good example of Solano network architecture is Spectrum's Mosport-VME board (see Figure 4). Mosport includes eight Solano/C6203 network nodes, each with four LVDS ports linking with other Mosport nodes or external Solano devices through connectors and cables. Each node comprises a C6203, Solano IC, and SDRAM, as shown in Figure 4.

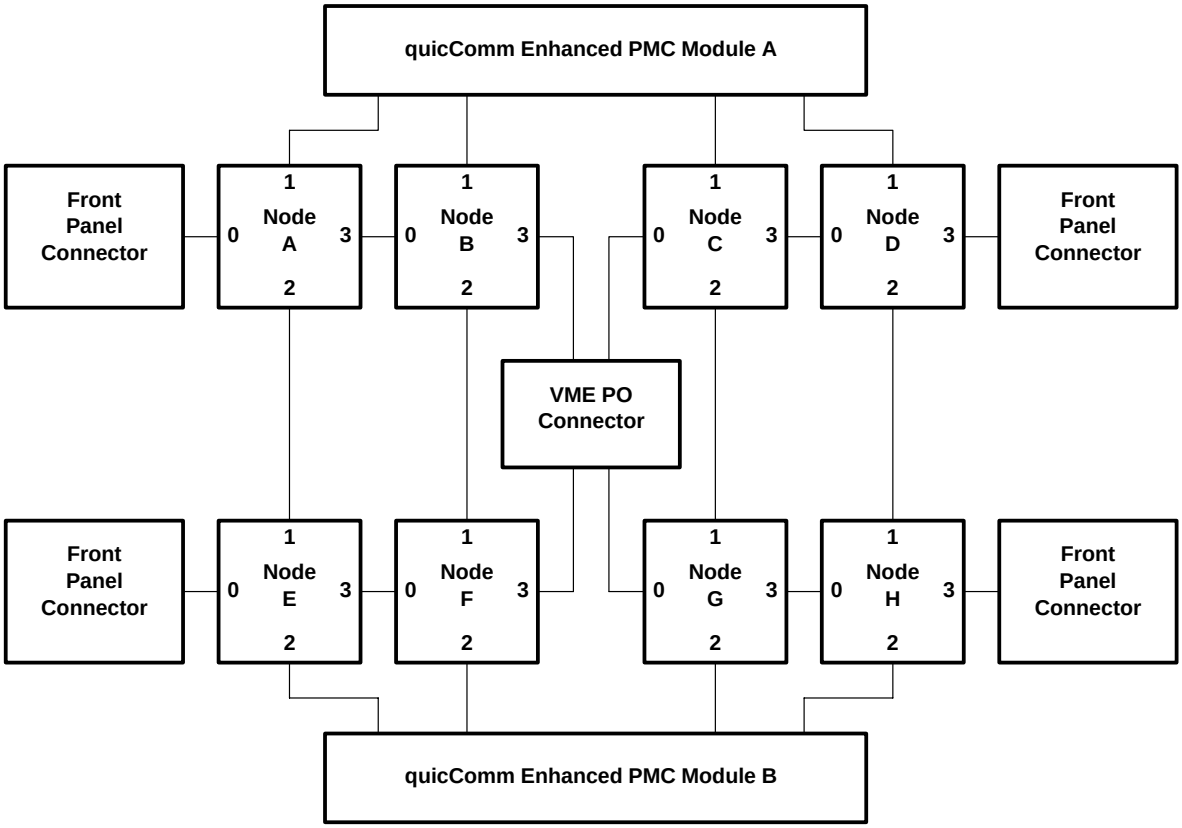


Figure 4. Mosport Solano/C620x Network

2.2 Asynchronous Slave Interface

The C620x DSP must map 0x40000 bytes (256kB) of external asynchronous memory space for the Solano IC. This memory space includes the Solano control registers and FIFO addresses. This glueless interface will appear to the C620x as asynchronous RAM, with an approximate bandwidth of 100 MB/s. Through this interface, the DSP can access both internal control registers and FIFOs. In practice, the DSP accesses the FIFOs using the Solano DMA engine because performance is much better than asynchronous cycles.

2.3 SDRAM Interface

The Solano EMIF bus mastering capability relieves the burden on the DSP with minimal overhead requirements for DMA initialization. To initiate a DMA, the C620x uses the asynchronous interface to set the DMA size, location, and start bit. The DSP can then perform other operations until an interrupt from the Solano IC signals DMA completion.

The Solano IC does not perform any SDRAM refresh operations, but it does ensure that the bus is released frequently enough so that the DSP can refresh SDRAM. Programming the C620x DSP to perform automatic SDRAM refresh cycles is sufficient.

The Solano DMA controller is capable of handling up to eight independent DMA channels, one for each FIFO (transmit and receive). The controller will schedule between DMA channels based on a round-robin scheme and channel priority settings.

Finally, the Solano IC does support several types of SDRAM by allowing standard SDRAM parameters such as the CAS latency, column address bits, and other timing parameters to be customized through internal control registers.

2.4 Interrupts

The most efficient method of retrieving status information from the Solano IC is through its interrupt controller. The Solano IC's single interrupt signal (edge triggered) can be connected to any one of the external interrupt input pins on the DSP. The DSP interrupt service routine must then query the Solano IC to determine the exact source of the interrupt.

An interrupt from the Solano IC could be the result of several standard FIFO status conditions, DMA completion, an LVDS loss of synchronization condition, an end of transfer indicator, or a signal change on one of the Solano IC's general purpose I/O pins. Each of these potential interrupt sources can be individually masked/unmasked and acknowledged through the internal control registers.

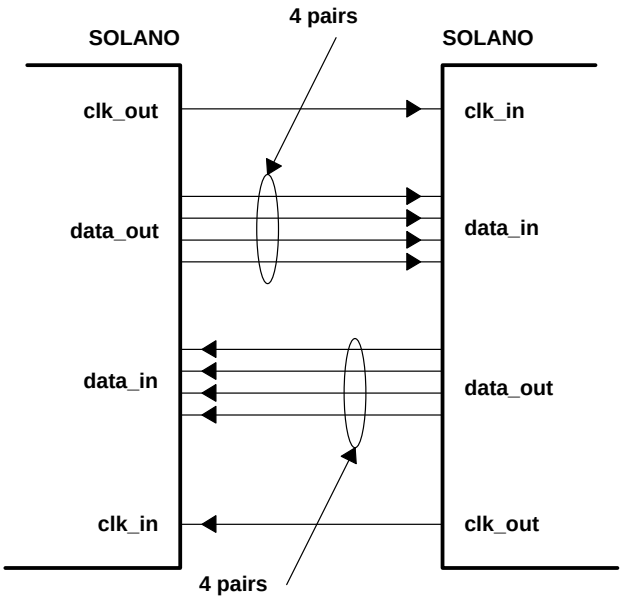
The interrupt controller also allows interrupt priorities to be assigned to internal functional blocks, which allows for high priority interrupt sources to signal interrupts immediately without having to wait until the Solano IC releases the EMIF. It is also possible to configure the Solano IC so that following an interrupt and bus release, it will not reacquire the bus until the interrupt is acknowledged.

2.5 LVDS Routing and Bandwidth

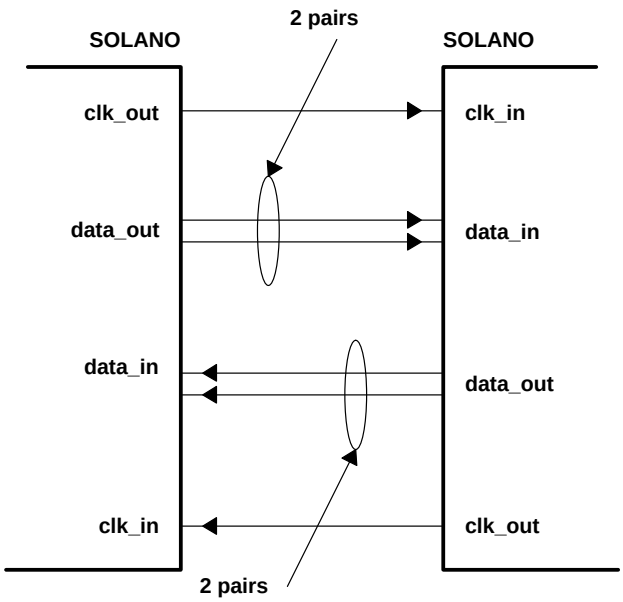
The Solano IC's LVDS interface is designed for complex network designs that may require a mixture of low and high bandwidth links.

The clock speed of an LVDS link is determined by the transmitter side of a connection. This means that one Solano IC could be running at a different link speed than the Solano nodes it is connected to.

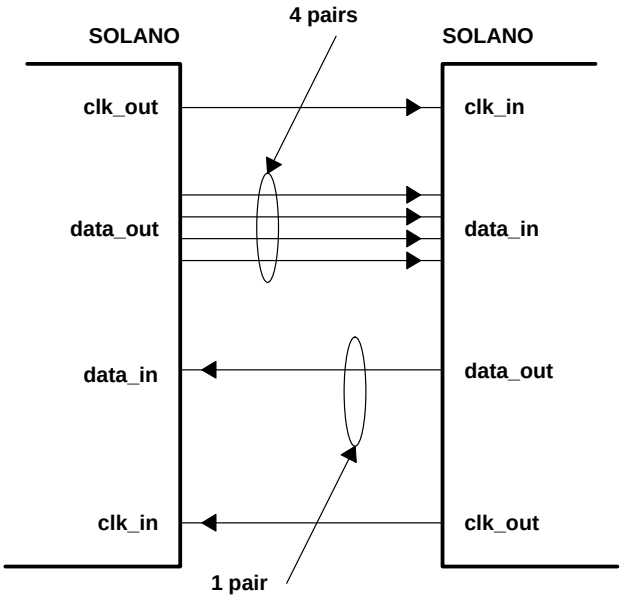
The bandwidth requirements of each Solano network will determine both the clock speed of each Solano IC, as well as the number of LVDS pair connections for each link. Each direction in a link consists of four data pairs that can each be enabled or disabled individually. This flexibility allows for a mixture of low and high bandwidth links in a network, minimized layout issues, and power savings. Figure 5 illustrates several possible link scenarios, which could all exist in a single Solano network.



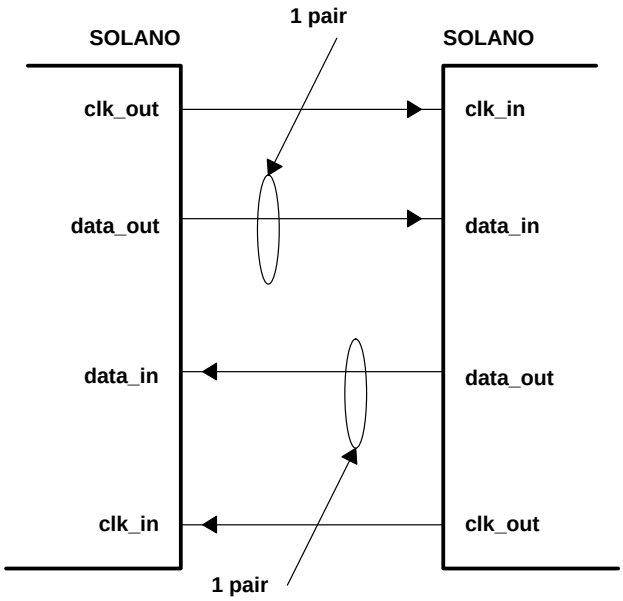
– Maximum bidirectional bandwidth
– Large number of connections



– Medium bidirectional bandwidth
– Modest number of connections



– Maximum unidirectional bandwidth, low reverse channel bandwidth
– Modest number of connections



– Minimum bidirectional bandwidth
– Minimum number of connections

Figure 5. Solano LVDS Link Examples

3 Conclusion

The Solano Communications IC provides a flexible high bandwidth network fabric for TI C6000 based communications infrastructure. The Solano IC was designed with the C620x processor family as the primary target for a host processor. An excellent example of a multiple processor Solano environment is Spectrum's Mosport-VME board, which features eight C6203 DSP processors and ten Solano Communications ICs.

For further information on the Solano Communications IC, visit Spectrum's website at

http://www.spectrumsignal.com/Wireless_Systems/01_Products/04_ASICs/

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