# Connecting TFT LCD Displays to the OMAP5910

*Gerald Coley* *DSPIEEE Catalog OMAP Applications*

**ABSTRACT**

The OMAP5910 contains an integrated LCD controller. Utilizing internal memory and dedicated DMA channels, this architecture contains a very efficient LCD control interface. This appnote describes how to connect two different LCD displays to the OMAP5910. While there are many sizes and types of LCD displays in the industry, this appnote focuses on two 240 × 320 color thin film transistor (TFT) displays and how they interface to the OMAP5910 processor.

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# 1 OMAP5910 LCD Controller

This section provides a high-level description of the LCD controller as it pertains to the TFT mode of operation that is being used in this appnote.

## 1.1 Features

The following features are provided by the OMAP5910 LCD controller:

- Mono passive: 1 BPP, 2 BPP, 4 BPP, and 8 BPP
  - 1 BPP: Two palette entries selecting one of 15 grayscale
  - 2 BPP: Four palette entries selecting one of 15 grayscale
  - 4 BPP: 16 palette entries selecting one of 15 grayscale
  - 8 BPP: 256 palette entries selecting one of 15 grayscale
- Color passive: 2 BPP, 4 BPP, 8 BPP, 12, and 16 BPP
  - 2 BPP: Four palette entries from 3375 possible colors
  - 4 BPP: 16 palette entries from 3375 possible colors
  - 8 BPP: 256 palette entries from 3375 possible colors
  - 12 BPP: 3375 possible on-screen colors
  - 16 BPP: 3375 possible on-screen colors
- Active: 2 BPP, 4BPP, 8BPP, 12 BPP, and 16BPP

- 2 BPP: Four palette entries selecting from 4096 colors
- 4 BPP: 16 palette entries selecting from 4096 colors
- 8 BPP: 256 palette entries selecting from 4096 colors
- 12 BPP: Maximum 64K colors
- 16 BPP: Maximum 64K colors, depending on LCD panel

The TFT is the most commonly used display for hand-held type devices and offers the best overall quality in terms of color depth, clarity, and overall brightness.

The other modes listed above are not covered in this application note.

## 1.2 Block Diagram

Figure 1 shows the block diagram of the LCD controller on the OMAP5910.

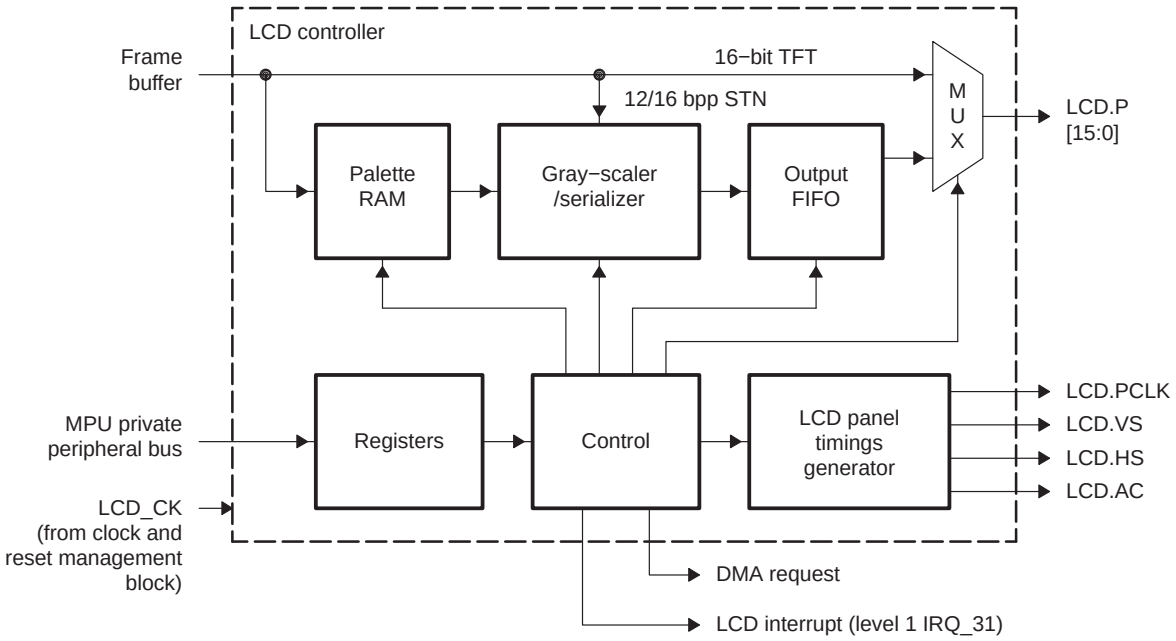



**Figure 1. OMAP5910 LCD Control Block Diagram**

In the TFT mode, the palette RAM, gray-scalar, and output FIFO are not used. The data is sent directly to the LCD display via the DMA controller from the internal frame buffer memory.

For more detailed information on the internal workings of the OMAP5910 LCD controller, refer to the OMAP5910 datasheet or Technical Reference Manual.

### 1.3 LCD Interface Signals

Table 1 defines the primary pins used by the OMAP5910 to control an external TFT LCD panel.

**Table 1. LCD Interface Signals**

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| LCD.P[15:0] | OUT | Pins used to transfer sixteen bit data values at a time to the LCD display. |
| LCD.PCLK | OUT | Pixel clock used by the LCD display to clock the pixel data into the line shift register. The pixel clock transitions continuously and the ac-bias pin is used as an output enable to signal when data is available on the LCD pins. |
| LCD.HS | OUT | Line clock used by the TFT displays as the horizontal synchronization signal. |
| LCD.VS | OUT | Frame clock used by the LCD displays to signal the start of a new frame of pixels. Used by TFT displays as the vertical synchronization signal. |
| LCD.AC | OUT | Used in TFT mode as the output enable to signal when data is latched from the data pins using the pixel clock. |

Additional signals may be required from the OMAP5910. These signals are typically GPIO pins and are used to control such things as:

- LCD power on/off
- Backlight on/off
- Brightness control

Depending on the system level design, several pins are available for these and similar functions. The designer of the board is free to choose if and how these functions are controlled by the OMAP5910 processor.

## 2 NEC 240 × 320 QVGA Display

The first display that we will discuss is the NEC NL2432DR22-11B LCD display. The features of this display include:

- 3.5” (8.9cm) diagonal
- 240 x 320 Resolution (QVGA)
- Reflective
- Portrait Mode

The remainder of this section describes how to interconnect the NEC LCD display and the OMAP5910.

## 2.1 Display Description

The NEC display is actually comprised of two components:

- NL2432DR22-11B LCD display
- The S1L50282F23k100 timing controller

### *2.1.1 LCD Display*

Table 2 lists the specifications of the NEC LCD.

**Table 2. NEC LCD Specifications**

| Parameter | Specification | Units |
|---|---|---|
| Screen Diagonal | 3.52”(8.9) | in(cm) |
| Display Area | 2.11(53.64)H × 2.82 (71.53)V | in(mm) |
| Pixel Format | 240 × 320 | |
| Colors | 262,144 | |
| Pixel Configuration | R,G,B Vertical Stripe | |
| Outline Dimensions | 2.56(65)W × 3.35(85)H × 18(4.5)D | in(mm) |

### *2.1.2 Timing Controller*

The OMAP5910 actually connects to the S1L50282F23k100 timing controller provided by NEC. The timing controller converts the 16-bit LCD data into the row and column scan data to drive the LCD panel itself. In some cases, the timing controller is integrated with the LCD panel. This is especially true of the larger size displays. However, in this case, the timing controller is separate from the LCD panel. Figure 2 shows the pinout of the timing controller.

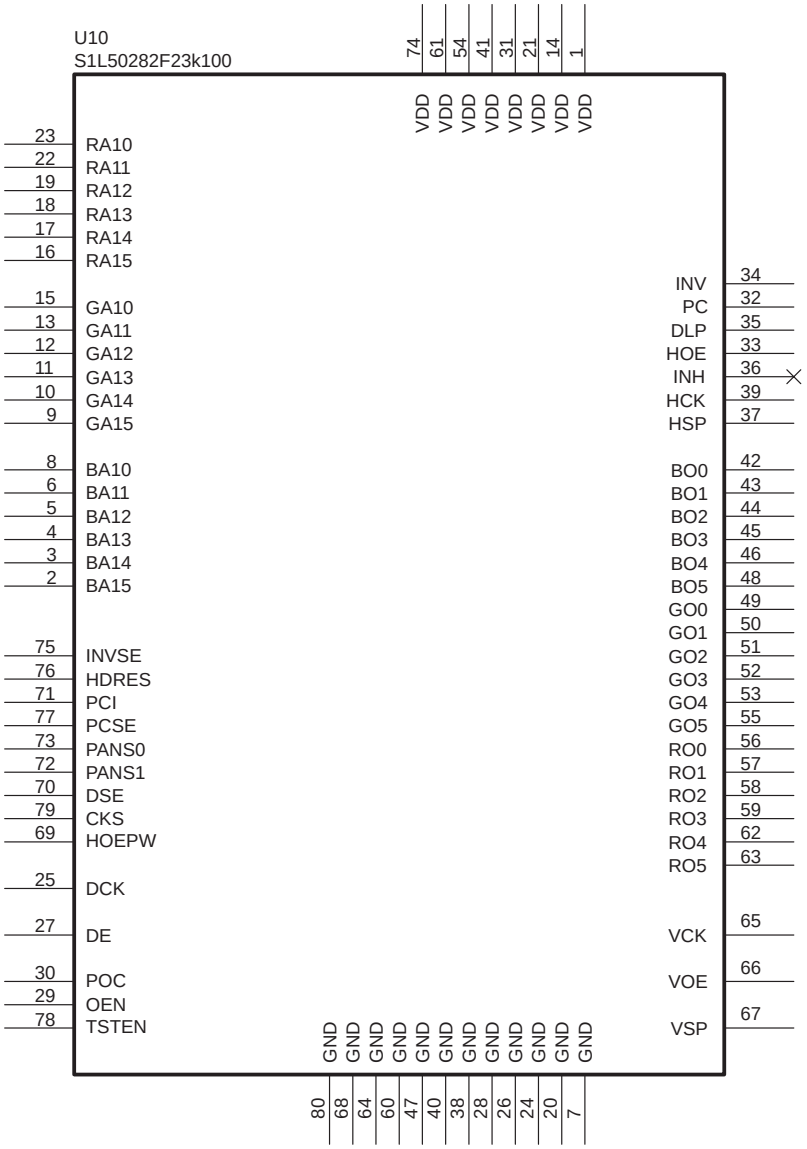



**Figure 2. NEC LCD Timing Controller**

The individual signals are discussed in the following sections.

## 2.2 LCD Control Signals

Table 3 describes the functions of the control signals on the S1L50282F23k100 timing controller that connects to the OMAP5910 LCD interface. The LCD side of the controller is not covered. Refer to the schematic in Appendix A for more details.

**Table 3. LCD Control Signals**

| Number | Name | I/O | Freq | Description |
|---|---|---|---|---|
| 6,8,5−2 | BI0-5 | I | 7.5 MHZ | Input data for the color blue. |
| 15,13−9 | GI0-5 | I | 7.5 MHZ | Input data for the color green. |
| 23,22,19−16 | RI0-5 | I | 7.5 MHZ | Input data for the color red. |
| 25 | DCK | I | 15 MHZ | Dot clock |
| 27 | DE | I | 18.75 KHZ | Data enable |
| 29 | OEN | I | DC | Gate driver output enable pin |
| 30 | POC | I | DC | Power on clear |
| 75 | INVSE | I | DC | Output data reverse (0:off,1:on) |
| 76 | HDRES | | DC | Data reverse of Internal PC (0:off,1:on) |
| 71 | PCI | I | DC | Polarity inversion (0:line reverse,1:frame reverse) |
| 77 | PCSE | I | DC | PC switching (0:internal PC,1:Internal PC reverse) |
| 73 | PANS0 | I | DC | Switching resolution setup 0 |
| 72 | PANS1 | I | DC | Switching resolution setup 1 |
| 70 | DSE | I | DC | Source driver switching |
| 79 | CKS | I | DC | DCK reverse (0:no-reverse, 1:reversed) |
| 69 | HOEPW | I | DC | HOE Pulse width selection. |
| 78 | TSTEN | I | DC | Test terminal (0:non-reversed’1=reversed. |

NOTE: Not all of these signals are controlled by the OMAP5910 processor.

## 2.3 OMAP5910 Interface

This section describes the interconnection of the LCD and timing controller into the OMAP5910 processor. Table 4 maps the LCD controller pins to the OMAP595910. In addition, those signals that do not connect to the OMAP5910, but need to be terminated, are also covered.

**Table 4. LCD Control Signals Connections**

| CONTROLLER SIGNAL | OMAP5910 SIGNAL | CONTROLLER SIGNAL | OMAP5910 SIGNAL |
|---|---|---|---|
| BI0 | LCD.P4 | DCK | LCD.PCLK |
| BI1 | LCD.P0 | DE | LCD.AC |
| BI2 | LCD.P1 | OEN | HIGH |
| BI3 | LCD.P2 | POC | HIGH via RC |
| BI4 | LCD.P3 | INVSE | Ground |
| BI5 | LCD.P4 | HDRES | Open |

**Table 4. LCD Control Signals Connections (Continued)**

| CONTROLLER SIGNAL | OMAP5910 SIGNAL | CONTROLLER SIGNAL | OMAP5910 SIGNAL |
|---|---|---|---|
| GI0 | LCD.P5 | PCI | Ground |
| GI1 | LCD.P6 | PCSE | Open |
| GI2 | LCD.P7 | PANS0 | High |
| GI3 | LCD.P8 | PANS1 | High |
| GI4 | LCD.P9 | DSE | Ground |
| GI5 | LCD.P10 | CKS | Open |
| RI0 | LCD.P15 | HOEPW | Ground |
| RI1 | LCD.P11 | TSTEN | Ground |
| RI2 | LCD.P10 | | |
| RI3 | LCD.P9 | | |
| RI4 | LCD.P8 | | |
| RI5 | LCD.P7 | | |

If you will note, BI0 and BI5 are connected to the same signal from the OMAP processor. This is because the timing controller is designed for 18-bit data, or R6:G6:B6, whereas OMAP5910 supports 16-bit data, or R5:G6:B5. Tying these two signals together, BI0, being the least significant bit, is an easy way of performing the conversion not only for the red component, but for the blue component as well. Green on the other hand, uses all available bits which results in a 5:6:5 configuration for the data.

What is unique about the NEC timing controller is that it does not require the vertical or horizontal sync data; only the pixel clock and the DE signal.

Refer to Appendix A for the complete schematic.

### *2.3.1 LCD Power*

Figure 3 illustratess the design of the LCD power for the NEC display. The power does not necessarily need to be designed in this manner, only the required power must be provided.

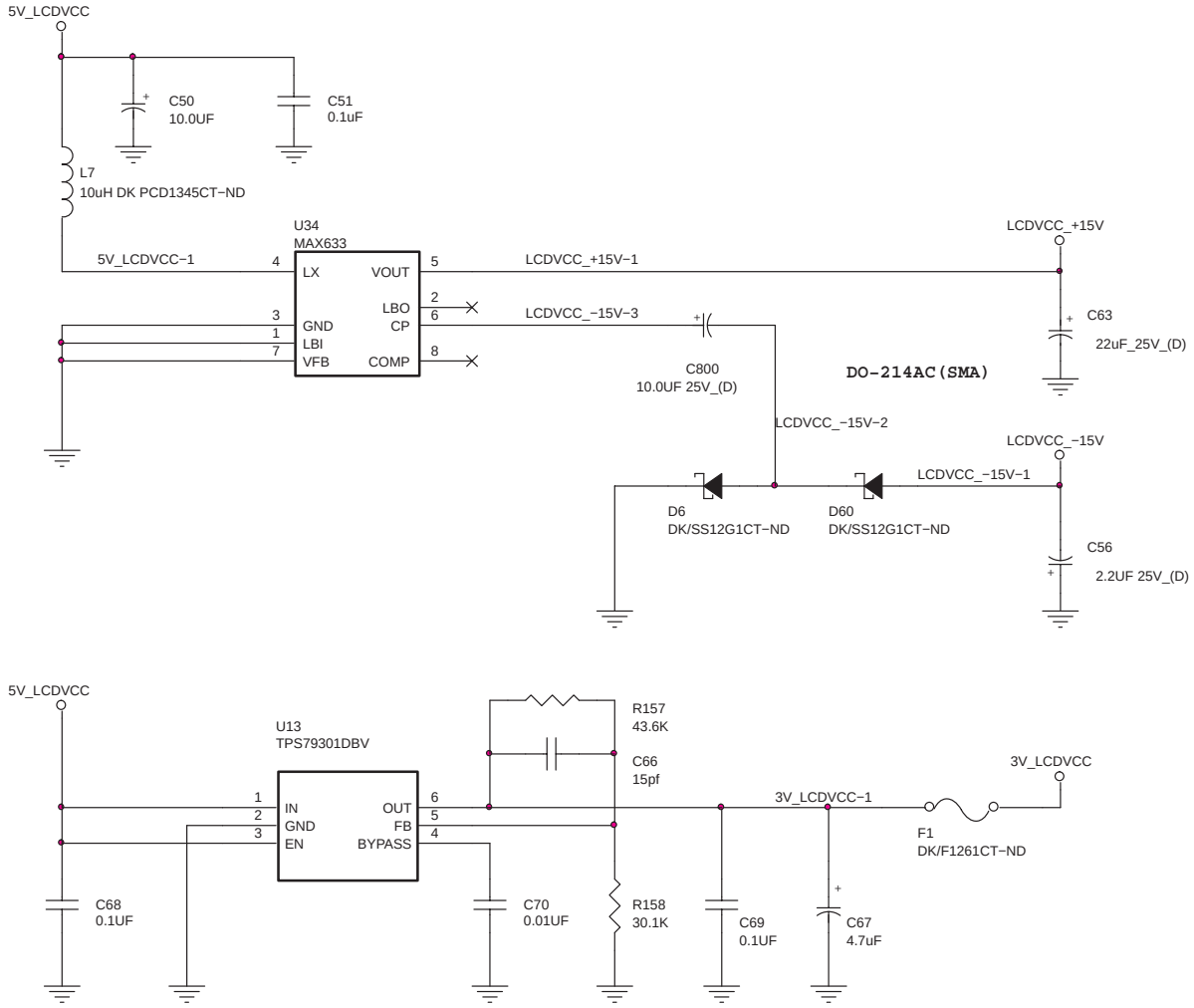



**Figure 3. NEC LCD Power**

The NEC display requires a + 15 V and a −15 V supply to power the LCD panel. The logic signals in the LCD panel are all at 3 VDC. In this design, all of the power is generated based on a 5 VDC supply. In the event the supply is different, Up converters can be used to create the required voltages.

Pin 2 on the LCD connector (refer to Appendix A) is the contrast control for the LCD panel. A potentiometer is used to adjust the voltage based on a 5v voltage source as needed.

### *2.3.2 Touchscreen*

In addition to the LCD panel, the NEC display also has an integrated touch panel over the display. This touch panel provides the ability to connect to a 4-wire touchscreen controller in order to decode the x and Y coordinates and pressure on the display where a stylus is being used. Any 4-wire touchscreen controller decodes this information. A good device is the TI ADS7486 as depicted in Figure 4.

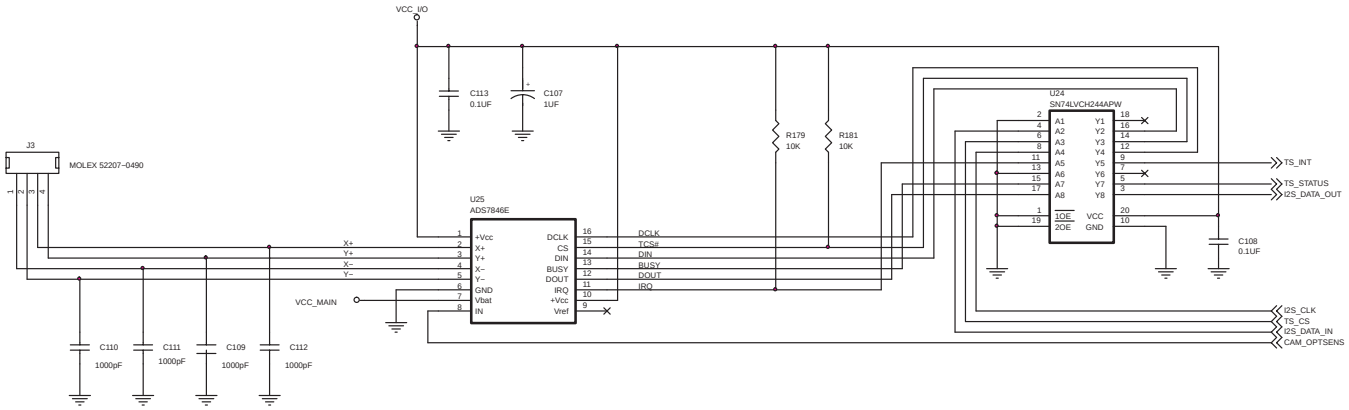



**Figure 4. NEC LCD Power**

### *2.3.3 LCD Panel Front Light*

The NEC display has an LED light source configured as a frontlight and integrated into the NEC panel. Figure 4 shows the frontlight power configuration. The LEDs require 7.9 V. In this case, however, a 15 V supply was used because it already existed for the LCD panel. The designer may choose to generate the required power differently.

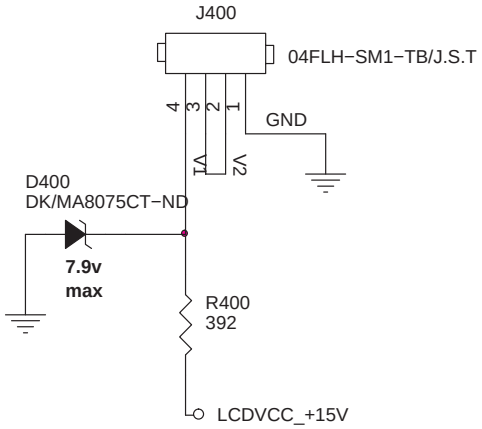



**Figure 5. NEC LCD LED Frontlight Power**

# 3 Sharp 240 × 320 Display

This section describes connecting a Sharp LQ035Q7D color TFT display to the OMAP5910. The schematic for this implementation can be found in Appendix B.

## 3.1 Display Description

The LQ035Q7D LCD display is a color reflective module based on TFT technology. It has an LCD panel, Driver ICs, back light, touch panel, and a back sealed casing.

The specifications of this display are included Table 5.

**Table 5. LCD Control Signals Connections**

| Parameter | Specification | Units |
|---|---|---|
| Screen diagonal | 3.52”(8.9) | in(cm) |
| Display area | 2.11(53.64)H × 2.82 (71.53) V | in(mm) |
| Pixel format | 240 × 320 | |
| Colors | 262,144 | |
| Pixel configuration | R,G,B Vertical stripe | |
| Outline dimensions | 2.56(65)W × 3.35(85)H ×.18(4.5)D | in(mm) |

### *3.1.1 Timing Controller*

The Sharp LCD also has a separate timing controller chip called the LZ9FC22. This chip converts the 16bi RGB digital data into the row and column driver information to drive the LCD panel. Figure 6 contains the pinout of the LCD timing controller.

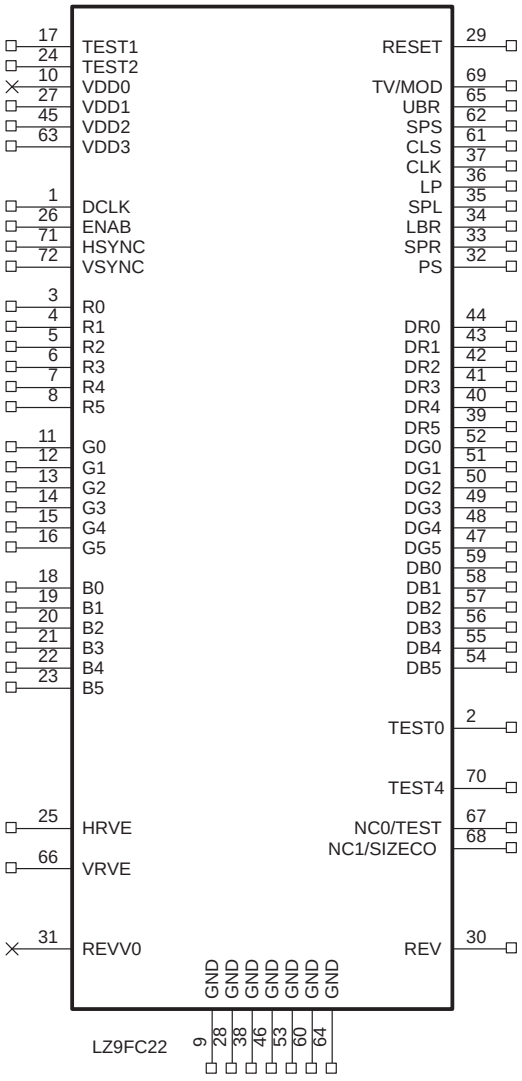



**Figure 6. Sharp LCD Timing Controller**

## 3.2 Control Signals

Table 6 defines the signals on the LCD timing controller that are used to connect to the OMAP5910 processor.

**Table 6. Sharp LCD Control Signals**

| No. | Name | I/O | Description |
|---|---|---|---|
| 1 | DCLK | I | Input terminal for data clock signal |
| 2 | SETR | I | Input terminal for control signal for PS (SIZEC0 = ”L” to the application) |
| 3−8 | R0-5 | I | Input data for the color red |
| 11−16 | G0-5 | I | Input data for the color green |
| 18−23 | B0-5 | I | Input data for the color blue |

**Table 6. Sharp LCD Control Signals (Continued)**

| No. | Name | I/O | Description |
|---|---|---|---|
| 25 | HREV | I | Input terminal for setting up right/left reverse scanning<br>H level : Normal L level : Reverse scanning |
| 26 | ENAB | I | Input terminal for signal to settle the horizontal display position |
| 66 | VREV | I | Input terminal for setting up up/down reverse scannning<br>(H:Normal L:Reverse scanning) |
| 68 | SIZECO | I | Input signal for drive condition change<br>SIZEC0 =<br>H : Portrait QVGA(240RGB × 320)<br>L : Landscape QVGA(320RGB × 240) |
| 70 | REM | I | Input terminal for reset signal |
| 71 | HS | I | Input terminal for horizontal sync. signal |
| 72 | VS | I | Input terminal for vertical sync. Signal |

## 3.3 OMAP5910 Interface

Table 7 defines the mapping between the Sharp LCD timing controller chip and the OMAP5910 processor LCD interface. It also shows the state of the pins that are not controlled directly by the OMAP5910 processor.

**Table 7. Sharp LCD OMA5910 Interface**

| CONTROLLER SIGNAL | OMAP5910 SIGNAL | CONTROLLER SIGNAL | OMAP5910 SIGNAL |
|---|---|---|---|
| B0 | LCD.P4 | DCK | LCD.PCLK |
| B1 | LCD.P0 | DE | LCD.AC |
| B2 | LCD.P1 | OEN | HIGH |
| B3 | LCD.P2 | POC | HIGH via RC |
| B4 | LCD.P3 | INVSE | Ground |
| B5 | LCD.P4 | HDRES | Open |
| G0 | LCD.P5 | PCI | Ground |
| G1 | LCD.P6 | PCSE | Open |
| G2 | LCD.P7 | PANS0 | High |
| G3 | LCD.P8 | PANS1 | High |
| G4 | LCD.P9 | DSE | Ground |
| G5 | LCD.P10 | CKS | Open |
| R0 | LCD.P15 | HOEPW | Ground |

**Table 7. Sharp LCD OMA5910 Interface (Continued)**

| CONTROLLER SIGNAL | OMAP5910 SIGNAL | CONTROLLER SIGNAL | OMAP5910 SIGNAL |
|---|---|---|---|
| R1 | LCD.P11 | TSTEN | Ground |
| R2 | LCD.P12 | | |
| R3 | LCD.P13 | | |
| R4 | LCD.P14 | | |
| R5 | LCD.P15 | | |

## 3.4 LCD Panel Power

Figure 7 shows a possible design for the LCD power. The LCD requires a +15 V supply for the LCD panel itself. The logic section of the LCD requires a 3.3 V supply. The designer may choose a different way to supply the power to the LCD.

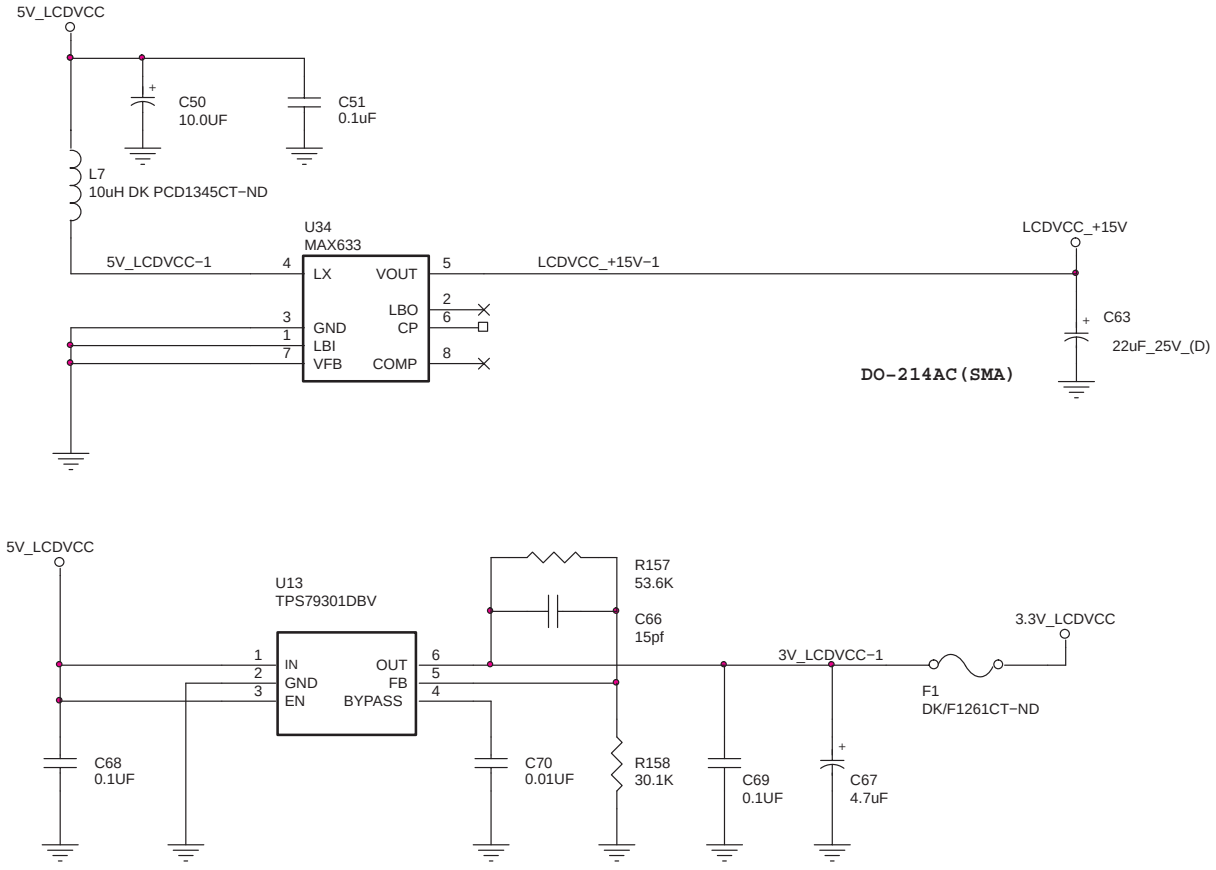



**Figure 7. Sharp Power Supply**

Both of these circuits use a 5 V source to create the required voltages. The fuse is not required and is  a part of this design, only as a precautionary measure.

## 3.5 LED Frontlight Interface

Figure 8 is the schematic for the control interface for the LED frontlight of the Sharp display.

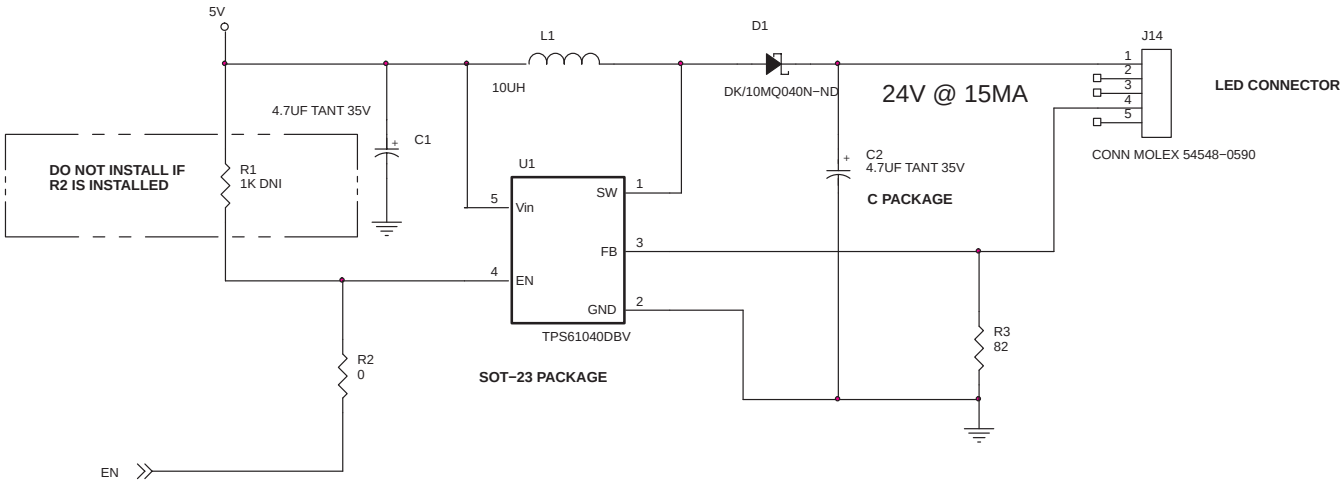



**Figure 8. Sharp LCD Frontlight Controller**

The power for the LED is supplied by U1, a 400-ma boost converter, which converts the 5 V input to the 24 V required by the LEDs. This design actually accepts and inputs a voltage range from 1.8 V to 6 V. So, depending on the individual designs, there is some flexibility here. Refer to the TPS61040 datasheet for more details.

The EN signal can be any GPIO pin on the OMAP5910. When it is Hi, U1 is active. As an option, R1 can be installed if the user wants the LCD to be on all the time.

## 3.6 Touchscreen

The requirements for the Touchscreen panel on the Sharp LCD are the same as found on the NEC Touchscreen interface.

# 4 Summary

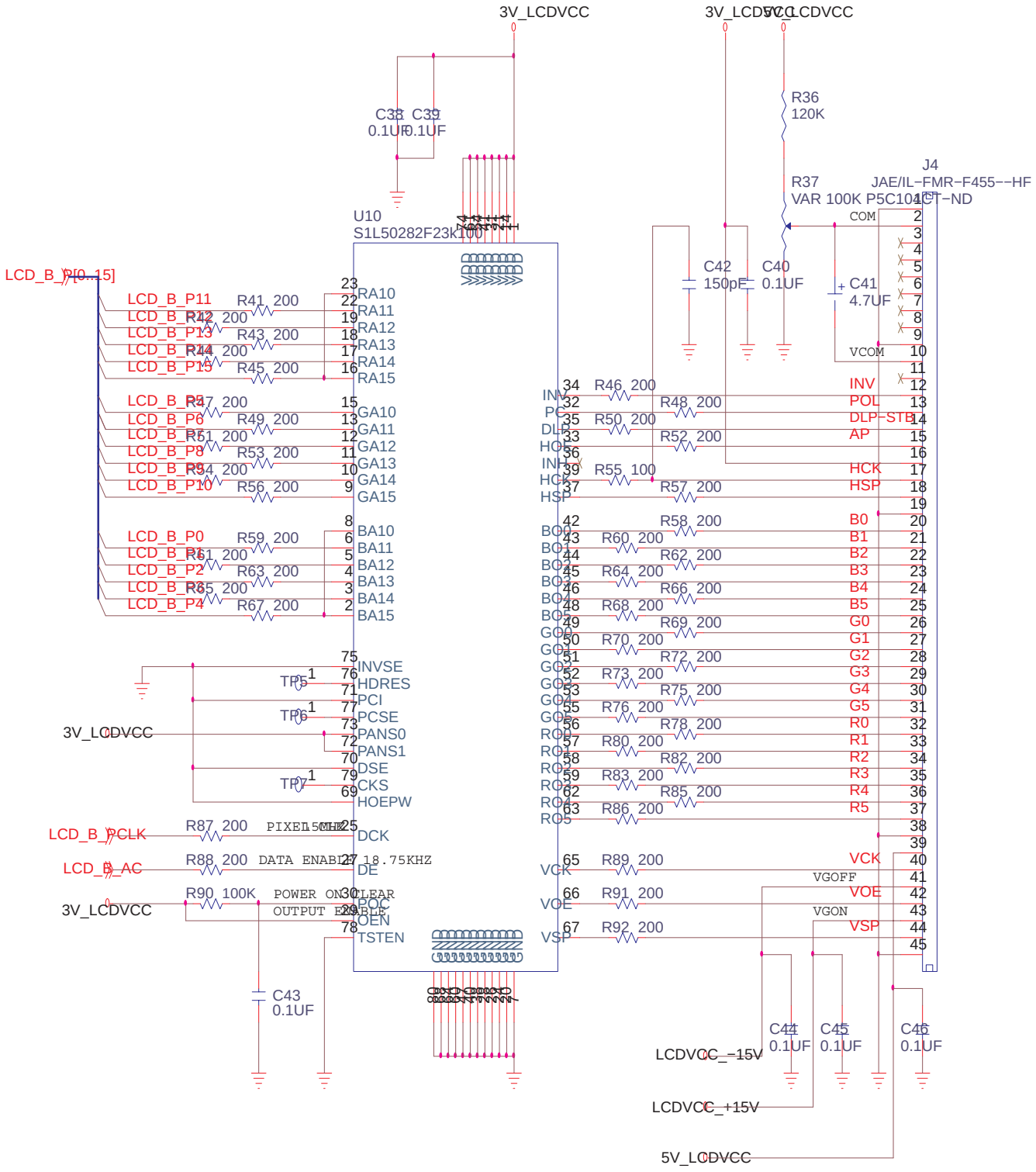
The NEC LCD design was verified and produced in the form of the Innovator Development Kit. The NEC design was used in the production units of the Innovator platform and is still being used.

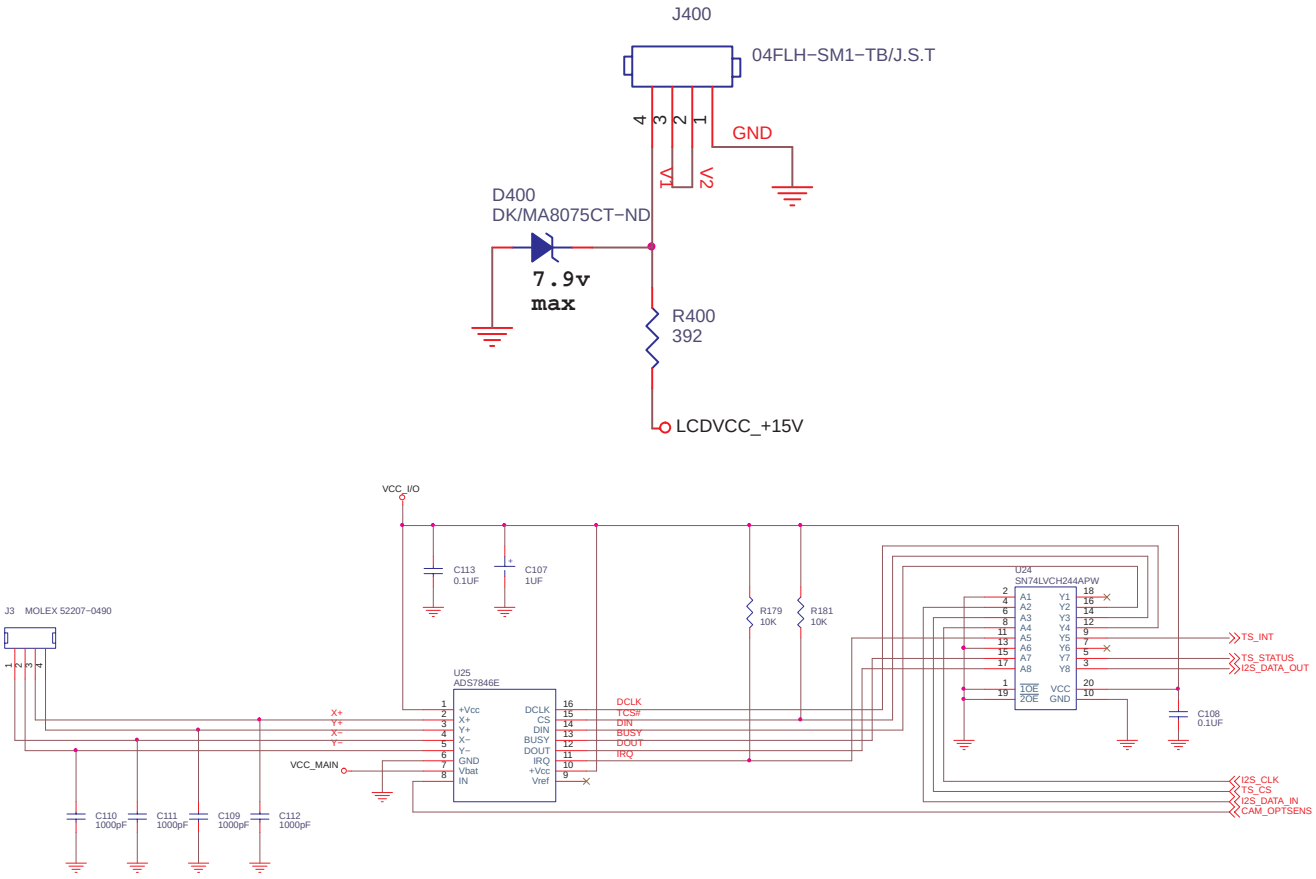
A printed circuit board design was made, and 10 units were assembled and tested for the Sharp design. It was never produced in large quantities. It was intended as a backup in case the NEC displays could not be obtained.

# 5 References


1. *OMAP1510 Dual-Core Processor Data Manual* (literature number SPRS197)
2. *OMAP1510 Dual-Core Processor Technical Reference Manual* (literature number SPRU602)
3. Sharp LCD Panel Datasheet LQ035Q7 B02 (LCY-02024, March 14, 2002)
4. NEC LCD Panel Datasheet NL2432DR22-11B (8th Edition, March 4, 2002)
5. Sharp Control IC for TFT-LCD Module LZ9FC22 (LCY-00136, June 26, 2001)
6. NEC LCD Controller S1L50282F23k100 (DOD-N-0192, 3rd Edition)

# Appendix A NEC Display Schematics

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04FLH−SM1−TB/J.S.T
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3
2
1
GND
V1
V2
D400
DK/MA8075CT−ND
7.9v
max
R400
392
LCDVCC_+15V
VCC_I/O
C113
0.1UF
C107
1UF
R179
10K
R181
10K
U24
SN74LVCH244APW
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TS_STATUS
I2S_DATA_OUT
C108
0.1UF
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TCS#
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BUSY
DOUT
IRQ
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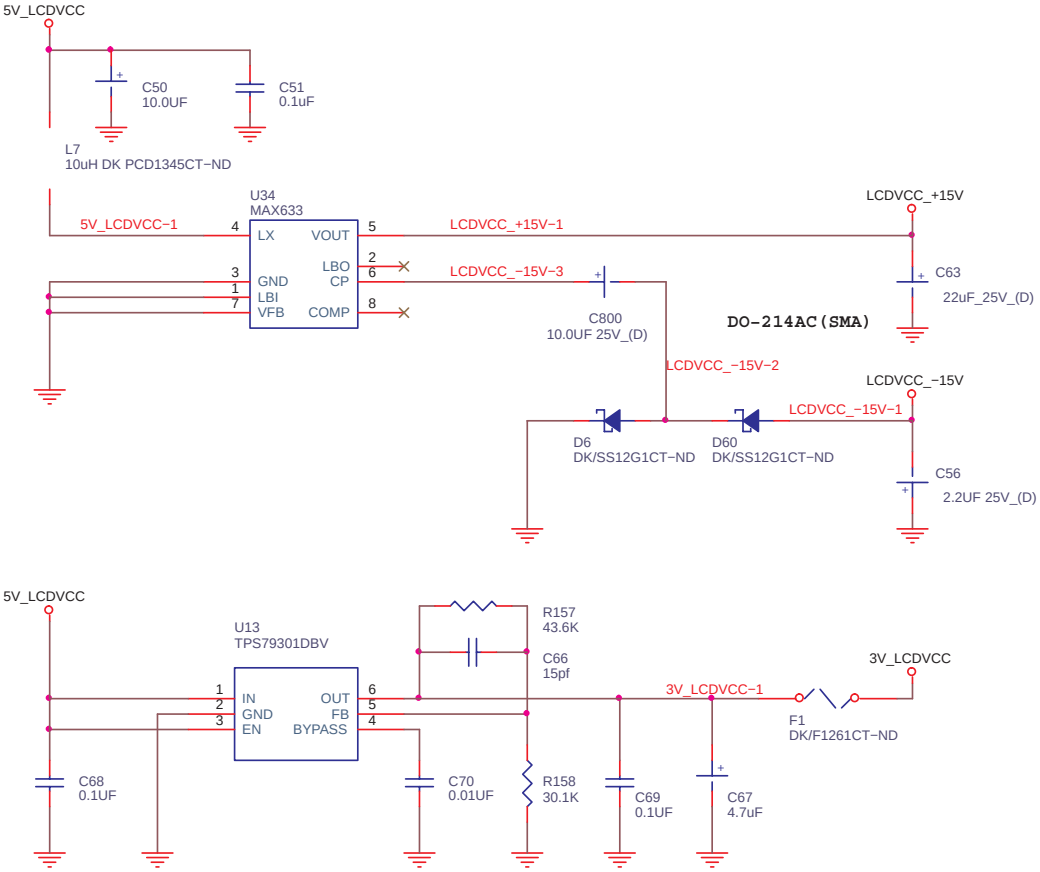
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10.0UF
C51
0.1uF
L7
10uH DK PCD1345CT−ND
U34
MAX633
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LX
VOUT
LCDVCC_+15V−1
LBO
CP
LCDVCC_−15V−3
GND
LBI
VFB
COMP
C800
10.0UF 25V_(D)
DO−214AC(SMA)
LCDVCC_+15V
C63
22uF_25V_(D)
LCDVCC_−15V−2
LCDVCC_−15V
LCDVCC_−15V−1
D6
DK/SS12G1CT−ND
D60
DK/SS12G1CT−ND
C56
2.2UF 25V_(D)
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U13
TPS79301DBV
R157
43.6K
C66
15pf
3V_LCDVCC
3V_LCDVCC−1
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GND
EN
OUT
FB
BYPASS
F1
DK/F1261CT−ND
C68
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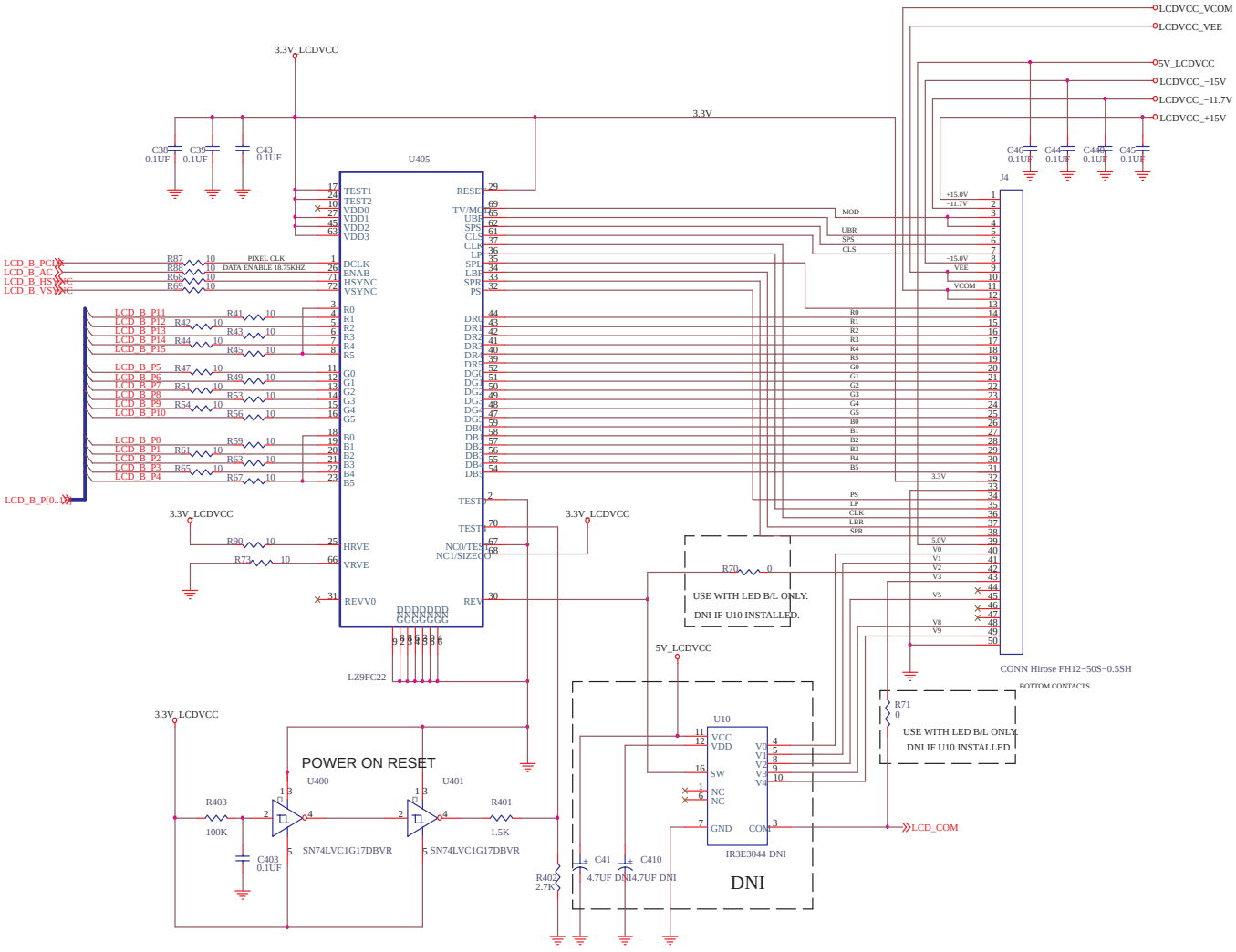
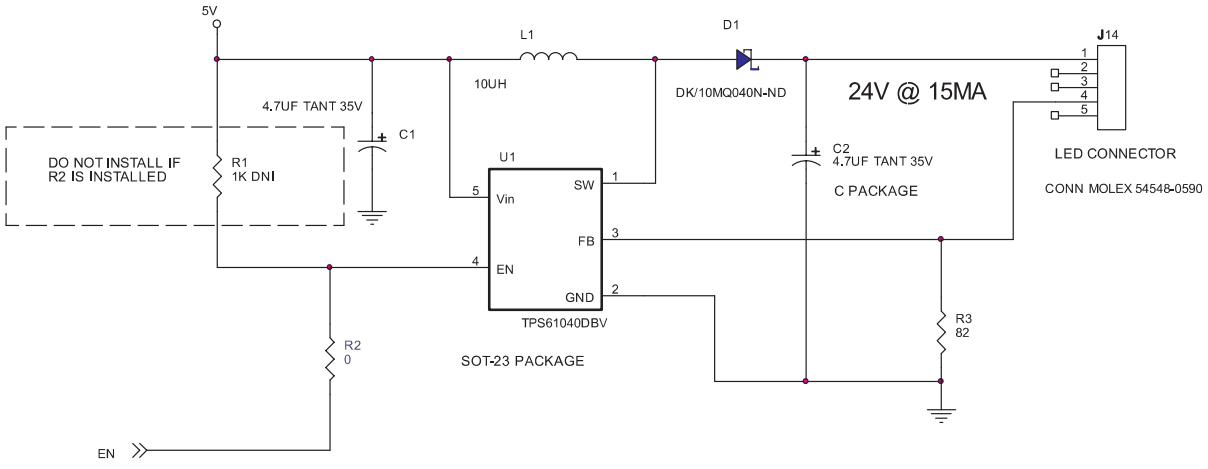
0.01UF
R158
30.1K
C69
0.1UF
C67
4.7uF

# Appendix B Sharp Display Schematics

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L1
10UH
D1
DK/10MQ040N-ND
24V @ 15MA
J14
1
2
3
4
5
LED CONNECTOR
CONN MOLEX 54548-0590
4.7UF TANT 35V
C1
DO NOT INSTALL IF
R2 IS INSTALLED
R1
1K DNI
U1
5
Vin
SW
1
FB
3
4
EN
GND
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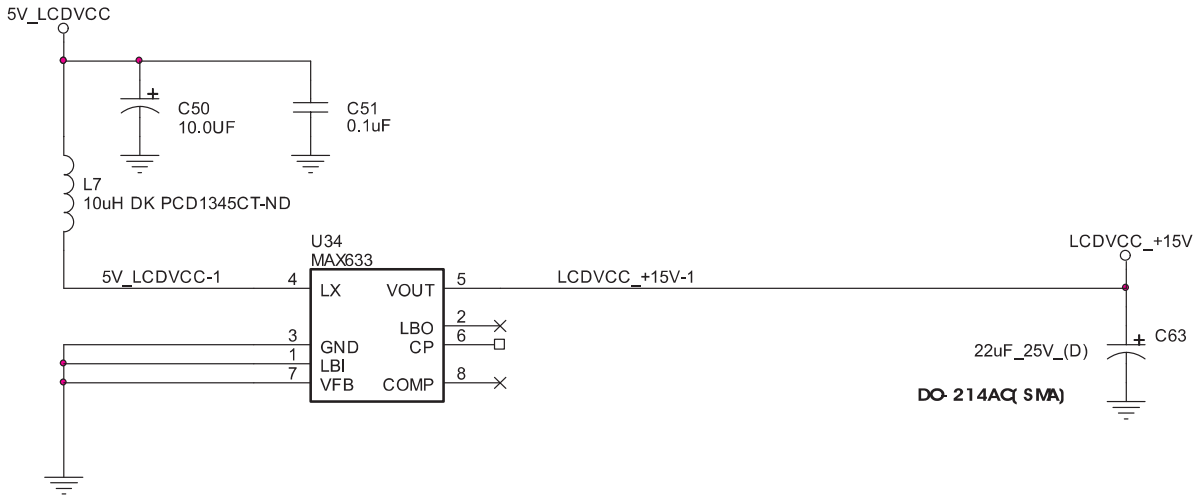
TPS61040DBV
SOT-23 PACKAGE
C2
4.7UF TANT 35V
C PACKAGE
R3
82
R2
0
EN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C50
10.0UF
C51
0.1uF
L7
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U34
MAX633
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4
LX
VOUT
5
LCDVCC_+15V-1
LCDVCC_+15V
3
GND
1
LBI
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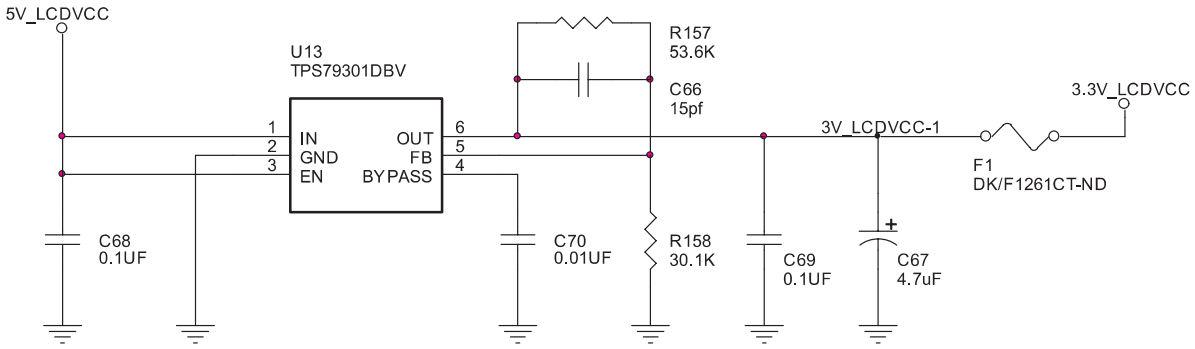
VFB
LBO
2
CP
6
COMP
8
C63
22uF_25V_(D)
DO-214AC(SMA)


5V_LCDVCC
U13
TPS79301DBV
R157
53.6K
C66
15pf
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3V_LCDVCC-1
1
IN
OUT
6
2
GND
FB
5
3
EN
BYPASS
4
F1
DK/F1261CT-ND
C68
0.1UF
C70
0.01UF
R158
30.1K
C69
0.1UF
C67
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## IMPORTANT NOTICE

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265