Application Report
SPRAAS3B–September 2009

TMS320TCI6487/88 Power Consumption Summary

Douglas Harrington

ABSTRACT

This document discusses the power consumption of the Texas Instruments TMS320TCI6487/88 digital signal processor (DSP). The power consumption on the TMS320TCI6487/88 device is highly application-dependent; therefore, a power spreadsheet that estimates power consumption is provided along with this application report. This spreadsheet can be used to model power consumption for user applications such as power supply design, thermal design, etc. To obtain good results from the spreadsheet, realistic usage parameters must be entered (see Section 3.1). The low-core voltage and other power design optimizations allow these devices to operate with industry-leading performance, while maintaining a low power-to-performance ratio.

The data presented in this document and in the accompanying spreadsheet were measured from devices at the maximum end of the power consumption for production devices. No production devices will have average power consumption that exceeds the spreadsheet values; therefore, the spreadsheet values may be used for board thermal analysis and power supply design as a maximum long-term average.

The spreadsheet discussed in this application report can be downloaded from the following URL: http://www-s.ti.com/sc/techlit/spraas3.zip .

Contents

List of Figures

List of Tables

1 Activity-Based Models

Power consumption for the TMS320TCI6487/88 DSP can vary widely depending on the use of on-chip resources. Therefore, the power consumption cannot be estimated accurately without an understanding of the components of the DSP in use and the usage patterns for those components. By providing the usage parameters that describe how and what is being used on the DSP, accurate power consumption numbers can be obtained for power-supply and thermal analysis. You can determine expected power consumption for worse case utilization, by choosing the peripherals in use.

The power spreadsheet divides the power consumption into two major components: baseline power and activity power.

1.1 Baseline Power

Baseline power consumption is the power consumed that is independent of chip activity such as static leakage power and core power. Core power includes clock tree, internal memory, on chip module power, etc. Baseline power is highly dependent on voltage, temperature, and CPU frequency.

1.2 Activity Power

Activity power consumption is power that is consumed by active parts of the DSP: central processing unit (CPU), enhanced direct memory access (EDMA), peripherals, etc. Active power is independent of temperature, but is dependent on activity levels of the CPU, EDMA, peripherals, etc. In the power spreadsheet, activity power is separated by the major modules/peripherals within the device. Therefore, the individual module/peripheral power consumption can be estimated independently. This helps with tailoring power consumption to the specific application.

Module/peripheral activity power consumption includes some necessary EDMA and CPU activity used to transfer data on-chip and off-chip when required. The power consumption, associated with EDMA and CPU activity, has been minimized to show only power consumption with respect to the module/peripheral tested.

2 Spreadsheet Parameters

The spreadsheet provides configurable parameters, which allow you to estimate power consumption based on configured usage parameters. To ensure realistic results, take care to make sure the spreadsheet is configured accurately. For more details, see Section 3.1. The parameters are as follows:

- Frequency: The operating frequency of a module/peripheral or the frequency of the external interface to that module.
- Modes: Selects
  - Receive accelerator (RAC) activity
    - High
    - Medium
    - Low
    - No activity
  - Ethernet media access controller (EMAC) SGMII mode
    - 1000/100/10 Mbps
  - Antenna interface (AIF)
    - OBSAI
    - CPRI
  - Serial RapidIO® (SRIO)
    - Number of lanes
    - Throughput
- % Utilization: The relative amount of time the module is active or in use versus off or idle.
- % Write: The relative amount of time (considering active time only) the module is transmitting versus receiving.
- Bits: Are the number of data bits being used in a selectable-width interface.
- % Switch: The probability that any one data bit on the relative data bus will change state from one cycle to the next.

2.1 Power Domains Details

The TMS320TCI6487/88 DSP has the capability to power-down and clock-gate peripherals within power domains [5:1]. When the power domain for a peripheral is disabled, the peripherals' memories are put to sleep for low-leakage mode and the peripheral is held in reset and clock-gated, thereby, reducing the power consumption of the device. Note that the device comes out of reset with power domains [5:1] disabled. The spreadsheet that accompanies this application report allows you to disable a power domain by selecting disable for the peripheral in the status column. The following peripherals have power domains available for power down:

- AIF – Power Domain1
- SRIO – Power Domain2
- RAC – Power Domain3
- Viterbi-Decoder Coprocessor 2 (VCP) – Power Domain4
- Turbo-Decoder Coprocessor 2 (TCP) – Power Domain5

For more information, see the *TMS320TCI6488 PSC User's Guide* (SPRUEF3) .

2.2 Device Modules/Peripherals

The TMS320TCI6487/88 power estimation spreadsheet contains the following modules with adjustable parameters:

- CPU[2:0]
- Rake/search accelerators (RSA[5:0])
- Timer[5:0]
- DDR2
- RAC
- Frame synchronization (FSYNC)
- AIF
- VCP
- TCP
- EMAC - SGMII
- SRIO
- Multichannel buffered seral port (McBSP[1:0])
- Inter-integrated chip (I2C)

EDMA is not listed as a separate module because the module/peripheral activity already includes any necessary EDMA activity used for memory-to-memory transfer only. For available peripheral configurations, see the device-specific data sheet.

3 Using the Power Estimation Spreadsheet

The use of the power estimation spreadsheet involves entering the appropriate usage parameters as input data in the spreadsheet. The following steps indicate how to use this spreadsheet:

1. Choose the appropriate CPU operating frequency. See the *TMS320TCI6487/TMS320TCI6488 Communications Infrastructure Digital Signal Processor Data Manual* (SPRS358) for valid operating frequencies.
2. Choose the case temperature for which you want to estimate power 0°C to 100°C.
3. Enable the appropriate peripherals used for your application including the mode, frequency, and bus width for that peripheral, if necessary.
4. Fill in the appropriate peripherals' or modules' % utilization, % writes, and % switching.

The spreadsheet takes the provided information and displays the details of power consumption for the chosen configuration.

As the spreadsheet is being configured, the settings are checked for conflicts, for example, if the peripheral's clock frequency is outside the allowed range, etc. For best results, enter the information from left to right, starting at the top and moving downward.

3.1 Choosing Appropriate Values

The frequency and bits user values are determined by design and the correct values to enter will be clear. You can disable unused modules/peripherals in the spreadsheet by selecting the *Disabled* tab in the column labeled *Status*. To choose the appropriate values, you need a good understanding of the read/write balance, bit switching required estimation, and utilization of the user application.

3.1.1 Utilization

For modules except the CPU, utilization is simply the percentage of the time the module spends doing something useful, versus being unused or idle. For these peripherals, there are no various degrees of use, so the value is just the average over time. For example, the DDR2 performs reads and writes one-quarter of the time, and has no data to move for the other three-quarters of the time (though it continues to perform background tasks like refreshes); this would be considered 25% utilization.

The CPU utilization is not as straightforward because there are varying degrees of use for the CPU. Here, 0% utilization means the CPU is active and does no useful work (NOP execution), whereas, 100% utilization is representative of a high activity condition with all eight functional units active every cycle, making use of the software-pipelined (SPLOOP) buffer hardware. The maximum amount of data is brought in every cycle. Few DSP algorithms achieve 100% utilization because this requires everything to be used every cycle with no stalls. Even intense applications do not spend all of the time in such highly parallel loops. Time is typically also spent executing control code or less demanding algorithms. Control type code may only execute a few instructions in parallel and significantly reduce the I/O of the CPU, thus, reducing overall utilization. Since you must consider the balance of CPU use for the application, entering 100% utilization is not practical for real applications.

For example, an application that executes control code (estimated at 25% of CPU capability) half of the time, and very dense DSP code (estimated at 90% of CPU capability) the other half, would have an average utilization of about 60% (25% × 50% + 90% × 50%). If the balance were changed to 25% control code and 75% DSP code, the weighted average would be approximately 74% utilization (25% × 25% + 90% × 75%). If the 25%/75% relation is kept, but the DSP code does not fully use all the CPU resources (estimate now at 75% of CPU capability) then the overall utilization returns approximately 63% (25% × 25% + 75% × 75%). By using estimates of intensity and duration of blocks of code in the application, an estimate of the overall CPU utilization can be obtained.

System level issues may also reduce utilization. Though the spreadsheet accepts 100% utilization for all peripherals, this is not possible in reality. As memory and EDMA bandwidth is consumed, peripheral activity is throttled back due to these bottlenecks, therefore, 100% utilization is not achievable. In applications with a lot of memory and/or EDMA usage, enter the individual module utilization numbers while keeping this overall limitation in mind.

3.1.2 % Writes

Peripherals that transmit as much as they receive have 50% writes; the spreadsheet assumes the remaining 50% of the time is spent on reads. In some applications, peripherals transmit in only one direction, or have a known balance of data movement. In these cases, the % writes option is not available for configuration. For the peripherals that have the % write configuration, 50% is a typical number that should be used.

3.1.3 %Switching

Random data has a 50% chance that any bit will change from one cycle to the next. Some applications may be able to predict this chance using some a priori information about the data set. If there is a property of the algorithm that allows prediction of the bit changes, the application-specific probability can be used. For all other applications, use the default number of 50%.

3.2 Peripheral Enabling and Disabling

As mentioned previously, the TMS320TCI6487/88 device provides the capability to enable/disable peripherals that are not within the always-on domain. This can be done by enabling the peripherals' power domains. The spreadsheet also allows you to disable peripherals within the always-on domain to ensure the peripherals' dynamic power is not included if the peripheral is not being used. For more information, see the device-specific data sheet and the *TMS320TCI6488 PSC User's Guide* (SPRUEF3) .

You can enable or disable a peripheral in the spreadsheet from the column labeled *Status*. If a peripheral is disabled, the CV_{DD} and I/O power for the peripheral will be zero. If the peripheral is enabled, with 0% utilization within the always-on power domain, the activity power for CV_{DD} and I/O will be zero. However, if a peripheral is enabled within power domain [5:1] with 0% utilization, the CV_{DD} supply reflects the delta power associated with powering up the peripherals' memories and enabling the peripherals' clock.

For more information, see the *TMS320TCI6488 PSC User's Guide* (SPRUEF3) .

4 Using the Results

The power data presented in this document and the accompanying spreadsheet is collected from devices considered to be at the maximum end of power consumption for production devices; no production units will have average power consumption that exceeds the spreadsheet values. The power consumption estimated by the spreadsheet is considered maximum average power consumption. Transient currents may cause power to spike above the spreadsheet values for a small amount of time; however, over a long period, the observed average power consumption will be below the spreadsheet value. The spreadsheet value may be used for board thermal analysis and power supply design as a maximum long-term average.

4.1 Adjusting I/O Power Results

I/O power is dependent not only on the DSP and activity, but also on the load being driven. For loads with CMOS inputs, the power required to drive the trace dominates; therefore, the power will scale based on the capacitance loading. The data presented in the spreadsheet for multichannel buffered serial port (McBSP), EMAC, and inter-integrated circuit (I2C) were loaded with approximately 2.5 inches of 50 Ω trace and serial termination.

For DDR2 and SRIO layout specification, see the device-specific physical guidelines documents.

4.2 Spreadsheet Layout and Details

The following sections discuss the spreadsheet layout and details.

4.2.1 Baseline Section of Spreadsheet

The baseline power portion, of the results section of the power spreadsheet, consolidates the average power associated with leakage, clock tree, and phase-locked loop (PLL) power. The clock tree power includes the power consumed by active clocks within the system. The Total System-on-Chip (SoC) (mW) column sums up the rows for leakage, clock tree, and PLL power.

4.2.2 Activity Section of Spreadsheet

The activity section of the spreadsheet contains the average power consumption associated with enabling a peripheral along with power consumed due to peripheral activity. The activity levels of a peripheral are defined by the peripheral frequency, % utilization, % writes, % switching, bus width, and peripheral mode.

4.2.3 Totals SoC Section of Spreadsheet

The totals section provides the total in each column for each power supply for Baseline plus Activity power. The total (mW) is equal to the total power for CV_{DD} and I/O all summed up i.e., total device power.

5 Spreadsheet Example

Section 5.2 demonstrates an example on how to choose appropriate values for a particular application. The values used in this example may be imported into the spreadsheet by clicking the *Base Station* button.

5.1 Idle Power Configuration

There is a button in the spreadsheet labeled *IDLE* that populates the following values:

- Case temperature: 100°C
- Device frequency: 1000 MHz
- CPU[2:0] 0% utilization
- All peripherals disabled

The IDLE power for CV_{DD} and I/O = 4.2 Watts

5.2 Typical Application

The following example provides an estimation of power consumption when the DSP is being used to process data for a typical application. The spreadsheet provides the estimated total power for core and I/O using the parameters defined below as input.

There is a button in the spreadsheet labeled *Thermal* that populates the following values.

- Case temperature: 100°C
- CPU[0] 15% utilization
- CPU[2:1] 30% utilization
- RAC medium activity
- RSA[5:2] active with 10% utilization
- Timer[5:0] active 75% utilization
- VCP2 10 % utilization
- TCP2 35 % utilization
- AIF CPRI 100% utilization
- FSYNC (enabled)
- SRIO active with two links at 3.125 Gbps with 5% utilization
- EMAC 1000 Mbps 10% utilization
- DDR2 (data rate 667 MHz, 10% utilization, 50% writes, 50% switching, 32-bits)
- McBSP0/1 (disabled)
- I2C (disabled)

The Typical Application total power for CV_{DD} and I/O = 7 Watts.

5.3 Power Supply Example

The macro button labeled *Power Supply* imports a DSP worse case average power consumption scenario for power supply and thermal design.

- Case temperature: 100°C
- CPU[0] 75% utilization
- CPU[2:1] 50% utilization
- RAC high activity
- RSA[5:2] active with 20% utilization
- Timer[5:0] active 75% utilization
- VCP2 15% utilization
- TCP2 25% utilization
- AIF CPRI 100% utilization
- FSYNC (enabled)

- SRIO active with two links at 3.125 Gbps with 17% utilization
- EMAC 1000 Mbps 10% utilization
- DDR2 (data rate 667 MHz, 66% utilization, 50% writes, 50% switching, 32-bits)
- McBSP0/1 (disabled)
- I2C 15% utilization, 50% switching

The Base Station total power for CV_{DD} and I/O = 8 Watts

6 TMS320TCI6487/88 Voltage supply Reference List

The voltage supply reference list provides a description for the pins connected to each power rail for power consumption.

Table 1. Power Pins

Group Name	Signal Name	Description
Cvdd	**CV** $_{DD}$	Core supply voltage
DVDD_IO_1.8	**DV** $_{DD\_18}$	1.8-V I/O supply voltage
	DV $_{DD1/2}$	1.8-V PLL1/2 supply voltage
	VDDDR	1.8-V AIF/SGR supply voltage
	AV $_{DDA}$	1.8-V EMU00/01 supply voltage
AIF_Vdd_1.1	**D** $_{DDD11}$	1.1-V AIF supply voltage
SGR-Vdd_1.1	**DV** $_{DD11}$	1.1-V SGR supply voltage
	DV $_{DDT}$	1.1-V SGR supply voltage
	DV $_{DDA}$	1.1-V SGR supply voltage

7 References

- *TMS320TCI6488 PSC User's Guide* (SPRUEF3)

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Broadband	www.ti.com/broadband
DSP	dsp.ti.com	Digital Control	www.ti.com/digitalcontrol
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Military	www.ti.com/military
Logic	logic.ti.com	Optical Networking	www.ti.com/opticalnetwork
Power Mgmt	power.ti.com	Security	www.ti.com/security
Microcontrollers	microcontroller.ti.com	Telephony	www.ti.com/telephony
RFID	www.ti-rfid.com	Video & Imaging	www.ti.com/video
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265