Application Report
SPRABW9A–October 2014–Revised July 2015

Migrating From KeyStone I to KeyStone II

High-Performance Multicore Processors

ABSTRACT

This guide describes the main System-on-Chip (SoC) level and peripheral changes that need to be considered when migrating a KeyStone I-based system design to a KeyStone II-based system design.

In this guide, KeyStone I includes all TMS320TCI661x devices and KeyStone II includes all TCI663xK2y devices. Any differences within KeyStone I or KeyStone II devices are described explicitly.

NOTE: The information in this document should be used in conjunction with information in the device-specific Keystone Architecture data manual that applies to the part number of your device.

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1 SoC-Level Migration

1.1 SoC-Level Migration Overview

This section describes the main SoC-level changes that must be considered when migrating a KeyStone I-based system design to a KeyStone II-based system design.

In this migration section, KeyStone I includes all TMS320TCI661x devices and KeyStone II includes all TCI663x devices. Any differences within KeyStone I or KeyStone II devices are explicitly mentioned.

There are some changes in KeyStone I and KeyStone II device nomenclature. The prefix of TMS320™ found on KeyStone I device nomenclature has been dropped from KeyStone II devices due to the architecture (KeyStone II, such as K2) and platform names (such as K, H, L, an so forth) are suffixed to the part numbers on the KeyStone II devices. The example of the TCI6630K2L device nomenclature is shown in Figure 1.

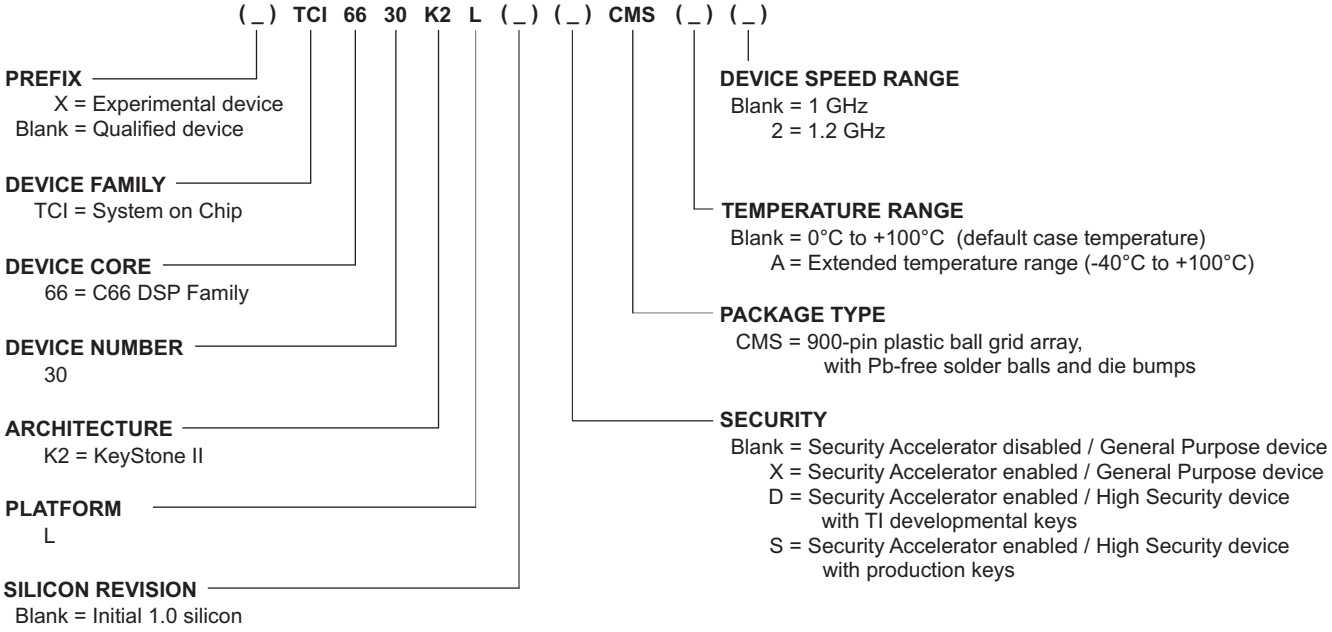

Figure 1. TCI6630K2L Device Nomenclature Example

1.2 Acronyms Used in This Document

Accronym	Definition
ACC	Accumulator Firmware
ARM	Advanced RISC Machines
AID	Antenna Interface Digital Front End
AIF	Antenna Interface
AIL	Antenna Interface CPRI/OBSAI Link
BCP	Bit Coprocessor
BCR	Receive Accelerator Coprocessor Broadcaster
CC	Channel Controllers
CFG	Configuration
CPPI	Communications Port Programming Interface (previous name for Multicore Navigator)
DSP	Digital Signal Processor
DDR	Dual Data Rate
EMIF	External Memory Interface Controller
EDMA	Enhanced Direct Memory Access
FDQ	Free Descriptor Queue
FFTC	Fast Fourier Transform Coprocessor
GPIO	General Purpose Input/Output
I2C	Inter Integrated Circuit
INTC	Interrupt Controller
INTD	Interrupt Distributor
IPC	Inter Processor Communication
IQN	IQNet Subsystem Antenna Interface
MSMC	Multicore Shared Memory Controller
MPU	Memory Protection Unit
OSR	On-Chip Standalone RAM
OTP	One Time Programmable Memory
PA	Packet Accelerator
PBIST	Programmable Built-In Self-Test
PCIE	Peripheral Component Interconnect Express
PDSP	Packet Data Structure Processor (used to run firmware to aid in QMSS functionality)
PLL	Phase Locked Loop
PKTDMA	Packet DMA (previously called CPPI-DMA or C-DMA)
PSC	Power Sleep Controller
QoS	Quality of Service Firmware
QM, QMSS	Queue Manager, Queue Manager Subsystem
RAC	Receive Accelerator Coprocessor
RSA	Rake Search Accelerator
SA	Security Accelerator
SGMII	Serial Gigabit Media Independent Interface
SMP	Symmetric Multi-Processing
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
STM	System Trace Module
TC	Transfer Controllers
TAC	Transmit Accelerator Coprocessor
TAC FL	Transmit Accelerator Coprocessor Functional Library
TCP	Turbo Coprocessor

Accronym	Definition
TETB	TI Embedded Trace Buffer
UART	Universal Asynchronous Receive/Transmit
VFP	Vector Floating Point
XGE	10 Gigabit Ethernet

1.3 Architectural Differences

Table 1 gives the architecture-related points, which should be considered for migrating a system using KeyStone I devices to a system using KeyStone II devices. For more details specific to individual KeyStone I and KeyStone II devices, see the device-specific data manuals.

Table 1. Architectural Differences Between KeyStone I and KeyStone II Devices

IP Block	KeyStone I	KeyStone II	Minimal to Moderate SW Changes (MMRs Added / Changed or Added Functionality)	New SW to Support New HW Block
Core and Memory Subsystem				
C66x DSP Core	4x	4x, 8x(1)	Completely software compatible	
ARM Cortex-A8 core(2)	1x	No		Required
ARM Cortex-A15 core	No	2x, 4x(3)		Required
MSMC	1x	1x	MMRs added to support additional cores	
DDR3 EMIF (64-bit)	1x	1x, 2x(4)	1) Programming changed due to PHY and EMIF controller changes 2) Changes to SDRAM settings to support up to DDR3-1600 3) Support for data obfuscation 4) DDR3A EMIF is connected to MSMC port, hence need MPAX setup to access EMIF MMRs (similar to TMS320TCI6618 device) 5) But DDR3B EMIF is connected to TeraNet, hence doesn't need any MPAX setup to access EMIF MMRs. 6) DDR3B has a storage capacity of 2 GB. The complete 2 GB is accessible from both DSP and ARM. The system masters can access only the first 512 MB of DDR3B memory.	
Memory				
L1P per DSP core (cache / SRAM)	32 Kbytes	32 Kbytes		
L1D per DSP core (cache / SRAM)	32 Kbytes	32 Kbytes		
L2 per DSP core (cache / SRAM)	1 Mbytes	1 Mbytes		
L1P cache per ARM core	32 Kbytes(5)	32 Kbytes		
L1D cache per ARM core	32 Kbytes(6)	32 Kbytes		
SL2 cache for all 4 ARM cores	256 Kbytes(7)	1, 4 Mbytes(8)		
MSMC SRAM	2 Mbytes	2, 6 Mbytes(9)		

(1) 8 C66x CorePac are available only in TCI6636K2H and TCI6638K2K.
(2) One ARM Cortex-A8 is present in TMS320TCI6612 and TMS320TCI6614.
(3) 4 ARM Cortex-A15s are available only in TCI6636K2H and TCI6638K2K.
(4) DDR3A and DDR3B are available only in TCI6636K2H and TCI6638K2K.
(5) Applicable only for TMS320TCI6612 and TMS320TCI6614.
(6) Applicable only for TMS320TCI6612 and TMS320TCI6614.
(7) Applicable only for TMS320TCI6612 and TMS320TCI6614.
(8) 4Mbytes are available only in TCI6636K2H and TCI6638K2K.
(9) 6Mbits of MSMC is available only in TCI6636K2H and TCI6638K2K.

Table 1. Architectural Differences Between KeyStone I and KeyStone II Devices (continued)

IP Block	KeyStone I	KeyStone II	Minimal to Moderate SW Changes (MMRs Added / Changed or Added Functionality)	New SW to Support New HW Block
DDR3A memory (max)	8 Gbytes	8 Gbytes[10]		
DDR3B memory (max)[11]	No	2 Gbytes (for ARM and DSP cores) and 512 Mbytes (system masters)[10]		
DSP Boot ROM	128 Kbytes	128 Kbytes		
ARM Boot ROM	No	256 Kbytes		
OTP memory	No[12]	4 Kbits		
OSR[13]	No	1Mbytes		
Hardware Coprocessors				
RAC	2x	1x, 4x[14]	RAC subsystem programming changed due to Receive Accelerator Coprocessor Broadcaster (BCR) (RAC broadcaster)	Required for BCR support
TAC[15]	1x	1x	Capacity is tripled, software changes needed to support new features	
FFTC	3x	2x, 6x[16]	Software changes needed for 8-bit support	
Bit Coprocessor (BCP)	1x	1x	Completely software compatible	
TCP3d	3x	2x, 4x[17]	Completely software compatible	
TCP3e	1x	No	TCP3e is integrated in the BCP so not required external	
VCP2	4x	4x, 8x[18]	Completely software compatible	
RSA1	4x	8x, 16x[19]	Completely software compatible	
Multicore Navigator				
Queue manager subsystem + PKTDMA	1x	2x	1) Double no. of queues (8K to 16K) 2) Descriptor size doubled (512K to 1M) 3) 2 Queue Managers and 2 Infrastructure DMAs 4) Queue event mapping changed	
EDMA3				
EDMA3CC	3x	3x, 5x[20]	1) More EDMA3CC instances added 2) Larger PaRAM sizes 3) Event mapping changed	
EDMA3TC	10x	10x, 14x[21]	More EDMA3TC instances added	
Network Coprocessor[22]				
Packet Accelerator (PA)	1x	1x	Completely software compatible	
Security Accelerator (SA)	1x	1x	Capacity doubled	

(10) With ECC capability. ECC is enhanced with a Read-Modify-Write sub-block which enables support for ECC generation in sub 64-bit accesses.
(11) DDR3B is available only in TCI6636K2H and TCI6638K2K.
(12) 4 Kbits of OTP memory is available only for TMS320TCI6612 and TMS320TCI6614.
(13) 1Mbits of OSR is available only in TCI6630K2L and TCI6631K2L.
(14) 4 RAC1.2 are available only in TCI6636K2H and TCI6638K2K.
(15) TCI6630K2L and TCI6631K2L have TAC2.2 instead of TAC2.1 used in others. TAC2.2 has 2 SGCP, 1 FEI and 1 BEI, whereas TAC2.1 had 6 SGCP, 3 FEI and 1 BEI
(16) 6 FFTC are available only in TCI6636K2H and TCI6638K2K.
(17) 4 TCP3d are available only in TCI6636K2H and TCI6638K2K.
(18) 8 VCP2 are available only in TCI6630K2H and TCI6638K2K.
(19) TCI6631 has no RSA1, TCI6630 has 8 RSA1 and TCI6636K2H and TCI6638K2K have 16 RSA1.
(20) 5 EDMA3CC are available only in TCI6636K2H and TCI6638K2K.
(21) 14 EDMA3TCs are available only in TCI6636K2H and TCI6638K2K.
(22) NetCP 1.5 is available only in TCI6630K2L and TCI6631K2L.It has the PA1.5 and SA1.3 whereas others use PA1.1 andSA1.2

Table 1. Architectural Differences Between KeyStone I and KeyStone II Devices (continued)

IP Block	KeyStone I	KeyStone II	Minimal to Moderate SW Changes (MMRs Added / Changed or Added Functionality)	New SW to Support New HW Block
Gigabit Ethernet Switch Subsystem (SGMII)	1 x 2	1 x 4	Support for 4 ports vs. 2 ports	Required support for new time sync operations
Peripherals				
AIF2[23]	1 x 6	1 x 6	1) Changes needed to support additional AT events (from 11 to 24 events) 2) SerDes related changes to MMRs	
IQNet2	No	1x[24]		Required
SRIO	1 x 4	1 x 4[25]	SerDes related changes to MMRs	
PCIe	1 x 2	1 x 2, 2x1[26]	SerDes related changes to MMRs	
HyperLink	1 x 2	2 x 4[27]	1) SerDes related changes to MMRs, 2) Some KeyStone II devices have 2 HyperLink modules, where as KeyStone I devices have only 1 HyperLink module	
XGE[28]	No	1 x 2		Required
UART	1x	2x, 4x[29]	Completely software compatible	
SPI	1x[30]	3x[31]	Support for additional chip selects (4 vs. 2) per SPI module	
I2C	1x	3x	Completely software compatible	
GPIO	1x16, 1x32[32]	1x32, 2x32[33]	Support for 32 GPIO pins vs. 16 pins	
Timer64	8x[34]	14x, 20x[35]	Completely sofware compatible	
Semaphore	1x	1x	1) More semaphores added (64 vs. 32) 2) Support for additional cores	
EMIF16[36]	1x	1x	Completely sofware compatible	
USIM[37]	1x	1x	Completely sofware compatible	
USB3	No	1x		Required
System Components				
PLL controller + On-chip PLLs	3x	5x	1) one additional PLL for DDR3B and one more for ARM subsystem[38] 2) programming identical to DDR3A PLL	
PSC			1) More power and clock domains added 2) LPSC allocations changed 3) Software needs to be modified to use the respective power/clock domains for peripheral power on and clocking	

[23] AIF2 is available only in TCI6636K2H and TCI6638K2K and KeyStone I devices.
[24] IQN2 is available only in TCI6630K2L and TCI6631K2L.
[25] SRIO is not available only in TCI6630K2L and TCI6631K2L.
[26] 2 PCIes (with 1 lane) are available only in TCI6630K2l and TCI6631K2L. Others have 1 PCIe (with 2 lanes).
[27] 2 HyperLink are available only in TCI6636K2H and TCI6638K2K.
[28] XGE is available only in TCI6636K2H and TCI6638K2K.
[29] 4 UARTs are available only in TCI6630K2L and TCI6631K2L.
[30] KeyStone I SPI supports 2 CSs.
[31] TCI6630K2L and TCI6631K2L support 5 CSs for SPI0 and SPI2 and 3 CSs for SPI1.
[32] 32 GPIOs are available for TMS320TCI6612 and TMS320TCI6614.
[33] 64 GPIOs are available only in TCI6630K2L and TCI6631K2L.
[34] 12 Timers are available for TMS320TCI6612 and TMS320TCI6614.
[35] 20 Timers are available only in TCI6636K2H and TCI6638K2K.
[36] EMIF16 is available only in the following KeyStone I(TMS320TCI6612 and TMS320TCI6614) and KeyStone II devices.
[37] USIM is available only in the following KeyStone I(TMS320TCI6612 and TMS320TCI6614) and KeyStone II devices.
[38] Applicable only for TCI6636K2H and TCI6638K2K.

Table 1. Architectural Differences Between KeyStone I and KeyStone II Devices (continued)

IP Block	KeyStone I	KeyStone II	Minimal to Moderate SW Changes (MMRs Added / Changed or Added Functionality)	New SW to Support New HW Block
BOOTCFG (Chip-level registers)			1) New chip-level MMRs added 2) Some existing MMRs also changed (for example no KICK protection for IPC registers, support for added cores, and so forth)	
Bootmode			Bootmode pin allocations changed	
INTC + GIC (for ARM)	3x or 4x[39] (INTCs)	2x, 3x (INTCs) and 1x (GIC)[40]	1) More INTC instantiations 2) Interrupt allocations changed	
Debug Subsystem + System TETB	1x	1x	Software change needed to support additional cores and added features	System TETB is a new HW block
ARM Subsystem ETB (16 KB)[41]	No	1x		Required
DSP TETB (4 KB)	4x	8x	Completely software compatible	
Tracer	16x	32x	Tracer allocations changed	
MPU	6x	16x	MPU allocations changed	
Security Manager	1x	1x	Completely software compatible	
Smart Reflex	1x	1x, 2x[42]	Completely software compatible	

(39) INTC3 is used for routing interrupts to ARM and is available only in TMS320TCI6612 and TMS320TCI6614.
(40) 3 INTC are available only for TCI6636K2H and TCI6638K2K.
(41) Applicable only for KeyStone II devices.
(42) 2 Smart Reflex are available only for TCI6636K2H and TCI6638K2K.

1.4 Memory Map

Both KeyStone I and KeyStone II devices feature on-chip internal memories, allowing efficient handling of varied partitions of internal program and data information. Both devices feature several different types of cache memory, allowing significant flexibility in using this memory to enhance algorithm performance. Both devices also provide an on-chip ROM, which contains the bootloader program. The memory map has changed considerably moving from KeyStone I to KeyStone II devices. For more details about the device memory map, see the device-specific data manuals. For KeyStone II devices, the device memory map is viewed differently from the ARM® (ARM A15 CorePac), the DSP CorePacs, and the system masters (SoC level). The view of the device memory map from these different entities is summarized in Table 2.

Table 2. KeyStone II Memory Map View From ARM, DSP, and System Masters

Start Address	End Address	ARM View	DSP View (After XMC)[1]	SoC view (After MPAX)[2]
0x00_0000_0000	0x00_0003_FFFF	ARM ROM	DSP Internal	ARM ROM
0x00_0004_0000	0x00_0100_0000	Reserved	DSP Internal	Reserved
0x00_0100_0000	0x00_0100_FFFF	ARM Internal	DSP Internal	Reserved
0x00_0101_0000	0x00_010F_FFFF	Reserved	DSP Internal	Reserved
0x00_0110_0000	0x00_0110_FFFF	ARM Internal	DSP Internal	Reserved
0x00_0111_0000	0x00_01BF_FFFF	Reserved	DSP Internal	Reserved
0x00_01C0_0000	0x00_20FF_FFFF	CFG/DMA Space	CFG/DMA Space	CFG/DMA Space
0x00_2100_0000	0x00_2100_01FF	DDR3A CFG[3]	DDR3A CFG	DDR3A CFG
0x00_2100_0200	0x00_5FFF_FFFF	CFG/DMA Space	CFG/DMA Space	CFG/DMA Space
0x00_6000_0000	0x00_7FFF_FFFF	DDR3B(Aliased from 0x8000_0000 - 0x9FFF_FFFF)	DDR3B (Aliased from 0x8000_0000 - 0x9FFF_FFFF)	DDR3B

(1) For DSP CorePac to access 40 bit address space, the XMC MPAX has to be programmed accordingly
(2) For System masters to access 40 bit address space, the MSMC MPAX has to be programmed accordingly
(3) DDR3A configuration space access requires re-mapping of 0x2100_0000 - 0x2100_01FF to 0x01_2100_0000 - 0x01_2100_01FF using XMC MPAX for DSP CorePac accesses and MSMC MPAX for System master accesses

Table 2. KeyStone II Memory Map View From ARM, DSP, and System Masters (continued)

Start Address	End Address	ARM View	DSP View (After XMC)[1]	SoC view (After MPAX)[2]
0x00_8000_0000	0x00_FFFF_FFFF	DDR3B[4]	DDR3B	DDR3A
0x01_2100_0000	0x01_2100_01FF	Reserved	DDR3A CFG	DDR3A CFG
0x08_0000_0000	0x09_FFFF_FFFF	DDR3A	DDR3A	DDR3A

(4) To enable ARM to boot Linux kernel from DDR3A without setting up MMU/LPAE, DDR3A can be mapped into the lower 32 bit address space, by setting the bootstrap pin ddr3a_map_en = 1. If this pin is set, the address from 0x00_8000_0000 - 0x00_FFFF_FFFF will be aliased at 0x08_0000_0000 - 0x08_7FFF_FFFF

The differences in the device memory map between KeyStone I and KeyStone II devices are shown in Table 3. Some software modifications may be required when migrating applications from KeyStone I devices to KeyStone II devices. For more details about the memory map of individual KeyStone I and KeyStone II devices, see the device-specific data manuals.

Table 3. KeyStone I to KeyStone II (TCI6638K2K) Memory Map Changes

Logical 32-Bit Address		Physical 40-Bit Address				
Start	End	Start	End	Bytes	KeyStone II(TCI6638K2K)	KeyStone I
0000 0000	0003 FFFF	00 0000 0000	00 0003 FFFF	256K	COREPAC_INTERNAL/ BOOT_ROM_ARM[1]	Reserved
0100 0000	017F FFFF	00 0100 0000	00 017F FFFF	8 M	COREPAC_INTERNAL[2]	Reserved
01D6 8000	01D6 807F	00 01D6 8000	00 01D6 807F	128	CPT_L2_4_CFG	CPT_RAC_FEI
01D7 0000	01D7 007F	00 01D7 0000	00 01D7 007F	128	CPT_L2_5_CFG	CPT_RAC_CFG
01D7 8000	01D7 807F	00 01D7 8000	00 01D7 807F	128	CPT_L2_6_CFG	CPT_TAC_BE
01D8 0000	01D8 007F	00 01D8 0000	00 01D8 007F	128	CPT_L2_7_CFG	Reserved
01D8 8000	01D8 807F	00 01D8 8000	00 01D8 807F	128	CPT_RAC_FEI_CFG	Reserved
01D9 0000	01D9 007F	00 01D9 0000	00 01D9 007F	128	CPT_RAC_CFG1_CFG	Reserved
01D9 8000	01D9 807F	00 01D9 8000	00 01D9 807F	128	CPT_TAC_BE_CFG	Reserved
01DA 0000	01DA 007F	00 01DA 0000	00 01DA 007F	128	CPT_QM_CFG2_CFG	Reserved
01DA 8000	01DA 807F	00 01DA 8000	00 01DA 807F	128	CPT_RAC_CFG2_CFG	Reserved
01DB 0000	01DB 007F	00 01DB 0000	00 01DB 007F	128	CPT_DDR3B_CFG	Reserved
01DB 8000	01DB 807F	00 01DB 8000	00 01DB 807F	128	CPT_BCR_CFG_CFG	Reserved
01DC 0000	01DC 007F	00 01DC 0000	00 01DC 007F	128	CPT_TPCC0_4_CFG	Reserved
01DC 8000	01DC 807F	00 01DC 8000	00 01DC 807F	128	CPT_TPCC1_2_3_CFG	Reserved
01DD 0000	01DD 007F	00 01DD 0000	00 01DD 007F	128	CPT_INTC_CFG	Reserved
01DD 8000	01DD 807F	00 01DD 8000	00 01DD 807F	128	CPT_MSMC4_CFG	Reserved
01DE 0000	01DE 007F	00 01DE 0000	00 01DE 007F	128	CPT_MSMC5_CFG	Reserved
01DE 0080	01DE 00FF	00 01DE 0080	00 01DE 00FF	128	CPT_MSMC6_CFG	Reserved
01DE 0100	01DE 017F	00 01DE 0100	00 01DE 017F	128	CPT_MSMC7_CFG	Reserved
01DE 8000	01DE 807F	00 01DE 8000	00 01DE 807F	128	CPT_SPI_ROM_ EMIF16_CFG	Reserved
01E8 0000	01E8 3FFF	00 01E8 0000	00 01E8 3FFF	16K	ARM_CFG	Reserved
01E8 4000	01E8 43FF	00 01E8 4000	00 01E8 43FF	1K	MSMC_PBIST_CTL	Reserved
0218 0000	021A FFFF	00 0218 0000	00 021A FFFF	192k	Reserved	TAC Control
021C 4000	021C 43FF	00 021C 4000	00 021C 43FF	1K	TCP3D_C_CFG	Reserved
021C 6000	021C 63FF	00 021C 6000	00 021C 63FF	1K	TCP3D_D_CFG	Reserved
021D F000	021DF07F	00 021D F000	00 021DF07F	128	USIM_CFG	Reserved
021E 0000	021E 00FF	00 021E 0000	00 021E 00FF	256	OTP_CFG	TCP3E (8K)
021F 0800	021F 0FFF	00 021F 0800	00 021F 0FFF	2K	FFTC_E_CFG	Reserved
021F 1000	021F 17FF	00 021F 1000	00 021F 17FF	2K	FFTC_F_CFG	Reserved

(1) This memory region is used for ARM boot ROM at chip-level and CorePac internal space inside CorePac. Where ARM boots from is hardcoded inside ARM IP.

(2) Addresses starting at 0x0100 0000 will be used for en_cfg_space and 0x0110 0000 will be used for stm space internal to ARM.

Table 3. KeyStone I to KeyStone II (TCI6638K2K) Memory Map Changes (continued)

Logical 32-Bit Address		Physical 40-Bit Address		Bytes	KeyStone II(TCI6638K2K)	KeyStone I
Start	End	Start	End			
021F 8000	021F 87FF	00 021F 8000	00 021F 87FF	2K	FFTC_C_CFG	Reserved
021FC000	021F C7FF	00 021FC000	00 021F C7FF	2K	FFTC_D_CFG	Reserved
0228 0000	0228 007F	00 0228 0000	00 0228 007F	128	TIMER8_CFG	Reserved[3]
0229 0000	0229 007F	00 0229 0000	00 0229 007F	128	TIMER9_CFG	Reserved
022A 0000	022A 007F	00 022A 0000	00 022A 007F	128	TIMER10_CFG	Reserved
022B 0000	022B 007F	00 022B 0000	00 022B 007F	128	TIMER11_CFG	Reserved
022C 0000	022C 007F	00 022C 0000	00 022C 007F	128	TIMER12_CFG	Reserved
022D 0000	022D 007F	00 022D 0000	00 022D 007F	128	TIMER13_CFG	Reserved
022E 0000	022E 007F	00 022E 0000	00 022E 007F	128	TIMER14_CFG	Reserved
022F 0000	022F 007F	00 022F 0000	00 022F 007F	128	TIMER15_CFG	Reserved
022F 0080	022F 00FF	00 022F 0080	00 022F 00FF	128	TIMER16_CFG	Reserved
022F 0100	022F 017F	00 022F 0100	00 022F 017F	128	TIMER17_CFG	Reserved
022F 0180	022F 01FF	00 022F 0180	00 022F 01FF	128	TIMER18_CFG	Reserved
022F 0200	022F 027F	00 022F 0200	00 022F 027F	128	TIMER19_CFG	Reserved
0232 0000	0232 3FFF	00 0232 0000	00 0232 3FFF	16K	PCIE_SERDES_CFG	GPIO: 02320000 to 023200FF. Rest reserved.
0232 4000	0232 5FFF	00 0232 4000	00 0232 5FFF	8K	AIF2_SERDES_B4_CFG	
0232 6000	0232 7FFF	00 0232 6000	00 0232 7FFF	8K	AIF2_SERDES_B8_CFG	
0232 8000	0232 8FFF	00 0232 8000	00 0232 8FFF	4K	DDR3B_PHY_CFG	
0232 9000	0232 9FFF	00 0232 9000	00 0232 9FFF	4K	DDR3A_PHY_CFG	
0232 A000	0232 AFFF	00 0232 A000	00 0232 AFFF	4K	NETCP_SERDES_CFG	
0232 B000	0232 BFFF	00 0232 B000	00 0232 BFFF	4K	HyperLink0_SERDES_CFG	
0232 C000	0232 CFFF	00 0232 C000	00 0232 CFFF	4K	SRIO_SERDES_CFG	
0232 D000	0232 DFFF	00 0232 D000	00 0232 DFFF	4K	HyperLink1_SERDES_CFG	
0232 E000	0232 EFFF	00 0232 E000	00 0232 EFFF	4K	XGE_SERDES_CFG	
0232 F000	0232 FFFF	00 0232 F000	00 0232 FFFF	4K	USB_PHY_CFG	
0233 0400	0233 07FF	00 0233 0400	00 0233 07FF	1K	Smart Reflex 1	Reserved
0234 0000	0234 00FF	00 0234 0000	00 0234 00FF	256	VCP2_E_CFG	Reserved
0234 4000	0234 40FF	00 0234 4000	00 0234 40FF	256	VCP2_F_CFG	Reserved
0234 8000	0234 80FF	00 0234 8000	00 0234 80FF	256	VCP2_G_CFG	Reserved
0234 C000	0234 C0FF	00 0234 C000	00 0234 C0FF	256	VCP2_H_CFG	Reserved
0238 8000	0238 83FF	00 0238 8000	00 0238 83FF	1K	MPU5_CFG	Reserved
0238 8400	0238 87FF	00 0238 8400	00 0238 87FF	1K	MPU6_CFG	Reserved
0238 8800	0238 8BFF	00 0238 8800	00 0238 8BFF	1K	MPU7_CFG	Reserved
0238 8C00	0238 8FFF	00 0238 8C00	00 0238 8FFF	1K	MPU8_CFG	Reserved
0238 9000	0238 93FF	00 0238 9000	00 0238 93FF	1K	MPU9_CFG	Reserved
0238 9400	0238 97FF	00 0238 9400	00 0238 97FF	1K	MPU10_CFG	Reserved
0238 9800	0238 9BFF	00 0238 9800	00 0238 9BFF	1K	MPU11_CFG	Reserved
0238 9C00	0238 9FFF	00 0238 9C00	00 0238 9FFF	1K	MPU12_CFG	Reserved
0238 A000	0238 A3FF	00 0238 A000	00 0238 A3FF	1K	MPU13_CFG	Reserved
0238 A400	0238 A7FF	00 0238 A400	00 0238 A7FF	1K	MPU14_CFG	Reserved
0240 0000	0243 FFFF	00 0240 0000	00 0243 FFFF	256K	Reserved	debug_SS_config
0248 0000	0248 3FFF	00 0248 0000	00 0248 3FFF	16K	ADTF4_CFG	Reserved
0249 0000	0249 3FFF	00 0249 0000	00 0249 3FFF	16K	ADTF5_CFG	Reserved
024A 0000	024A 3FFF	00 024A 0000	00 024A 3FFF	16K	ADTF6_CFG	Reserved
024B 0000	024B 3FFF	00 024B 0000	00 024B 3FFF	16K	ADTF7_CFG	Reserved

(3) Timers 8-11 are applicable only for TMS320TCI6614 and TMS320TCI6612

Table 3. KeyStone I to KeyStone II (TCI6638K2K) Memory Map Changes (continued)

Logical 32-Bit Address		Physical 40-Bit Address		Bytes	KeyStone II(TCI6638K2K)	KeyStone I
Start	End	Start	End			
024C 0800	024C 0BFF	00 024C 0800	00 024C 0BFF	1K	PBIST_CTL1_CFG	Reserved
0250 0000	0250 7FFF	00 0250 0000	00 0250 7FFF	32K	SEC_MGR_CFG	SEC_CTL (0250 0000 to 0250 007F, Rest is reserved)
0252 0000	0252 03FF	00 0252 0000	00 0252 03FF	1K	Reserved	SEC_KEY_MGR
0253 0400	0253 047F	00 0253 0400	00 0253 047F	128	I2C1_CFG	Reserved
0253 0800	0253 087F	00 0253 0800	00 0253 087F	128	I2C2_CFG	Reserved
0253 0C00	0253 0C3F	00 0253 0C00	00 0253 0C3F	64	UART0_CFG	Reserved
0253 1000	0253 103F	00 0253 1000	00 0253 103F	64	UART1_CFG	Reserved
0254 0000	0255 FFFF	00 0254 0000	00 0255 FFFF	128K	BCP_CFG	UART (up to 0254003F, Rest is reserved)
0256 0000	0257 FFFF	00 0256 0000	00 0257 FFFF	128K	GIC_CFG	Reserved
0258 0000	025F FFFF	00 0258 0000	00 025F FFFF	512K	TAC_CFG	Reserved
0260 BF00	0260 BFFF	00 0260 BF00	00 0260 BFFF	256	GPIO_CFG	Reserved
0268 0000	026F FFFF	00 0268 0000	00 026F FFFF	512K	USB_MMR_CFG	Reserved
0270 8000	0270 FFFF	00 0270 8000	00 0270 FFFF	32K	EDMA4_CC_CFG	Reserved
0272 8000	0272 FFFF	00 0272 8000	00 0272 FFFF	32K	EDMA3_CC_CFG	Reserved
027B 0000	027B 03FF	00 027B 0000	00 027B 03FF	1K	EDMA3_TC0_CFG	Reserved
027B 8000	027B 83FF	00 027B 8000	00 027B 83FF	1k	EDMA3_TC1_CFG	Reserved
027B 8400	027B 87FF	00 027B 8400	00 027B 87FF	1K	EDMA4_TC0_CFG	Reserved
027B 8800	027B 8BFF	00 027B 8800	00 027B 8BFF	1K	EDMA4_TC1_CFG	Reserved
027C 0000	027C 03FF	00 027C 0000	00 027C 03FF	1K	BCR_CFG	Reserved
027D 4000	027D 7FFF	00 027D 4000	00 027D 7FFF	16K	TBR_SYS_ARM	Reserved
0281 0000	0281 3FFF	00 0281 0000	00 0281 3FFF	16k	TETB4_CFG	Reserved
0282 0000	0282 3FFF	00 0282 0000	00 0282 3FFF	16k	TETB5_CFG	Reserved
0283 0000	0283 3FFF	00 0283 0000	00 0283 3FFF	16k	TETB6_CFG	Reserved
0284 0000	0284 3FFF	00 0284 0000	00 0284 3FFF	16k	TETB7_CFG	Reserved
0285 0000	0285 7FFF	00 0285 0000	00 0285 7FFF	32k	DBG_TBR_SYS	TETB4 (system trace)
02A0 0000	02AF FFFF	00 02A0 0000	00 02AF FFFF	1M	QM_CFG1 and QM_CFG2	QM_SS_CFG
02B0 0000	02BF FFFF	00 02B0 0000	00 02BF FFFF	1M	QM_CFG2 Linking RAM	Reserved
02C0 0000	02C5 FFFF	00 02C0 0000	00 02C5 FFFF	384K	RAC_C_CFG	Reserved
02C8 0000	02CD FFFF	00 02C8 0000	00 02CD FFFF	384K	RAC_D_CFG	Reserved
02F0 0000	02FF FFFF	00 02F0 0000	00 02FF FFFF	1M	XGE_CFG	Reserved
0300 0000	030F FFFF	00 0300 0000	00 030F FFFF	1M	DBG_CFG	Reserved
0C00 0000	0C1F FFFF	00 0C00 0000	00 0C1F FFFF	2M	MSMC SRAM	MSMC SRAM
0C20 0000	0C5F FFFF	00 0C20 0000	00 0C5F FFFF	4M	MSMC SRAM	Reserved
1480 0000	148F FFFF	00 1480 0000	00 148F FFFF	1M	COREPAC4_SDMA - L2 SRAM	Reserved
14E0 0000	14E0 7FFF	00 14E0 0000	00 14E0 7FFF	32K	COREPAC4 L1P SRAM	Reserved
14F0 0000	14F0 7FFF	00 14F0 0000	00 14F0 7FFF	32K	COREPAC4 L1D SRAM	Reserved
1580 0000	158F FFFF	00 1580 0000	00 158F FFFF	1M	COREPAC5_SDMA - L2 SRAM	Reserved
15E0 0000	15E0 7FFF	00 15E0 0000	00 15E0 7FFF	32K	COREPAC5 L1P SRAM	Reserved
15F0 0000	15F0 7FFF	00 15F0 0000	00 15F0 7FFF	32K	COREPAC5 L1D SRAM	Reserved
1680 0000	168F FFFF	00 1680 0000	00 168F FFFF	1M	COREPAC6_SDMA - L2 SRAM	Reserved
16E0 0000	16E0 7FFF	00 16E0 0000	00 16E0 7FFF	32K	COREPAC6 L1P SRAM	Reserved
16F0 0000	16F0 7FFF	00 16F0 0000	00 16F0 7FFF	32K	COREPAC6 L1D SRAM	Reserved

Table 3. KeyStone I to KeyStone II (TCI6638K2K) Memory Map Changes (continued)

Logical 32-Bit Address		Physical 40-Bit Address		Bytes	KeyStone II(TCI6638K2K)	KeyStone I
Start	End	Start	End			
1780 0000	178F FFFF	00 1780 0000	00 178F FFFF	1M	COREPAC7_SDMA - L2 SRAM	Reserved
17E0 0000	17E0 7FFF	00 17E0 0000	00 17E0 7FFF	32K	COREPAC7 L1P SRAM	Reserved
17F0 0000	17F0 7FFF	00 17F0 0000	00 17F0 7FFF	32K	COREPAC7 L1D SRAM	Reserved
2020 0000	205F FFFF	00 2020 0000	205F FFFF	4M	Reserved	RAC_B Data (FEI)
2070 0000	207F FFFF	00 2070 0000	00 207F FFFF	1M	TCP3D_C_DATA	Reserved
2090 0000	209F FFFF	00 2090 0000	00 209F FFFF	1M	TCP3D_D_DATA	TCP3E Data (2090 0000 to 2090 3FFF, Rest is reserved)
20BF 0000	20BF FFFF	00 20BF 0000	00 20BF FFFF	64K	Reserved	SPI (20BF 0000 to 20BF 01FF, Rest is Reserved)
2100 0000	2100 03FF	00 2100 0000	00 2100 03FF	1K	Reserved	DDR3-EMIF Config
2100 0400	2100 05FF	00 2100 0400	00 2100 05FF	512	SPI0 Slave	Reserved
2100 0600	2100 07FF	00 2100 0600	00 2100 07FF	512	SPI1 Slave	Reserved
2100 0800	2100 09FF	00 2100 0800	00 2100 09FF	512	SPI2 Slave	Reserved
2100 0A00	2100 0AFF	00 2100 0A00	00 2100 0AFF	256	EMIF16_CONFIG	Reserved
2101 0000	2101 01FF	01 2101 0000	01 2101 01FF	512	DDR3A_CONFIG	Reserved
2102 0000	2103 FFFF	00 2102 0000	00 2103 FFFF	128K	DDR3B_CONFIG	Reserved
2140 0100	2140 01FF	00 2140 0100	00 2140 01FF	256	HyperLink1_CONFIG	Reserved
22E0 0000	22E0 FFFF	00 22E0 0000	00 22E0 FFFF	64K	VCP2_E_DATA	Reserved
22F0 0000	22F0 FFFF	00 22F0 0000	00 22F0 FFFF	64K	VCP2_F_DATA	Reserved
2300 0000	2300 FFFF	00 2300 0000	00 2300 FFFF	64K	VCP2_G_DATA	Reserved
2310 0000	2310 FFFF	00 2310 0000	00 2310 FFFF	64K	VCP2_H_DATA	Reserved
2320 0000	2324 FFFF	00 2320 0000	00 2324 FFFF	384K	TAC_BEI	Reserved
23A0 0000	23BF FFFF	00 23A0 0000	00 23BF FFFF	2M	QM Slave	Reserved
23C0 0000	23FF FFFF	00 23C0 0000	00 23FF FFFF	4M	RAC_A Data (FEI) (BCR)	Reserved
2800 0000	2FFF FFFF	00 2800 0000	00 2FFF FFFF	128M	HyperLink1_DATA	Reserved
3000 0000	33FF FFFF	00 3000 0000	00 33FF FFFF	64M	EMIF16 CS2 Data	RAC_A Data (3320 0000-335F FFFF)
3400 0000	37FF FFFF	00 3400 0000	00 37FF FFFF	64M	EMIF16 CS3 Data	QMSS_SLV (3400 0000 -341F FFFF), TAC DATA (34C0 0000 - 34C4 FFFF)
3800 0000	3BFF FFFF	00 3800 0000	00 3BFF FFFF	64M	EMIF16 CS4 Data	Reserved
3C00 0000	3FFF FFFF	00 3C00 0000	00 3FFF FFFF	64M	EMIF16 CS5 Data	Reserved
5000 0000	5FFF FFFF	00 5000 0000	00 5FFF FFFF	256M	PCIE DATA	SRIO Data
6000 0000	7FFF FFFF	00 6000 0000	00 7FFF FFFF	512M	DDR3B_DATA	PCIE DATA (6000 0000 to 6FFF FFFF), Rest is reserved
8000 0000	FFFF FFFF	08 8000 0000	08 FFFF FFFF	2G	DDR3A_DATA	DDR3 Data
		08 0000 0000	08 7FFF FFFF	2G	DDR3A_DATA	Reserved
		09 0000 0000	09 FFFF FFFF	4G	DDR3A_DATA	Reserved

1.5 Interrupts and EDMA Events

The C66x CorePacs, ARM CorePac, EDMA3 CCs, and HyperLink are responsible for handling all the events in KeyStone I and KeyStone II devices. Primary events are those that are directly connected to the masters that handle them. Secondary events are those that are routed through interrupt controllers to the masters that handle them. The interrupt controllers consist of simple combinational logic to provide additional events to:

- C66x CorePacs
- ARM CorePac
- EDMA3 Channel Controllers
- HyperLink bus

The following are some high-level changes in interrupt and Enhanced Direct Memory Access (EDMA) events when migrating from KeyStone I to KeyStone II devices:

- INTC0 provides 20 Broadcast events and 18 secondary events to each C66x CorePac(0 - 3).
- INTC1 (Available on TCI6636K2H and TCI6638K2K)provides 20 Broadcast events and 18 secondary events to each C66x CorePac(4 - 7).
- INTC2 provides 8 events each to HyperLink0/1 and EDMA3 CC0/2/3/4, respectively, 20 events to EDMA3 CC1 and 36 events to ARM CorePac INTC (GIC).
- All C66x CorePac primary events are also routed as secondary events through INTC 0/1.

Figure 2 (KeyStone I(TMS320TCI6614) Interrupt topology) and Figure 3 (KeyStone II (TCI6638K2K) Interrupt topology) provide a good visual comparison of KeyStone I and KeyStone II interrupt architecture. For more details about the Interrupt/EDMA events pertaining to individual KeyStone I and KeyStone II devices, see the device-specific data manuals.

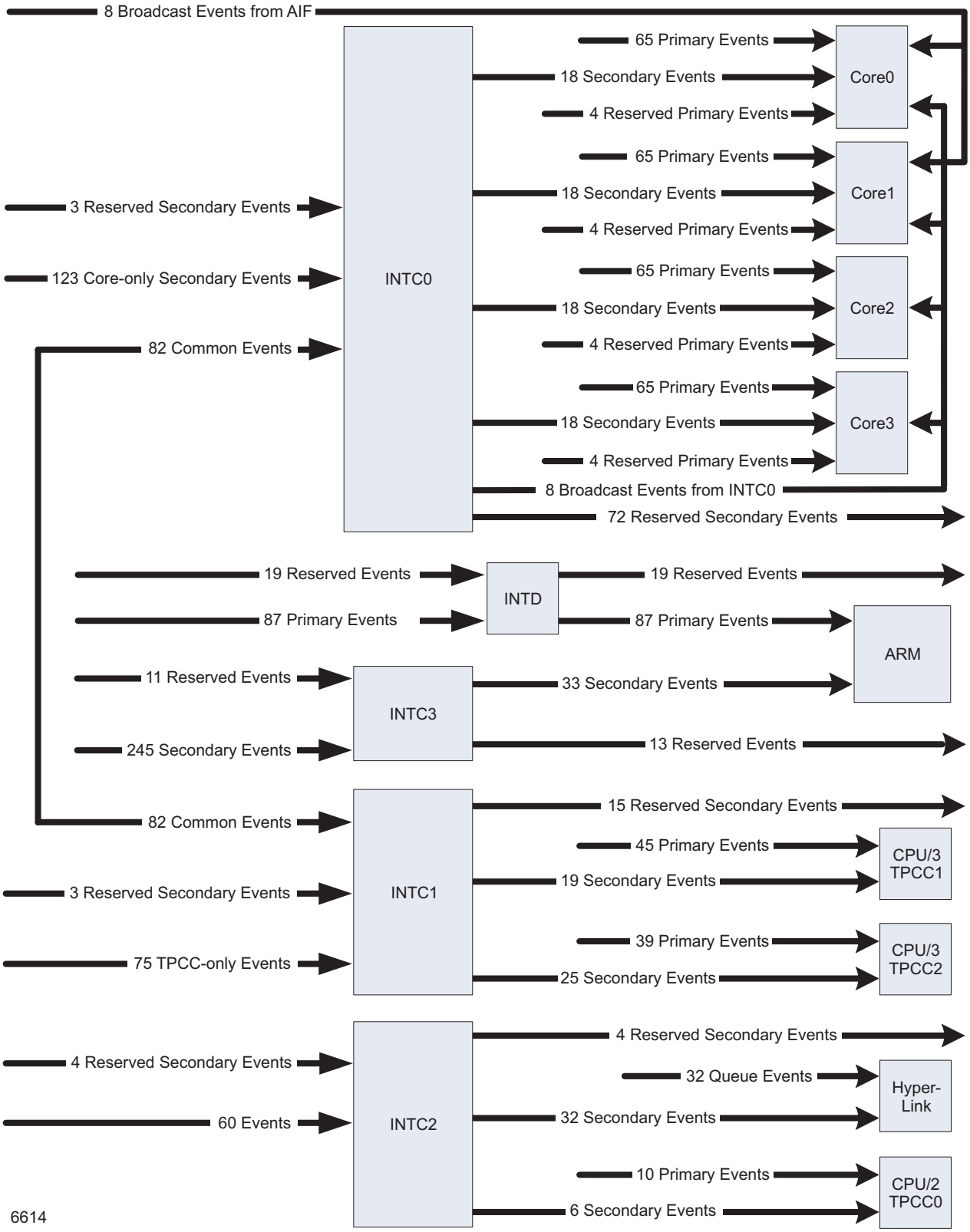

Figure 2. KeyStone I (TMS320TCI6614) Interrupt Topology

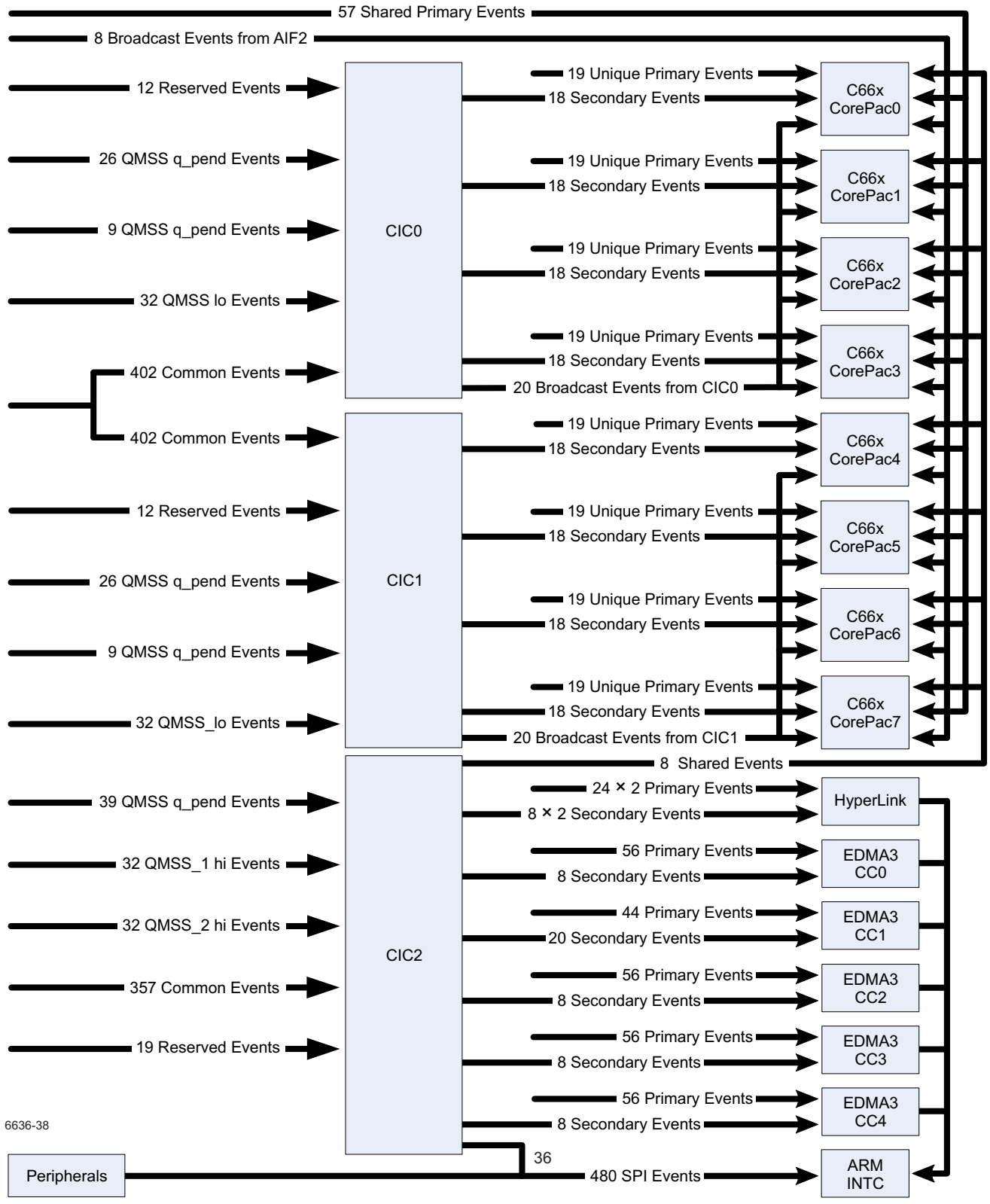

Figure 3. KeyStone II (TCI6638K2K) Interrupt Topology

KeyStone I devices, Table 4 shows the events interconnection matrix (system IP-wise) between the system IPs to the INTCs, C66x CorePacs (COREPACx), EDMA CCs, and HyperLink. For KeyStone II devices, Table 5 shows the events interconnection matrix (system IP-wise) between the system IPs to the INTCs, CorePacs, EDMA CCs, and HyperLink.

From these two tables (system IP-wise), the newly added events in KeyStone II devices can be determined. For exact information about interrupt/EDMA event numbers for individual KeyStone I and KeyStone II devices, see the device-specific data manuals.

Table 4. KeyStone I (TMS320TCI6614) Events Interconnection Matrix

Interrupt Name	ARM SS	INTC0	INTC1	INTC2	INTC3	COREPAC0	COREPAC1	COREPAC2	COREPAC3	Hyper Link	EDMA0	EDMA1	EDMA2	Notes
AIF2														
alarm_intr		1	1											
error_intr		1	1											
cppi_starve_intr		1	1											
aif_atevt[1:0]					2	2	2	2	2		2	2		aif_atevt[1:0] is connected to TPCC0 in TMS320TCI6614/12 and TPCC1 in TMS320TCI6616/18
aif_atevt[7:2]					6	6	6	6	6			6		
aif_intd					1									Combined event for AIF_EVT0, AIF_EVT1 and AIF_EVT Starvation. Applicable only in TMS320TCI6614/12 devices
RAC[2]														
rac_to_dsp_intr0[a,b]						2						2		
rac_to_dsp_intr1[a,b]							2					2		
rac_to_dsp_intr2[a,b]								2				2		
rac_to_dsp_intr3[a,b]									2			2		
rac_trace_gccp[1:0][2] / Debug		4										4		
TAC														
tac_intd_intr		1										1		
sgcpTevent[1:0] / Debug		2										2		
FFTC[3]														
fttca_intd_intr[3:0]		4	4		4									3 FFTCs in TMS320TCI6618, 2 FFTCs in TMS320TCI6612/14/16
fttcb_intd_intr[3:0]		4	4		4									
fttcc_intd_intr[3:0]		4	4											
VCP[4]														
vcp_revt[3:0]		4											4	
vcp_xevt[3:0]		4											4	
vcp_cpu_error_int		4	4											
TCP_3D[(1)][3]														

(1) In TMS320TCI6618, TCP3D_C Error Event and MPU5_INTD (MPU5_ADDR_ERR_INT and MPU5_PROT_ERR_INT combined) goes as a single input to INTC2

Table 4. KeyStone I (TMS320TCI6614) Events Interconnection Matrix (continued)

Interrupt Name	ARM SS	INTC0	INTC1	INTC2	INTC3	COREPAC0	COREPAC1	COREPAC2	COREPAC3	Hyper Link	EDMA0	EDMA1	EDMA2	Notes
tcp3d_intd_intr[3]		3	3	1	2									3 TCP3Ds inTMS320TCI6618, 2 TCP3Ds in TMS320TCI6612/14/16
tcp3d_revt[3][1:0]	4	6											6	
TCP_3E														
TCP3E_INTD		1	1											TCP3E is available only in TMS320TCI6616/18
TCP3EREVT		1											1	
TCP3EWEVT		1											1	
BOOTCFG[2]														
addr_err_intr					1									
prot_err_intr		1	1		1									
MPU[3]**[8]**														
addr_err_intr[8]		8	8		8									8 MPUs in TMS320TCI6614/12, 6 in TMS320TCI6618 and 5 in TMS3206616
prot_err_intr[12]					8									
CPTRACER[18]														
CPT_intr[18]		18	18	18	18									16 CPTs in TMS320TCI6616/18, 18 CPTs in TMS320TCI6614/12
GPIO [32]														
gpio_intr0				1	1	1						1	1	
gpio_intr1				1	1		1					1	1	
gpio_intr2				1	1			1				1	1	
gpio_intr3				1	1				1			1	1	
gpio_intr[5:4]			2	2	2	2	2	2	2		2			In TMS320TCI6614/12, GPIO 5 & 4 are connected to TPCC0 only and not to CPINTC2.
gpio_intr[15:6]			10	10	10	10	10	10	10					
gpio_intr[31:16]					16									
TIMER64[12]														
timer_tint12[0]						1								12 64 bit Timers in TMS320TCI6614/12, 8 64 bit Timers in TMS320TCI6616/18
timer_tint34[0]						1								
timer_tint12[1]							1							
timer_tint34[1]							1							
timer_tint12[2]								1						
timer_tint34[2]								1						
timer_tint12[3]									1					

(2) BOOTCFG prot_err_intr and addr_err_int are combined inTMS320TCI6616/18. In TMS320TCI6614/12, these events are combined for the GEM and not combined for ARM.
(3) MPU prot_err_intr and addr_err_int are combined in TMS320TCI6616/18. In TMS320TCI6614/12, these events are combined for the GEM and not combined for ARM.

Table 4. KeyStone I (TMS320TCI6614) Events Interconnection Matrix (continued)

Interrupt Name	ARM SS	INTC0	INTC1	INTC2	INTC3	COREPAC0	COREPAC1	COREPAC2	COREPAC3	Hyper Link	EDMA0	EDMA1	EDMA2	Notes
timer_tint34[3]									1					
timer_tint12[4]	1			1		1	1	1	1			1	1	Timers 4,5,6 are connected to TPCC2 in TMS320TCI6616/18 and Timers 9,10,11 are connected to TPCC2 in TMS320TCI6614/12
timer_tint34[4]	1			1		1	1	1	1			1	1	
timer_tint12[5]	1			1		1	1	1	1			1	1	
timer_tint34[5]	1			1		1	1	1	1			1	1	
timer_tint12[6]	1			1		1	1	1	1			1	1	
timer_tint34[6]	1			1		1	1	1	1			1	1	
timer_tint12[7]	1			1		1	1	1	1			1		
timer_tint34[7]	1			1		1	1	1	1			1		
timer_tint12[8]	1													
timer_tint34[8]	1													
timer_tint12[11:9]	3										3		3	
timer_tint34[11:9]	3										3		3	
UART														
intr[1:0]		2			2									1 UART inTMS320TCI6616/18 and 2 UARTs in TMS320TCI6614/12
urxevt[1:0]		2			2								2	
utxevt[1:0]		2			2								2	
I2C														
intr		1			1									
xevt		1			1							1	1	
revt		1			1							1	1	
PCIE														
PCIE_ERR_INT	1	1												
PCIE_PM_INT	1	1												
PCIE_LEGACY[A:D]	4	4												
PCIE_MSI_INT0		1				1								
PCIE_MSI_INT1		1					1							
PCIE_MSI_INT2		1						1						
PCIE_MSI_INT3		1							1					
PCIE_MSI_INT4	1	1				1								
PCIE_MSI_INT5	1	1					1							
PCIE_MSI_INT6	1	1						1						
PCIE_MSI_INT7	1	1							1					
QMSS														
qmss_lo_intr[15:0]					16	16	16	16	16					
qmss_hi_intr[31:0]	32		32			8	8	8	8					

Table 4. KeyStone I (TMS320TCI6614) Events Interconnection Matrix (continued)

Interrupt Name	ARM SS	INTC0	INTC1	INTC2	INTC3	COREPAC0	COREPAC1	COREPAC2	COREPAC3	Hyper Link	EDMA0	EDMA1	EDMA2	Notes
qmss_cdma_intr[1:0]		2	2		2									
NETCP														
mdio_link_intr[1:0]		2	2		2									
mdio_user_intr[1:0]		2	2		2									
misc_intr		1	1		1									
starve_intr		1	1		1									
HYPERLINK														
vusr_intpls	1	1		1										
USIM														
usim_ponirq		1			1									Only applicable for TMS320TCI6614/12
usim_posdmarreq_intd		1			1								1	
usim_posdmawreq_intd		1			1								1	
EMIF16														
EASYNCERR		1	1		1									Only applicable for TMS320TCI6614/12
DDR3														
DDR3_ERR		1		1	1									
SEMAPHORE														
semint0						1						1	1	
semint1							1					1	1	
semint2								1				1	1	
semint3									1			1	1	
semint4					1									Applicable only in TMS320TCI6614/12
semint5					1									
semint6					1									
semint7	1												1	
semerr0			1			1								
semerr1			1				1							
semerr2			1					1						
semerr3			1						1					
semerr4					1									Applicable only in TMS320TCI6614/12
semerr5					1									
semerr6					1									
semerr7	1		1											
MSMC														
dedc_cerror		1	1		1									

Table 4. KeyStone I (TMS320TCI6614) Events Interconnection Matrix (continued)

Interrupt Name	ARM SS	INTC0	INTC1	INTC2	INTC3	COREPAC0	COREPAC1	COREPAC2	COREPAC3	Hyper Link	EDMA0	EDMA1	EDMA2	Notes
dedc_nc_error		1	1		1									
scrub_nc_error		1	1		1									
scrub_cerror		1	1		1									
mpf_error0			1		1	1								
mpf_error1			1		1		1							
mpf_error2			1		1			1						
mpf_error3			1		1				1					
mpf_error [15:4]		12	12		12									
BCP														
BCP_ERROR0		1			1	1								In TMS320TCI6618, BCP_ERROR0-3 is input to INTC0. In TMS320TCI6614/12, BCP_ERROR0-3 is input to INTC3 and to CorePac0-3
BCP_ERROR1		1			1		1							
BCP_ERROR2		1			1			1						
BCP_ERROR3		1			1				1					
SRIO SS														
srio_intdst[1:0]		2	2		2							2		In TMS320TCI6614/12, SRIO INTDST 0-1 are directly connected to TPCC1
srio_intdst[15:2]		14	14		14									
srio_intdst16			1			1								
srio_intdst17			1				1							
srio_intdst18			1					1						
srio_intdst19			1						1					
srio_intdst20	1		1			1								
srio_intdst21	1		1				1							
srio_intdst22	1		1					1						
srio_intdst23	1		1						1					
srio_starve_intr		1	1		1									
SEC_CTL and KEY MGR														
KEYMGRINT1		1												
KEYMGRINT_A					1									
KEYMGRINT_B					1									
SECCTLINT		1			1									
SPI														
int_req[1:0]		2			2							2		
dma_req[1:0]		2			2							2		
PSC														
ALLINT		1			1									

Table 4. KeyStone I (TMS320TCI6614) Events Interconnection Matrix (continued)

Interrupt Name	ARM SS	INTC0	INTC1	INTC2	INTC3	COREPAC0	COREPAC1	COREPAC2	COREPAC3	Hyper Link	EDMA0	EDMA1	EDMA2	Notes
SMART REFLEX														
smartreflex_intr[3:0]		4			4									
vpnosmpsack_intr		1			1									
vpeqvalue_intr		1			1									
vpmaxvdd_intr		1			1									
vpminvdd_intr		1			1									
vpinidle_intr		1			1									
vpoppchangedone_intr		1			1									
vcon_smpserr_int		1			1									
smpsack_intr				1	1									
DFT SS														
dft_pbist_cpu_int		1	1		1									
COREPAC TETB[0]														
half_full			1	1	1	1								
full			1	1	1	1								
acq_comp_intr			1	1	1	1								
ovf_intr					1	1								
uflow_intr					1	1								
COREPAC TETB[1]														
half_full			1	1	1		1							
full			1	1	1		1							
acq_comp_intr			1	1	1		1							
ovf_intr					1		1							
uflow_intr					1		1							
COREPAC TETB[2]														
half_full			1	1	1			1						
full			1	1	1			1						
acq_comp_intr			1	1	1			1						
ovf_intr					1			1						
uflow_intr					1			1						
COREPAC TETB[3]														
half_full			1	1	1				1					
full			1	1	1				1					
acq_comp_intr			1	1	1				1					
ovf_intr					1				1					
uflow_intr					1				1					

Table 4. KeyStone I (TMS320TCI6614) Events Interconnection Matrix (continued)

Interrupt Name	ARM SS	INTC0	INTC1	INTC2	INTC3	COREPAC0	COREPAC1	COREPAC2	COREPAC3	Hyper Link	EDMA0	EDMA1	EDMA2	Notes
DEBUG_SS (STM)														
half_full		1	1	1	1									
full		1	1	1	1									
acq_comp_intr		1	1	1	1									
ovf_intr		1			1									
uflow_intr		1			1									
ARM_ETB														
ARM_ETBFULLINT				1	1									Applicable only in TMS320TCI6614/12
ARM_ETBACQINT				1	1									
IPC														
IPCGR0						1								
IPCGR1							1							
IPCGR2								1						
IPCGR3									1					
IPCGRH	1													
RSTMUX														
NMI8	1													
QMSS QUEUE PENDING														
netcp[31:22]		10												
QM_INT_TXQ_ PEND_[657:650]	8													
QM_INT_PASS_TXQ_ PEND_[671:670]	2													
Que_Pending_[864:895]										32				
EDMA0														
edma0_tpcc_intg		1			1									
edma0_tpcc_int[1:0]		2												
edma0_tpcc_int[2]	1	1												
edma0_tpcc_int[3]		1			1									
edma0__tpcc_int[5:4]		2												
edma0__tpcc_int[6]	1	1												
edma0__tpcc_int[7]		1			1									
edma0__tpcc_errint		1			1									
edma0__tpcc_mpint		1			1									
edma0__tptc[1:0]_errint		2			2									
EDMA1														

Table 4. KeyStone I (TMS320TCI6614) Events Interconnection Matrix (continued)

Interrupt Name	ARM SS	INTC0	INTC1	INTC2	INTC3	COREPAC0	COREPAC1	COREPAC2	COREPAC3	Hyper Link	EDMA0	EDMA1	EDMA2	Notes
edma1__tpcc_intg_po		1			1									
edma1__tpcc_int_po[1:0]		2												
edma1__tpcc_int_po[2]	1	1												
edma1__tpcc_int_po[3]		1			1									
edma1__tpcc_int_po[5:4]		2												
edma1__tpcc_int_po[6]	1	1												
edma1__tpcc_int_po[7]		1			1									
edma1__tpcc_errint_po		1			1									
edma1__tpcc_mpint_po		1			1									
edma1__tptc[3:0]_erint_po		4			4									
EDMA2														
edma2__tpcc_intg_po		1			1									
edma2__tpcc_int_po[1:0]		2												
edma2__tpcc_int_po[2]	1	1												
edma2__tpcc_int_po[3]		1			1									
edma2__tpcc_int_po[5:4]		2												
edma2__tpcc_int_po[6]	1	1												
edma2__tpcc_int_po[7]		1			1									
edma2__tpcc_errint_po		1			1									
edma2__tpcc_mpint_po		1			1									
edma2__tptc[3:0]_erint_po		4			4									
EDMA AET														
aetmux_edma_0						1	1	1	1					
aetmux_edma_1						1	1	1	1					
aetmux_edma_2						1	1	1	1					
CPINTC0														
host_intr						26	26	26	26					
CPINTC1														
host_intr												19	25	For TMS320TCI6616/18, 22 events come from CPINTC1. For TMS320TCI6614/12 19 events come from CPINTC1.
CPINTC2														
host_intr										32	6			
CPINTC3														
host_intr	33													

Table 5. KeyStone II (TCI6638K2K) Events Interconnection Matrix

Interrupt Name	GIC	INTC0	INTC1	INTC2	CORE PAC0	CORE PAC1	CORE PAC2	CORE PAC3	CORE PAC4	CORE PAC5	CORE PAC6	CORE PAC7	Hyper Link0	Hyper Link1	EDMA0	EDMA1	EDMA2	EDMA3	EDMA4
AIF2																			
cppi_starve_intr		1	1	1															
aif_atevt[7:0]	8			8	8	8	8	8	8	8	8	8			8	8			8
aif_atevt[12:8]		5	5	5															
aif_atevt[15:13]		3	3	3															
aif_atevt[23:16]	8	8	8																8
aif_intd_intr		1	1	1															
RAC[4]																			
raca_to_dsp_intr				1	1	1	1	1	1	1	1	1					1		
racb_to_dsp_intr				1	1	1	1	1	1	1	1	1					1		
racc_to_dsp_intr				1	1	1	1	1	1	1	1	1					1		
racd_to_dsp_intr				1	1	1	1	1	1	1	1	1					1		
rac_trace_gccp[1:0][4] / Debug		8	8	8															
TAC[2]																			
tac_intd_intr[2]	2	2	2														2		
sgcpTevent[1:0][2] / Debug		4	4														4		
FFTC[6]																			
fftca_intd_intr[3:0]		4	4	4															
fftcb_intd_intr[3:0]		4	4	4															
fftcc_intd_intr[3:0]		4	4	4															
fftcd_intd_intr[3:0]		4	4	4															
fftce_intd_intr[3:0]		4	4	4															
fftcf_intd_intr[3:0]		4	4	4															
VCP[8]																			
vcp_revt[3:0]		4	4	4													4	4	
vcp_xevt[3:0]		4	4	4													4	4	
vcp_revt[7:4]		4	4	4														4	
vcp_xevt[7:4]		4	4	4														4	
vcp_cpu_error_int[8]		8	8	8															
TCP[4]																			
tcp3d_intd_intr[4]		4	4	4															
tcp3d_revt[4][1:0]		8	8	8													4	8	
BOOTCFG																			
prot_err_intr/addr_err_intr		1	1	1															
MPU[12]																			

Table 5. KeyStone II (TCI6638K2K) Events Interconnection Matrix (continued)

Interrupt Name	GIC	INTC0	INTC1	INTC2	CORE PAC0	CORE PAC1	CORE PAC2	CORE PAC3	CORE PAC4	CORE PAC5	CORE PAC6	CORE PAC7	Hyper Link0	Hyper Link1	EDMA0	EDMA1	EDMA2	EDMA3	EDMA4
prot_err_intr[12]/addr_ err_intr[12]		12	12	12															
CPTRACER[32]																			
CPT_intr[32]		32	32	32															
GPIO [32]																			
gpio_intr0	1			1	1								1	1	1	1	1		
gpio_intr1	1			1		1							1	1	1	1	1		
gpio_intr2	1			1			1						1	1	1	1	1		
gpio_intr3	1			1				1					1	1	1	1	1		
gpio_intr4	1			1					1				1	1	1	1	1		
gpio_intr5	1			1						1			1	1	1	1	1		
gpio_intr6	1			1							1		1	1	1	1	1		
gpio_intr7	1			1								1	1	1	1	1	1		
gpio_intr[12:8]	5			5	5	5	5	5	5	5	5	5			5				
gpio_intr[15:13]	3			3	3	3	3	3	3	3	3	3			3				
gpio_intr[23:16]	8	8	8																8
gpio_intr[31:24]	8	8	8																
TIMER64[20]																			
timer_tint12[0]	1	1	1		1										1				
timer_tint34[0]	1	1	1		1										1				
timer_tint12[1]	1	1	1			1									1				
timer_tint34[1]	1	1	1			1									1				
timer_tint12[2]	1	1	1				1								1				
timer_tint34[2]	1	1	1				1								1				
timer_tint12[3]	1	1	1					1							1				
timer_tint34[3]	1	1	1					1							1				
timer_tint12[4]	1	1	1						1						1				
timer_tint34[4]	1	1	1						1						1				
timer_tint12[5]	1	1	1							1					1				
timer_tint34[5]	1	1	1							1					1				
timer_tint12[6]	1	1	1								1				1				
timer_tint34[6]	1	1	1								1				1				
timer_tint12[7]	1	1	1									1			1				
timer_tint34[7]	1	1	1									1			1				
timer_tint12[8]	1			1	1	1	1	1	1	1	1	1	1	1	1	1			1
timer_tint34[8]	1			1	1	1	1	1	1	1	1	1	1	1	1	1			1

Table 5. KeyStone II (TCI6638K2K) Events Interconnection Matrix (continued)

Interrupt Name	GIC	INTC0	INTC1	INTC2	CORE PAC0	CORE PAC1	CORE PAC2	CORE PAC3	CORE PAC4	CORE PAC5	CORE PAC6	CORE PAC7	Hyper Link0	Hyper Link1	EDMA0	EDMA1	EDMA2	EDMA3	EDMA4
timer_tint12[11:9]	3			3	3	3	3	3	3	3	3	3	3	3	3	3			
timer_tint34[11:9]	3			3	3	3	3	3	3	3	3	3	3	3	3	3			
timer_tint12[13:12]	2	2	2										2	2	2	2			
timer_tint34[13:12]	2	2	2										2	2	2	2			
timer_tint12[15:14]	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2			2
timer_tint34[15:14]	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2			2
timer_tint12[16]	1	1	1																
timer_tint34[16]	1																		
timer_tint12[17]	1	1	1																
timer_tint34[17]	1																		
timer_tint12[18]	1	1	1																
timer_tint34[18]	1																		
timer_tint12[19]	1	1	1																
timer_tint34[19]	1																		
UART																			
intr	1	1	1																
urxevt	1	1	1														1		
utxevt	1	1	1														1		
intr	1	1	1																
urxevt	1	1	1															1	
utxevt	1	1	1															1	
I2C																			
intr	1	1	1																
xevt	1	1	1														1	1	
revt	1	1	1														1	1	
intr	1	1	1																
xevt	1	1	1															1	
revt	1	1	1															1	
intr	1	1	1																
xevt	1	1	1															1	
revt	1	1	1															1	
PCIE																			
PCIE_LEGACY[A:D]	4	4	4																
PCIE_MSI_INT0	1	1			1														
PCIE_MSI_INT1	1	1				1													
PCIE_MSI_INT2	1	1					1												

Table 5. KeyStone II (TCI6638K2K) Events Interconnection Matrix (continued)

Interrupt Name	GIC	INTC0	INTC1	INTC2	CORE PAC0	CORE PAC1	CORE PAC2	CORE PAC3	CORE PAC4	CORE PAC5	CORE PAC6	CORE PAC7	Hyper Link0	Hyper Link1	EDMA0	EDMA1	EDMA2	EDMA3	EDMA4
PCIE_MSI_INT3	1	1						1											
PCIE_MSI_INT4	1		1						1										
PCIE_MSI_INT5	1		1							1									
PCIE_MSI_INT6	1		1								1								
PCIE_MSI_INT7	1		1									1							
PCIE_ERR_INT	1	1	1																
PCIE_PM_INT	1	1	1																
QMSS																			
qmss1_lo_intr[15:0]	16	16	16																
qmss1_hi_intr[31:0]	32			32	4	4	4	4	4	4	4	4							
qmss1_cdma_intr[1:0]	2	2	2	2															
qmss2_lo_intr[15:0]	16	16	16																
qmss2_hi_intr[31:0]	32			32	4	4	4	4	4	4	4	4							
qmss2_cdma_intr[1:0]	2	2	2	2															
NETCP																			
mdio_link_intr[1:0]	2	2	2	2															
mdio_user_intr[1:0]	2	2	2	2															
misc_intr	1	1	1	1															
starve_intr	1	1	1	1															
XGE																			
mdio_link_intr[1:0]	2	2	2	2															
mdio_user_intr[1:0]	2	2	2	2															
misc_intr	1	1	1	1															
starve_intr	1	1	1	1															
HYPERLINK0																			
vusr_intpls_0	1	1	1	1															
HYPERLINK1																			
vusr_intpls_0	1	1	1	1															
USB																			
INTR[0]	1	1	1																
OABS	1	1	1																
INTR[3:1]	3																		
INTR[11:4]	1	8	8	8															
MISC	1	1	1																
USIM																			
usim_ponirq	1	1	1																

Table 5. KeyStone II (TCI6638K2K) Events Interconnection Matrix (continued)

Interrupt Name	GIC	INTC0	INTC1	INTC2	CORE PAC0	CORE PAC1	CORE PAC2	CORE PAC3	CORE PAC4	CORE PAC5	CORE PAC6	CORE PAC7	Hyper Link0	Hyper Link1	EDMA0	EDMA1	EDMA2	EDMA3	EDMA4
usim_posdmarreq_intd	1	1	1													1			
usim_posdmawreq_intd	1	1	1													1			
EMIF16																			
emif16__mem_error_pls_int		1	1	1															
DDR3B																			
sys_err_intr_req		1	1	1															
DDR3A																			
sys_err_intr_req		1	1	1															
SEMAPHORE																			
semint0				1	1											1			
semint1				1		1										1			
semint2				1			1									1			
semint3				1				1								1			
semint4				1					1							1			
semint5				1						1						1			
semint6				1							1					1			
semint7				1								1				1			
semint8	1			1												1			
semint9	1			1												1			
semint10	1			1												1			
semint11	1			1												1			
semint12		1	1	1												1			
semint13		1	1	1												1			
semerr0				1	1														
semerr1				1		1													
semerr2				1			1												
semerr3				1				1											
semerr4				1					1										
semerr5				1						1									
semerr6				1							1								
semerr7				1								1							
semerr8	1			1															
semerr9	1			1															
semerr10	1			1															
semerr11	1			1															
semerr12		1	1	1															

Table 5. KeyStone II (TCI6638K2K) Events Interconnection Matrix (continued)

Interrupt Name	GIC	INTC0	INTC1	INTC2	CORE PAC0	CORE PAC1	CORE PAC2	CORE PAC3	CORE PAC4	CORE PAC5	CORE PAC6	CORE PAC7	Hyper Link0	Hyper Link1	EDMA0	EDMA1	EDMA2	EDMA3	EDMA4
semerr13		1	1	1															
MSMC																			
dedc_cerror		1	1	1															
dedc_nc_error		1	1	1															
scrub_nc_error		1	1	1															
scrub_cerror		1	1	1															
mpf_error0				1	1														
mpf_error1				1		1													
mpf_error2				1			1												
mpf_error3				1				1											
mpf_error4				1					1										
mpf_error5				1						1									
mpf_error6				1							1								
mpf_error7				1								1							
mpf_error [11:8]	4	4	4	4															
mpf_error [15:12]		4	4	4															
BCP																			
bcp_cpu_event[3:0]		4	4	4													1		
SRIO																			
srio_intdst[7:0]	8	8	8	8													8	8	
srio_intdst[15:0]	8	8	8	8															
srio_intdst16	1	1		1	1														
srio_intdst17	1	1		1		1													
srio_intdst18	1	1		1			1												
srio_intdst19	1	1		1				1											
srio_intdst20	1		1	1					1										
srio_intdst21	1		1	1						1									
srio_intdst22	1		1	1							1								
srio_intdst23	1		1	1								1							
srio_starve_intr	1	1	1	1															
SEC_MGR or KEY MGR																			
violation_intr		1	1	1															
SPI[2]																			
int_req[1:0]	2	2	2													2			
dma_req[1:0]	2	2	2													2	2		
int_req[1:0]	2	2	2															2	

Table 5. KeyStone II (TCI6638K2K) Events Interconnection Matrix (continued)

Interrupt Name	GIC	INTC0	INTC1	INTC2	CORE PAC0	CORE PAC1	CORE PAC2	CORE PAC3	CORE PAC4	CORE PAC5	CORE PAC6	CORE PAC7	Hyper Link0	Hyper Link1	EDMA0	EDMA1	EDMA2	EDMA3	EDMA4
dma_req[1:0]	2	2	2															2	
int_req[1:0]	2	2	2															2	
dma_req[1:0]	2	2	2															2	
PSC																			
ALLINT		1	1	1															
SMART REFLEX 0																			
smartreflex_intr0	1	1	1																
smartreflex_intr1	1	1	1																
smartreflex_intr2	1	1	1																
smartreflex_intr3	1	1	1																
vpnosmpsack_intr	1	1	1																
vpeqvalue_intr	1	1	1																
vpmaxvdd_intr	1	1	1																
vpminvdd_intr	1	1	1																
vpinidle_intr	1	1	1																
vpoppchangedone_intr	1	1	1																
vcon_smpserr_int	1	1	1																
smpsack_intr	1	1	1																
temp_sensor_intr	1	1	1																
timer_intr	1	1	1																
SMART REFLEX 1 [(1)]																			
smartreflex_intr0	1																		
smartreflex_intr1	1																		
smartreflex_intr2	1																		
smartreflex_intr3	1																		
vpnosmpsack_intr	1																		
vpeqvalue_intr	1																		
vpmaxvdd_intr	1																		
vpminvdd_intr	1																		
vpinidle_intr	1																		
vpoppchangedone_intr	1																		
vcon_smpserr_int	1																		
smpsack_intr	1																		
temp_sensor_intr	1																		
timer_intr	1																		

(1) Smart Reflex 1 is available only in Rev1.0 TCI6636K2H and TCI6638K2K devices

Table 5. KeyStone II (TCI6638K2K) Events Interconnection Matrix (continued)

Interrupt Name	GIC	INTC0	INTC1	INTC2	CORE PAC0	CORE PAC1	CORE PAC2	CORE PAC3	CORE PAC4	CORE PAC5	CORE PAC6	CORE PAC7	Hyper Link0	Hyper Link1	EDMA0	EDMA1	EDMA2	EDMA3	EDMA4
DFT SS																			
Idft__dft_pbist_cpu_int		1	1	1															
COREPAC TETB[0]																			
half_full				1	1													1	
full				1	1													1	
acq_comp_intr				1	1														
ovf_intr				1	1														
uflow_intr				1	1														
COREPAC TETB[1]																			
half_full				1		1												1	
full				1		1												1	
acq_comp_intr				1		1													
ovf_intr				1		1													
uflow_intr				1		1													
COREPAC TETB[2]																			
half_full				1			1											1	
full				1			1											1	
acq_comp_intr				1			1												
ovf_intr				1			1												
uflow_intr				1			1												
COREPAC TETB[3]																			
half_full				1				1										1	
full				1				1										1	
acq_comp_intr				1				1											
ovf_intr				1				1											
uflow_intr				1				1											
COREPAC TETB[4]																			
half_full				1					1								1		
full				1					1								1		
acq_comp_intr				1					1										
ovf_intr				1					1										
uflow_intr				1					1										
COREPAC TETB[5]																			
half_full				1						1							1		
full				1						1							1		
acq_comp_intr				1						1									

Table 5. KeyStone II (TCI6638K2K) Events Interconnection Matrix (continued)

Interrupt Name	GIC	INTC0	INTC1	INTC2	CORE PAC0	CORE PAC1	CORE PAC2	CORE PAC3	CORE PAC4	CORE PAC5	CORE PAC6	CORE PAC7	Hyper Link0	Hyper Link1	EDMA0	EDMA1	EDMA2	EDMA3	EDMA4
ovf_intr				1						1									
uflow_intr				1						1									
COREPAC TETB[6]																			
half_full				1							1						1		
full				1							1						1		
acq_comp_intr				1							1								
ovf_intr				1							1								
uflow_intr				1							1								
COREPAC TETB[7]																			
half_full				1								1					1		
full				1								1					1		
acq_comp_intr				1								1							
ovf_intr				1								1							
uflow_intr				1								1							
ARM TRACE																			
davdma_top_intr_req	1	1	1	1															1
aqcmpintr_top_intr_req	1	1	1																
SYSTEM TRACE																			
davdma_top_intr_req	1	1	1	1															1
aqcmpintr_top_intr_req	1	1	1																
IPC																			
IPCGR0				1	1														
IPCGR1				1		1													
IPCGR2				1			1												
IPCGR3				1				1											
IPCGR4				1					1										
IPCGR5				1						1									
IPCGR6				1							1								
IPCGR7				1								1							
IPCGR8	1																		
IPCGR9	1																		
IPCGR10	1																		
IPCGR11	1																		
RSTMUX																			
NMI8	1																		
NMI9	1																		

Table 5. KeyStone II (TCI6638K2K) Events Interconnection Matrix (continued)

Interrupt Name	GIC	INTC0	INTC1	INTC2	CORE PAC0	CORE PAC1	CORE PAC2	CORE PAC3	CORE PAC4	CORE PAC5	CORE PAC6	CORE PAC7	Hyper Link0	Hyper Link1	EDMA0	EDMA1	EDMA2	EDMA3	EDMA4
NMI10	1																		
NMI11	1																		
QMSS QUEUE PENDING																			
netcp[17:12]		6	6	6															
netcp[25:18]	8	8	8	8									8	8					8
netcp[31:26]		6	6	6															
other[145:140]		6	6	6															
other[153:146]		8	8	8															
other[159:154]		6	6	6															
other[47:40]													8	8					
other[39:32]																			8
other[31:0]	32																		
remote[31:16]														16					
remote[15:0]													16						
ARM																			
npmuirq[3:0]	4			4															
ninterrirq	1	1	1	1															
naxierrirq	1	1	1	1															
ncntpnsirq [3:0]																			4
ncntvirq [3:0]																			4
EDMA0																			
edma0__tpcc_intg	1	1	1																
edma0__tpcc_int[7:0]	8	8	8																
edma0__tpcc_errint		1	1	1															
edma0__tpcc_mpint		1	1	1															
edma0__tptc[1:0]_erint		2	2	2															
EDMA1																			
edma1__tpcc_intg	1	1	1																
edma1__tpcc_int[7:0]	8	8	8																
edma1__tpcc_errint		1	1	1															
edma1__tpcc_mpint		1	1	1															
edma1__tptc[3:0]_erint		4	4	4															
EDMA2																			
edma2__tpcc_intg	1	1	1																
edma2__tpcc_int[7:0]	8	8	8																
edma2__tpcc_errint		1	1	1															

Table 5. KeyStone II (TCI6638K2K) Events Interconnection Matrix (continued)

Interrupt Name	GIC	INTC0	INTC1	INTC2	CORE PAC0	CORE PAC1	CORE PAC2	CORE PAC3	CORE PAC4	CORE PAC5	CORE PAC6	CORE PAC7	Hyper Link0	Hyper Link1	EDMA0	EDMA1	EDMA2	EDMA3	EDMA4
edma2__tpcc_mpint		1	1	1															
edma2__tptc[3:0]_erint		4	4	4															
EDMA3																			
edma3__tpcc_intg	1	1	1																
edma3__tpcc_int[7:0]	8	8	8																
edma3__tpcc_errint		1	1	1															
edma3__tpcc_mpint		1	1	1															
edma3__tptc[1:0]_erint		2	2	2															
EDMA4																			
edma4__tpcc_intg	1	1	1																
edma4__tpcc_int[7:0]	8	8	8																
edma4__tpcc_errint		1	1	1															
edma4__tpcc_mpint		1	1	1															
edma4__tptc[1:0]_erint		2	2	2															
EDMA AET																			
aetmux_edma_0_4					1	1	1	1	1	1	1	1							
aetmux_edma_1_3					1	1	1	1	1	1	1	1							
aetmux_edma_2					1	1	1	1	1	1	1	1							
CPINTC2																			
host_intr	32				4	4	4	4	4	4	4	4	8	8	8	20	8	8	8
CPINTC0/1																			
host_intr					38	38	38	38	38	38	38	38							

1.6 Power Domains

Both KeyStone I and KeyStone II devices have several power domains that can be turned on for operation or turned off to minimize power dissipation. The Global Power Sleep Controller (GPSC) is used to control the power gating of various power domains.

Table 6 lists the power domain allocations for both KeyStone I and KeyStone II devices. For more information about the power domains available for individual KeyStone I and KeyStone II devices, see the device-specific data manuals.

Table 6. Power Domain Changes

Domain	Blocks	
	KeyStone I	**KeyStone II (TCI6638K2K)**
0	Most peripheral logic (TeraNet, QMSS, EDMA3, HW SEM, GPIO, I2C, UART, BOOTCFG, TIMER, INTC, USIM, Smart Reflex SS, EMIF16, DDR3 EMIF, VCP2A and HyperLink)(1)	Most peripheral logic (TeraNet, QMSS, EDMA3, HW SEM, GPIO, I2C, UART, BOOTCFG, TIMER, INTC, USIM, USB SS and EMIF16)
1	TETBs and Debug SS	TETBs and Debug SS
2	Network Coprocessor	Network Coprocessor
3	PCIe	PCIe
4	SRIO	SRIO
5	BCP or HyperLink(2)	HyperLink 0
6	ARM subsystem(3)	Smart Reflex Subsystem
7	MSMC RAM	MSMC RAM
8	RAC_A, RAC_B, and TAC	C66x CorePac0, L1/L2 RAMs
9	FFTC_A and FFTC_B	C66x CorePac1, L1/L2 RAMs
10	AIF2	C66x CorePac2, L1/L2 RAMs
11	TCP3d_A	C66x CorePac3, L1/L2 RAMs
12	VCP2_B, VCP2_C, and VCP2_D	C66x CorePac4, L1/L2 RAMs
13	C66x CorePac0, L1/L2 RAMs	C66x CorePac5, L1/L2 RAMs
14	C66x CorePac1, L1/L2 RAMs	C66x CorePac6, L1/L2 RAMs
15	C66x CorePac2, L1/L2 RAMs	C66x CorePac7, L1/L2 RAMs
16	C66x CorePac3, L1/L2 RAMs	DDR3A_EMIF and DDR3B_EMIF
17	TCP3d_B	RAC_A, RAC_B, and TAC
18	BCP, FFTC_C, and TCP3d_C(4)	RAC_C and RAC_D
19	NA	FFTC_A and FFTC_B
20	NA	FFTC_C, FFTC_D, FFTC_E and FFTC_F
21	NA	AIF2
22	NA	TCP3d_A and TCP3d_B
23	NA	TCP3d_C and TCP3d_D
24	NA	VCP2_A, VCP2_B, VCP2_C, and VCP2_D
25	NA	VCP2_E, VCP2_F, VCP2_G, and VCP2_H
26	NA	BCP
27	NA	Reserved
28	NA	HyperLink 1
29	NA	XGE
30	NA	ARM Smart Reflex SS
31	NA	ARM CorePac

(1) Power Domain 0 includes HyperLink only in TMS320TCI6612 and TMS320TCI6614 devices.
(2) Power Domain 5 is for BCP in TMS320TCI6612 and TMS320TCI6614 devices and for HyperLink in TMS320TCI6616 and TMS320TCI6618 devices.
(3) Power Domain 6 is reserved for TMS320TCI6616 and TMS320TCI6618 devices.
(4) Power Domain 18 is applicable only for TMS320TCI6618 device.

1.7 Clock Domains

Clock gating to each logic block is managed by the Local Power Sleep Controllers (LPSCs) of each module. For modules with a dedicated clock or multiple clocks, the LPSC communicates with the PLL controller to enable and disable that module's clock(s) at the source. For modules that share a clock with other modules, the LPSC controls the clock gating.

Table 7 shows the clock domain allocations for both KeyStone I and KeyStone II (TCI6638K2K) devices. For more information about the clock domains available for individual KeyStone I and KeyStone II devices, see the device-specific data manuals.

Table 7. Clock Domain Changes

LPSC Number	Modules	
	KeyStone I	KeyStone II (TCI6638K2K)
0	Shared LPSC for all peripherals other than those listed in this column	Shared LPSC for all peripherals other than those listed in this column
1	SmartReflex	Reserved
2	DDR3 EMIF	USB Subsystem
3	TCP3e(1)	EMIF16
4	VCP2_A	Reserved
5	Debug subsystem and tracers	Debug subsystem and tracers
6	Per-core TETB and system TETB	Per-core TETB and system TETB
7	Packet Accelerator	Packet Accelerator
8	Ethernet SGMIIs	Ethernet SGMIIs
9	Security Accelerator	Security Accelerator
10	PCIe	PCIe
11	SRIO	SRIO
12	HyperLink or BCP(2)	HyperLink 0
13	ARM subsystem reset control(3)	SmartReflex 0
14	MSMC RAM	MSMC RAM
15	RAC_A and RAC_B	C66x CorePac 0
16	TAC	C66x CorePac 1
17	FFTC_A and FFTC_B	C66x CorePac 2
18	AIF2	C66x CorePac 3
19	TCP3d_A	C66x CorePac 4
20	VCP2_B	C66x CorePac 5
21	VCP2_C	C66x CorePac 6
22	VCP2_D	C66x CorePac 7
23	C66x CorePac0 and Timer0	DDR3A_EMIF
24	C66x CorePac1 and Timer1	DDR3B_EMIF
25	C66x CorePac1 RSAs	TAC
26	C66x CorePac2 and Timer2	RAC_A and RAC_B
27	C66x CorePac2 RSAs	RAC_C and RAC_D
28	C66x CorePac3 and Timer3	FFTC_A
29	TCP3d_B	FFTC_B
30	BCP, FFTC_C, and TCP3d_C(4)	FFTC_C
31	NA	FFTC_D
32	NA	FFTC_E
33	NA	FFTC_F

(1) LPSC 3 is mapped to HyperLink in TMS320TCI6612 and TMS320TCI6614 devices.
(2) LPSC 12 is mapped to HyperLink in TMS320TCI6616 and TMS320TCI6618 devices and to BCP in TMS320TCI6612 and TMS320TCI6614 devices.
(3) LPSC 13 is applicable only for TMS320TCI6612 and TMS320TCI6614 devices.
(4) LPSC 30 is reserved for TMS320TCI6612, TMS320TCI6614 and TMS320TCI6616 devices.

Table 7. Clock Domain Changes (continued)

LPSC Number	Modules	
	KeyStone I	KeyStone II (TCI6638K2K)
34	NA	AIF2
35	NA	TCP3d_A
36	NA	TCP3d_B
37	NA	TCP3d_C
38	NA	TCP3d_D
39	NA	VCP2_A
40	NA	VCP2_B
41	NA	VCP2_C
42	NA	VCP2_D
43	NA	VCP2_E
44	NA	VCP2_F
45	NA	VCP2_G
46	NA	VCP2_H
47	NA	BCP
48	NA	Reserved
49	NA	HyperLink 1
50	NA	XGE
51	NA	SmartReflex 1
52	NA	ARM CorePac

1.8 Master IDs

Table 8 shows the master ID changes from KeyStone I to KeyStone II devices. For the master IDs of individual KeyStone I and KeyStone II devices, see the device-specific data manuals.

Table 8. Master ID Changes

Master ID	KeyStone I	KeyStone II (TCI6638K2K)
0	CorePac0	CorePac0
1	CorePac1	CorePac1
2	CorePac2	CorePac2
3	CorePac3	CorePac3
4	ARM_Port1 (1)	CorePac4
5	Reserved	CorePac5
6	Reserved	CorePac6
7	Reserved	CorePac7
8,12	CorePac0 CFG	ARM_CPU0
9,13	CorePac1 CFG	ARM_CPU1
10,14	CorePac2 CFG	ARM_CPU2
11,15	CorePac3 CFG	ARM_CPU3
16	Reserved	CorePac0 CFG
17	Reserved	CorePac1 CFG
18	Reserved	CorePac2 CFG
19	Reserved	CorePac3 CFG
20	EDMA0_TC0 read/write	CorePac4 CFG
21	EDMA0_TC1 read/write	CorePac5 CFG
22	EDMA1_TC0 read/write	CorePac6 CFG

(1) Applicable only for TMS320TCI6612 and TMS320TCI6614 devices.

Table 8. Master ID Changes (continued)

Master ID	KeyStone I	KeyStone II (TCI6638K2K)
23	EDMA1_TC1 read/write	CorePac7 CFG
24	EDMA1_TC2 read	Reserved
25	EDMA1_TC2 write	EDMA0_TC0 read
26	EDMA1_TC3 read	EDMA0_TC0 write
27	EDMA1_TC3 write	EDMA0_TC1 read
28	EDMA2_TC0 read	HyperLink0 master
29	EDMA2_TC0 write	HyperLink1 master
30	EDMA2_TC1 read	SRIO master
31	EDMA2_TC1 write	PCIE master
32	EDMA2_TC2 read	EDMA0_TC1 write
33	EDMA2_TC2 write	EDMA1_TC0 read
34	EDMA2_TC3 read	EDMA1_TC0 write
35	EDMA2_TC3 write	EDMA1_TC1 read
36	Reserved	EDMA1_TC1 write
37	Reserved	EDMA1_TC2 read
38	SRIO PktDMA	EDMA1_TC2 write
39	SRIO PktDMA	EDMA1_TC3 read
40	FFTC_A	EDMA1_TC3 write
41	Reserved	EDMA2_TC0 read
42	FFTC_B	EDMA2_TC0 write
43	Reserved	EDMA2_TC1 read
44	RAC_B_BE0	EDMA2_TC1 write
45	RAC_B_BE1	EDMA2_TC2 read
46	RAC_A_BE0	EDMA2_TC2 write
47	RAC_A_BE1	EDMA2_TC3 read
48	DAP	EDMA2_TC3 write
49	TPCC0	EDMA3_TC0 read
50	TPCC1	EDMA3_TC0 write
51	TPCC2	EDMA3_TC1 read
52	MSMC[2]	MSMC
53	PCIe	EDMA3_TC1_WR
54	SRIO_M	SRIO PktDMA
55	Hyperbridge	SRIO PktDMA
56	PA_SS(QM_SS in Turbo Nyquist and Appleton)	FFTC_A
57		FFTC_B
58		RAC_B_BE0
59		RAC_B_BE1
60	Reserved	RAC_A_BE0
61	Reserved	RAC_A_BE1
62	Reserved	TPCC0
63	Reserved	TPCC1
64	AIF2	TPCC2
65		FFTC_C
66		Reserved
67		FFTC_D
68-71		QM_SEC_MST

(2) The master ID for MSMC is for the transactions initiated by MSMC internally and sent to the DDR.

Table 8. Master ID Changes (continued)

Master ID	KeyStone I	KeyStone II (TCI6638K2K)
72-79	Reserved	AIF2_CDMA
80	Reserved	Reserved
81	Reserved	BCP_DIO0
82	Reserved	BCP_DIO1
83	Reserved	EDMA3_CC_TR
84-87	Reserved	XGE master
88	Reserved	RAC_C_BE0
89	QM PktDMA	RAC_C_BE1
90	QM PktDMA	RAC_D_BE0
91	QM PktDMA	RAC_D_BE1
92-93	QM_second (PA_SS in Turbo Nyquist)	QM2 PktDMA
94	TAC	QM2 PktDMA
95	Reserved	QM2 PktDMA
96-99	Reserved	QM1 PktDMA
100-101	Reserved	Reserved
102	Reserved	BCP PktDMA
103	Reserved	TAC_FEI0
104	Reserved	TAC_FEI1
105	Reserved	FFTC_E
106	Reserved	FFTC_F
107	Reserved	DAP master
108-127	Reserved	Reserved
128	Tracer_L2_0	Reserved
129	Tracer_L2_1	Reserved
130	Tracer_L2_2	Reserved
131	Tracer_L2_3	Reserved
132-135	Reserved	Reserved
136	Tracer_MSMC0	Reserved
137	Tracer_MSMC1	Reserved
138	Tracer_MSMC2	Reserved
139	Tracer_MSMC3	Reserved
140	Tracer_DDRA	Tracer_L2_0
141	Tracer_SM	Tracer_L2_1
142	Tracer_QM_P	Tracer_L2_2
143	Tracer_QM_M	Tracer_L2_3
144	Tracer_CFG	Tracer_L2_4
145	Tracer_RAC	Tracer_L2_5
146	Tracer_RAC_CFG	Tracer_L2_6
147	Tracer_TAC	Tracer_L2_7
148	Tracer_SCR_6p_A[3]	Tracer_MSMC0
149	Tracer_DDR_2[4]	Tracer_MSMC1
150	Reserved	Tracer_MSMC2
151	Reserved	Tracer_MSMC3
152	Reserved	Tracer_DDR3A
153	Reserved	Tracer_SM
154	Reserved	Tracer_QM_CFG1

(3) Applicable only for TMS320TCI6612 and TMS320TCI6614 devices.
(4) Applicable only for TMS320TCI6612 and TMS320TCI6614 devices.

Table 8. Master ID Changes (continued)

Master ID	KeyStone I	KeyStone II (TCI6638K2K)
155	Reserved	Tracer_QM_M
156	Reserved	Tracer_CFG
157	Reserved	Tracer_RAC_FEI
158	Reserved	Tracer_RAC_CFG1
159	Reserved	Tracer_TAC_BE
160	Reserved	Tracer_QM_CFG2
161	Reserved	Tracer_DDR3B
162	Reserved	Tracer_RAC_CFG2
163	Reserved	Tracer_BCR_CFG
164	Reserved	Tracer_TPCC0_4
165	Reserved	Tracer_TPCC1_2_3
166	Reserved	Tracer_INTC
167	Reserved	Tracer_SPI_ROM_EMIF16
168	Reserved	USB master
169	Reserved	EDMA4_TC0 read
170	Reserved	EDMA4_TC0 write
171	Reserved	EDMA4_TC1 read
172	Reserved	EDMA4_TC1 write
173	Reserved	TPCC4
174	Reserved	Tracer_MSMC5
175	Reserved	Tracer_MSMC6
176	Reserved	Tracer_MSMC7
177	Reserved	Tracer_MSMC4
178	Reserved	Reserved
179	Reserved	TAC_FEI2
180-183	Reserved	NETCP master
184-223	Reserved	Reserved
224-255	ARM_Port0[5]	Reserved

[5] Applicable only for TMS320TCI6612 and TMS320TCI6614 devices.

1.9 Privilege IDs

Table 9 shows the privilege ID changes from KeyStone I to KeyStone II devices. For the privilege IDs of individual KeyStone I and KeyStone II devices, see the device-specific data manuals.

Table 9. Privilege ID Changes

PrivID	KeyStone I	KeyStone II (TCI6638K2K)
0	CorePac0	CorePac0
1	CorePac1	CorePac1
2	CorePac2	CorePac2
3	CorePac3	CorePac3
4	AIF	CorePac4
5	TAC	CorePac5
6	RAC	CorePac6
7	FFTC	CorePac7
8	NetCP PktDMA(1)	ARM
9	SRIO PktDMA/SRIO_M	SRIO_M and all PktDMA masters (NetCP, Both QM1 and QM2, FFTC, BCP, AIF, SRIO, USB/XGE)
10	QM PktDMA/QM_second(2)	QM_Second
11	PCIe	PCIe
12	DAP	DAP
13	Reserved	RAC_TAC/BCP_DIO
14	Reserved	HyperLink
15	Reserved	Reserved

(1) privilege ID 8 is for QM_second in TMS320TCI6618 device.
(2) privilege ID 10 is for QM PktDMA/NetCP PktDMA in TMS320TCI6618 device.

1.10 Clock Architecture

In both KeyStone I and KeyStone II devices, the PLL controller along with the Main PLL manages various internal clocks for the SoC including the DSP/ARM cores. From a design point view, there are no changes in either the PLL controller or any of the on-chip PLLs. Some clock-related changes from KeyStone I to KeyStone II are:

- In KeyStone I devices, most of the clock division (CPU/2, CPU/3, CPU/6, an so forth) happens inside the PLL controller. Whereas, in KeyStone II devices, most of the clock division happens within the individual IP modules.
- In KeyStone II devices, two additional on-chip PLLs are added for DDR3B (on TCI6636K2H, TCI6638K2K) and ARM CorePac Subsystem.
- In KeyStone II devices, all the TeraNets operate at CPU/3. Whereas, in KeyStone I devices, there are two main TeraNets: one that operates at CPU/2 and one that operates at CPU/3.
- In KeyStone II devices, the MSMC controller operates at CPU speed. Whereas, in KeyStone I devices, the MSMC controller operates at CPU/2 speed.

For more details about the various clocks used in individual KeyStone I and KeyStone II devices, see the device-specific data manuals. Table 10 shows all the external clock pin-related changes from KeyStone I to KeyStone II devices.

Table 10. Clock Changes

	KeyStone I		KeyStone II (TCI6638K2K)	
	Frequency (MHz)		Frequency (MHz)	
Clock inputs (N|P)	Min	Max	Min	Max
RP1CLK	30.72		30.72	
ALT_CORE_CLK	40	312.5	40	312.5
ARM_CLK	NA		40	312.5
DDR3A_CLK	40	312.5	40	312.5
DDR3B_CLK	NA		40	312.5
PA_CLK	40	312.5	40	312.5
SYS_CLK	122.88, 153.6, 307.2		125, 162.12	
SRIO_SGMII_CLK	156.25, 250, 312.5		125, 162.12	
HYPERLINK_CLK	156.25, 250, 312.5		125, 162.12	
PCIE_CLK	100, 125, 156.25, 250, 312.5		125, 162.12	
XGMII_CLK	NA		125, 162.12	
USB_CLK	NA		100	
TSREFCLK	NA		40, 125	

2 Peripheral-Level Migration

2.1 Peripheral-Level Migration Overview

This section describes the main peripheral-level changes that must be considered when migrating KeyStone I-based system design to a KeyStone II-based system design.

In this migration section, KeyStone I includes all TMS320TCI661x devices and KeyStone II includes all TCI663xK2y devices. Any differences within KeyStone I or KeyStone II devices are explicitly mentioned.

2.2 ARM A15 CorePac Features

The ARM A15 CorePac is a new addition to KeyStone II devices. The ARM CorePac can consist of a dual-core or a quad-core ARM Cortex®-A15 cluster. The following are the main features of the ARM A15 CorePac:

- Quad core ARM Cortex-A15 Symmetric Multi Processing (SMP) capable of operating at up to 1.41312 GHz
- Full implementation of ARMv7-A architecture instruction set
- Integrated Neon and Vector Floating Point (VFP) unit
- Support for security and virtualization extensions
- ARM cluster master port directly connected to MSMC2 for low-latency access to shared MSMC SRAM
- Dedicated ARM interrupt controller (GIC400) to distribute system interrupts to the four ARM cores
- Advanced power management with fine-grained control of individual core power domains, coarse grained cluster level power management and low-power standby modes (WFI/WFE modes)
- Four integrated 64-bit general purpose timers per core, in addition to one dedicated SoC-level watchdog timer (Timer64) per ARM core
- Support for invasive (stop-mode) and non-invasive (tracing, performance monitoring) debug modes and cross triggering for multiprocessor debugging
- 256 KB BOOTROM for A15 cores

2.3 10G Ethernet (XGE) Switch Subsystem

The 10G Ethernet switch subsystem is a new addition to KeyStone II devices. The following are the main features of the 10G Ethernet (XGE) switch subsystem:

- Two 10/100/1G/10G Ethernet ports
- SGMII interface for 10/100/1G and 10GBase-R for 10G
- IEEE 1588 clock synchronization support
  - Annex D, E and F
- Ethernet port reset isolation support
- MACSEC (MAC security) on Ethernet ports
- VLAN support
- Jumbo packet support with max size frame 9600B (9604B with VLAN)
- EMAC loopback and SGMII loopback support
- Support for Audio/Video bridging (P802.1Qav/D6.0)

2.4 USB3 Subsystem

The USB3 subsystem is a new addition to KeyStone II devices. The following are the main features of the USB3 subsystem:

- Single-port dual-mode controller at the following speeds capable of operating either as a host or a device statically:
  - SS (5Gbps)
  - HS (480 Mbps)
  - FS (12 Mbps)
  - LS (1.5 Mbps) in Host mode of operation only
- Integrated DMA controller with extensible Host Controller Interface (xHCI v1.0) support
  - Per core programmable interrupt with programmable event rings
- Integrated USB PHY capable of supporting both USB 3.0 and USB2.0 supported speeds
- Support for 16 transmit and receive endpoints

2.5 EDMA3

The following are the changes in EDMA3 from KeyStone I devices to KeyStone II devices:

- Increased total number of EDMA3 Channel Controllers (CC) from three (KeyStone I) to five (KeyStone II)
  - Total EDMA channels in SoC increased from 144 (KeyStone I) to 320 (KeyStone II)
- Increased total number of EDMA3 Transfer Controllers (TC) from 10 (KeyStone I) to 14 (KeyStone II)
  - In KeyStone II devices, TCs connected to CC0 and CC4 are 256-bit wide and operate at CPU/3 clock. Whereas, in KeyStone I devices, TCs connected to CC0 operate at CPU/2 clock.
  - In KeyStone II devices, all TCs connected to CC1, CC2, and CC3 are 128-bit wide and operate at CPU/3 clock.
- The following are the main reasons for adding more EDMA3 CCs in KeyStone II devices from KeyStone I:
  - Need for larger PaRAM set entries
  - Need for increased number of EDMA 3 channels and sync events to handle additional slave data transfers (VCP2 is increased from 4 to 8)
  - Need for optimized data movement between RAC and DDR3 memory

For more details about KeyStone I or KeyStone II EDMA3, see *Enhanced Direct Memory Access (EDMA3) Controller User's Guide* (SPRUGS5). For EDMA3 events specific to individual KeyStone I and KeyStone II devices, see the device-specific data manuals.

EDMA3 CC3 and CC4 are newly added in KeyStone II devices. For more details about EDMA3 CC or EDMA3 TC modules, see the *Enhanced Direct Memory Access (EDMA3) Controller User's Guide* (SPRUGS5).

The EDMA3 CC and TC changes from KeyStone I to KeyStone II devices are highlighted (bold) in Table 11 and Table 12. The highlighted values should be interpreted as KeyStone II vs. KeyStone I comparison.

Table 11. EDMA3 CC Changes (KeyStone II vs. KeyStone I)

Description	EDMA CC0	EDMA CC4	EDMA CC1	EDMA CC2	EDMA CC3
Number of DMA Channels in channel controller	64 vs. 16	64	64	64	64
Number of QDMA Channels	8	8	8	8	8
Number of interrupt channels	64 vs. 16	64	64	64	64
Number of PaRAM set entries	512 vs. 128	512	512	512	512
Number of event queues	2	2	4	4	2
Number of transfer controllers	2	2	4	4	2
Memory protection existence	Yes	Yes	Yes	Yes	Yes
Number of memory protection and shadow regions	8	8	8	8	8

Table 12. EDMA3 TC Changes (KeyStone II vs. KeyStone I)

	EDMA3 CC0		EDMA3 CC4		EDMA3 CC1				EDMA3 CC2				EDMA3 CC3	
Parameter	TC0	TC1	TC0	TC1	TC0	TC1	TC2	TC3	TC0	TC1	TC2	TC3	TC0	TC1
DATA FIFOSIZE (Bytes)	1024	1024	1024	1024	1024	1024 vs. 512	1024	1024 vs. 512	1024	1024 vs. 512	1024 vs. 512	1024	1024	1024
DATA BUSWIDTH (Bytes)	32	32	32	32	16	16	16	16	16	16	16	16	16	16
DSTREGDEPTH (Entries)	4	4	4	4	4	4	4	4	4	4	4	4	4	4
DBS (Bytes)	128	128	128	128	128 vs. 64	128 vs. 64	128 vs. 64	128 vs. 64	128 vs. 64	128 vs. 64	128 vs. 64	128 vs. 64	64	64

2.6 Network Coprocessor

The following are some high-level changes in NetCP from KeyStone I to KeyStone II devices:

- Four external port Ethernet switch in KeyStone II versus two external port Ethernet switch in KeyStone I
  - TX throughput 2.8gpbs @ 350 MHz
  - RX throughput 4gbps @ 350 MHz
- Packet acceleration functionality is the same for both KeyStone I and KeyStone II devices.
  - KeyStone II devices support 1.5 million packets/sec network processing capability
- KeyStone II SerDes configuration is different from KeyStone I due to the usage of new 28-nm SerDes in KeyStone II.
- Ethernet switch configuration of KeyStone II is expanded for using four ports.
- Memory map of the IP is expanded to support four external ports.
- Four sets of statistics blocks are used for recording events associated with frame traffic, as opposed to two blocks in KeyStone I.

The NetCP on the TCI6630K2L and TCI6631K2L has been enhanced (NetCP 1.5) with the followings:

- Security Acceleration (SA) functionality is the same for both KeyStone I and KeyStone II devices. However, KeyStone II security accelerator integrates two IPSEC/SRTP engines versus one in KeyStone I for increased throughput.

- Max IP datagram support up to 64K
- Provides eight instances of 1st pass Lookup Table (LUT1) accelerator, each with support for up to 256 entries
- Provides 2nd pass lookup table (LUT2) accelerator with support for up to 3K entries
- Stateless firewall support with 512 entries
- NAT support on egress and NAT-T support on ingress
- Hardware IP reassembly (1K contexts total) supporting inner and outer IPv4/IPv6 in any order
- Dedicated Packet DMA, Queue Managers, and memory for local PA traffic (offloads global QMSS for Reassembly and Security Accelerator transactions)
- Statistics support for up to 4096 individual counters
- The SA also supports algorithms such as: F9, Snow3G F8/F9, ZUC F8/F9 /ZUC-MAC

2.7 Time Synchronization

The following are some high-level changes with respect to time synchronization from KeyStone I to KeyStone II devices:

- KeyStone II uses CPTS 1.5, providing better integration for time synchronization compared to KeyStone I, which used CPTS 1.0.
- KeyStone II supports timestamping of IEEE1588 Annex D, E, and F packets by the CPTS block. KeyStone I supported only Annex F sync packets in the CPTS block. Annex D packet timestamping could be supported using Packet Accelerator (PA).
- KeyStone II CPTS integrates a compare register that can be used to provide precise output pulse based on the CPTS reference clock. This output pulse signal is available as a device pin (TSCOMPOUT). This feature was not available in KeyStone I in the CPTS module, but it could be supported using the general purpose timer modules called Timer64.
- KeyStone II CPTS has support for hardware push events that can be used to precisely timestamp external events based of the CPTS reference clock. These events inputs are available as device pins (TSPUSHEVT0/1). This feature was not available in KeyStone I in the CPTS module, but it could be supported using the general purpose timer modules (Timer64) capture feature.
- KeyStone II supports all the same reference clock sources for the CPTS block as in KeyStone I. In addition, KeyStone II supports an external differential clock source (TSCLKp/n).
- From a SyncE support perspective, KeyStone II exports recovered clocks from the four SGMII ports to device pins(TSRXCLKOUT0/1). The recovered clocks could be used by logic external to the device to implement a clock forwarding Synchronous Ethernet solution. KeyStone I did not support exporting of recovered receive clock from ethernet ports.

2.8 Receive Accelerator Coprocessor (RAC)

KeyStone II architecture devices support a RAC Broadcaster (BCR), which performs a selected repetition of write transactions to one to *N* RAC Front End Interfaces. Only write transactions are supported by the RAC BCR and any read transaction will be rejected or acknowledged with a default read return.

The RAC BCR has a slave port connected to the Data TeraNet via a 128-bit VBUSM interface and has N Master ports connected to N RAC Front Interfaces using 64-bit VBUSP interfaces. The RAC BCR is also connected to the configuration TeraNet using a 32-bit configuration VBUSP interface.

The RAC BCR can be used in streaming mode (default mode) or it can be configured such that all but one RAC are in streaming mode (example: Parallel Interference Cancellation use case).

The antenna data from the AIF2 needs to be written to the RAC BCR data memory regions (0 to 7) depending on the master port configuration. The master port's default value at power-up is 0, which means that all RAC connected to the Broadcaster are in a streaming mode as shown in Figure 4.

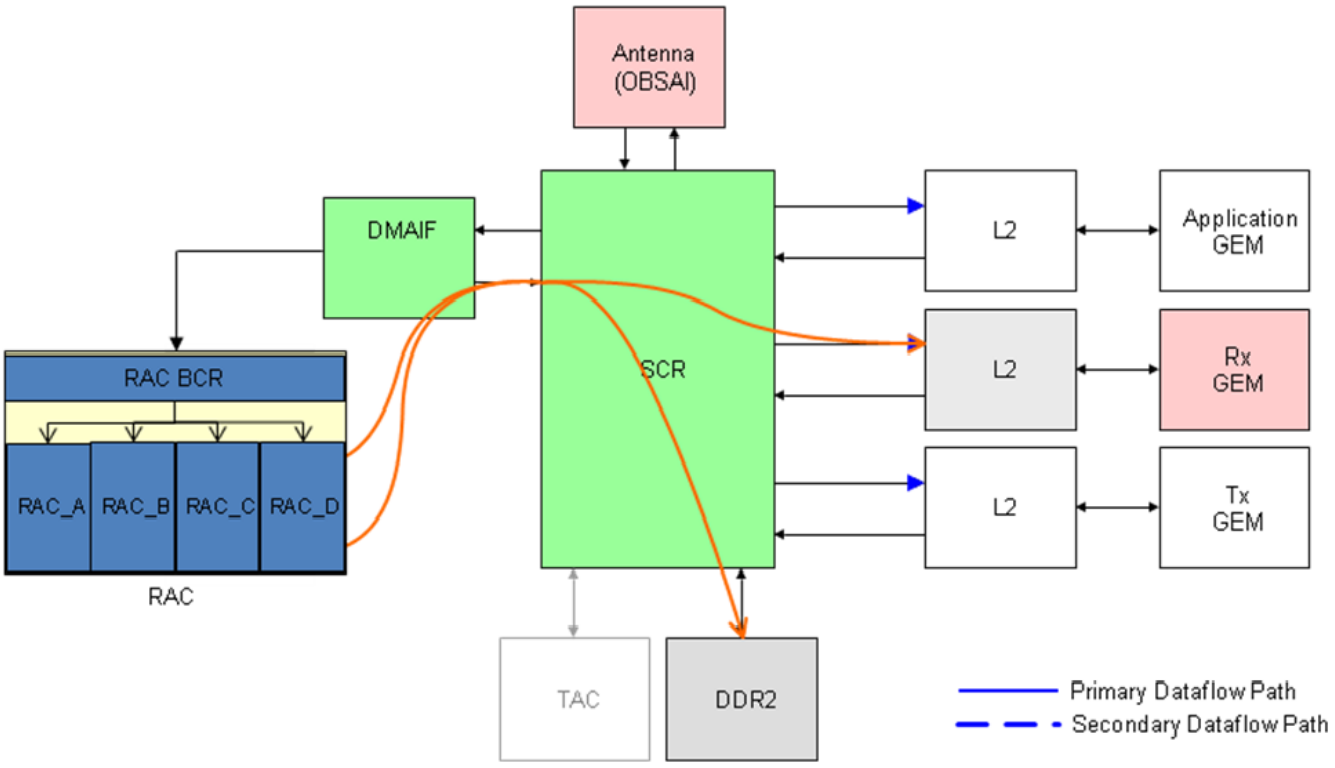

Figure 4. KeyStone II RAC Data Flow

In addition to RAC BCR, the following changes were made to the RAC:

- Single clock domain (DSP/3)
- Increased memory space in datapath to accommodate the speed increase from DSP/4 to DSP/3
- Removal of read access for Front End
- Back End Interrupt Registers modification
- Added RAC Back End IQ Swap Register

2.9 Transmit Accelerator Coprocessor

KeyStone II architecture devices support a Transmit Accelerator (TAC) with enhanced capabilities over those of the TAC in KeyStone I architecture devices. The TAC on KeyStone II devices will be referred to as TAC2.1. The following enhancements to TAC are included in the TAC2.1:

- Increase in channel capacity due to
  - Increase in number of spreader group coprocessors from two to six.
  - Increase in number of front ends from one to three.
- Increase in capacity of signature based channels from 128 to 1536.
- Increase in capacity of signatures across signature based channels from 1536 to 9216.
- Native support for Virtual Antenna Mapping without having to use beam-forming message handlers and dummy spreaders.
- Support for gain compensation for Virtual Antenna Mapping.
- Support for beam-forming weight update for HS-PDSCH channels of HSDPA sets performed on a group basis rather than on a channel-by-channel basis.
- Support for diversity-mode change on a sub-frame basis for E-AGCH channels.

- Support for DTX of non-diversity sub-frames for E-AGCH, HS-SCCH and HS-PDSCH channels when beam forming is employed on diversity transmitted channels (such as, 2xN beam forming diversity mode).

The Transmit Accelerator Functional Library (TAC FL) for KeyStone II architecture devices facilitates the use of all of the enhanced capabilities of TAC2.1 by Application software. The Transmit Accelerator Functional Library Interface specification document provides the details for use and integration of TAC FL into Application software.

A high-level description of the API changes is as follows:

- TAC_hsdpaSetupPrepareReq API: Response structure for this was updated to return beam forming group indices.
- TAC_hsdpaReconfigPrepareReq API: Response structure was updated to return beam forming group indices.
- TAC_updateHsPdschGrpWghtsReq API: API name was changed from TAC_updateHsPdschChanWghtsReq because beam-forming weight updates for HS-PDSCH channels are supported on a group basis rather than a channel-by-channel basis.
- HS-PDSCH sub-frame header now includes a beam-forming group index field to support weight updates per group.
- E-AGCH sub-frame header now includes a diversity-mode field to support diversity mode change on sub-frame basis.
- A buffer of size that is a multiple of 4 must be allocated from providing input signatures for HSUPA channels because HSUPA signatures are handled by TAC2 hardware in multiples of 4.
- I/Q components of VAM weights were increased from 8-bit size to 16-bit size.
- New warning type for VAM weight updates has been added.

2.10 DDR3 Memory

KeyStone II devices have two DDR3 subsystems (DDR3A and DDR3B) compared to only one DDR3 subsystem in KeyStone I devices. DDR3A has a 64 bit/72 bit EMIF interface port on the MSMC controller and supports a max of 8 GB of storage. DDR3B also has a 64 bit/72 bit EMIF interface port directly connected to the TeraNet and supports a maximum of 2GB of storage. In KeyStone II devices, one of the main reasons to add the DDR3B interface is to provide a quick and short datapath from system masters like RAC to the DDR3B memory. Figure 5 shows the DDR3 connectivity in KeyStone II devices.

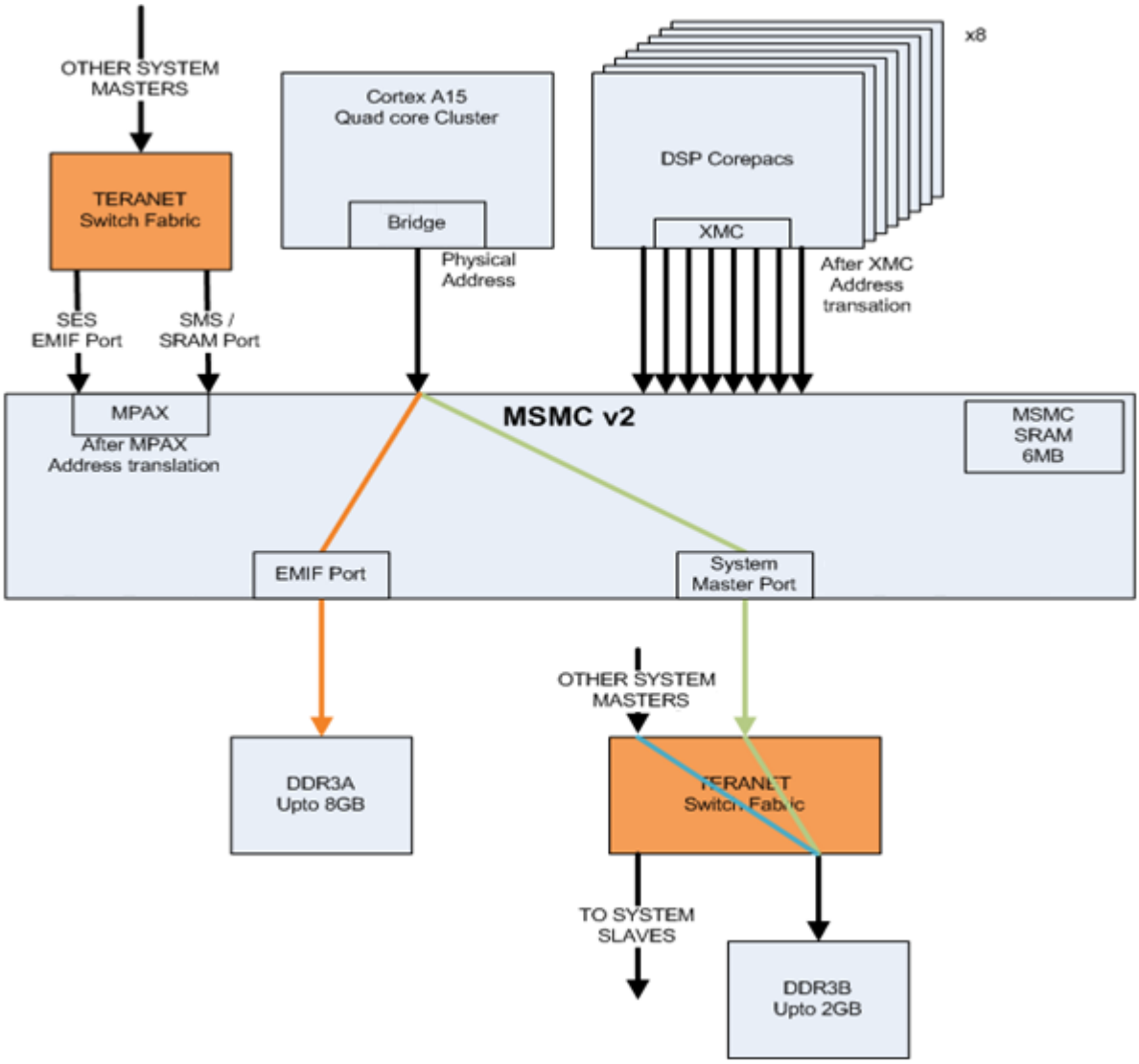

Figure 5. DDR3 Connectivity in KeyStone II Devices

When migrating from KeyStone I to KeyStone II devices, the following are some important points with respect to DDR3 memory:

- The Bridge inside Cortex ARM A15 CorePac, provides logic to remap the physical address from 0x8000_0000 - 0xFFFF_FFFF to 0x08_0000_0000 - 0x08_7FFF_FFFF automatically based on the bootstrap pin ddr3a_map_en.
- SoC System masters other than the ARM or DSP CorePACs can access DDR3B without going through the MSMC. The addresses that they use to access DDR3B are 0x6000_0000 – 0x7FFF_FFFF. This is a 512MB-space for the SoC masters.

- The ARM and DSP CorePACs, see DDR3B at address 0x6000_0000 – 0xFFFF_FFFF, where addresses 0x6000_0000 – 0x7FFF_FFFF are aliased at 0x8000_0000 – 0x9FFF_FFFF. Effectively this is a 2GB-space for the ARM and DSP CorePACs.

2.10.1 ECC

For data integrity, the DDR3 memory controller supports ECC on the data written to or read from the ECC-protected address ranges in memory. Eight-bit ECC is calculated over 64-bit data quanta. ECC can be enabled or disabled by setting or clearing ECC_EN bit in the ECC Control register and the DXEN bit in the DATX8 8 General configuration register. The system must ensure that any bursts accesses starting in the ECC protected region must not cross over into the unprotected region and vice-versa. The controller on some KeyStone II devices supports an additional read-modify-write (RMW) feature. This feature can be enabled by programming RMW_EN = 1 in the ECC Control register.

For memory controllers that do not support RMW, all accesses to ECC protected space must be 64-bit aligned and multiples of 64 bits.

For memory controllers that support RMW, ECC protected-space can be used regardless of the alignment or quanta conditions, if RMW_EN=1. If RMW_EN=0, the controller will again assume the same 64-bit alignment and quanta conditions.

Silicon rev1.0 and 1.1 of the K2K and K2H device families do not support RMW. Other K2Kand K2H silicon revisions and all revisions in the K2L family support RMW.

2.11 On-Chip Standalone RAM (OSR)

The OSR is a new addition to some KeyStone II devices. The OSR is not available on TCI6636K2H and TCI6638K2K devices. The 1-MB OSR is added to the KeyStone II device for:

- QM External Linking RAM
- NetCP1.5 intermediate data buffer
- Intermediate buffering of other data storage

The OSR supported features include:

- SRAM supports ECC with Read-Modify-Write logic
- RTA memory
- Support interrupt for ECC error event
- Support Little and Big-endian modes of operation

OSR does not support any type of cache access, hence this memory space must always be marked as non-cacheable region for both DSP and ARM cores.

2.12 Multicore Navigator

The Multicore Navigator's primary function in KeyStone devices is to coordinate data movement around the device. It also can perform various types of synchronization and notification, as well as job (load) management. For operational and programming details concerning the Navigator, see the *KeyStone Architecture Multicore Navigator User's Guide* (SPRUGR9).

This migration section assumes basic familiarity with the Multicore Navigator as defined for KeyStone I devices.

2.12.1 Features

The major functional components of Multicore Navigator are as follows:

- One hardware queue manager, including:
  - 8192 queues (some dedicated for specific use)
  - 20 descriptor memory regions
- Two linking RAMs (one internal to QMSS, supporting 16K descriptors, and one external (located in L2, MSMC or DDR))

- One infrastructure PKTDMA inside QMSS
- Two PDSPs, each with its own Timer module
- One interrupt distributor (INTD) for generating QMSS interrupts

Multicore Navigator provides the following features in KeyStone I devices:

- Supports up to 512K descriptors
- Packet-based DMA for zero-overhead transfers

For KeyStone II devices, the following enhancements were made to QMSS:

- Two hardware queue managers (QM1, QM2), including:
  - 8192 queues per queue manager
  - 64 descriptor memory regions per queue manager
- Three linking RAMs (one internal to QMSS, supporting 32K descriptors, and one external for QM1 and QM2)
- Two infrastructure PKTDMAs (PKTDMA1 driven by QM1, PKTDMA2 driven by QM2)
- Eight PDSPs (PDSP1 to PDSP8), each with its own dedicated Timer module
- Two interrupt distributors (INTD1, INTD2), which service two pairs of PDSPs each
- A second slave VBUSP for QM2 to optimize push/pop latency
- Supports up to 1,024K descriptors

2.12.2 Functional Block Diagram

Figure 6 shows the architecture of the QMSS in KeyStone II devices.

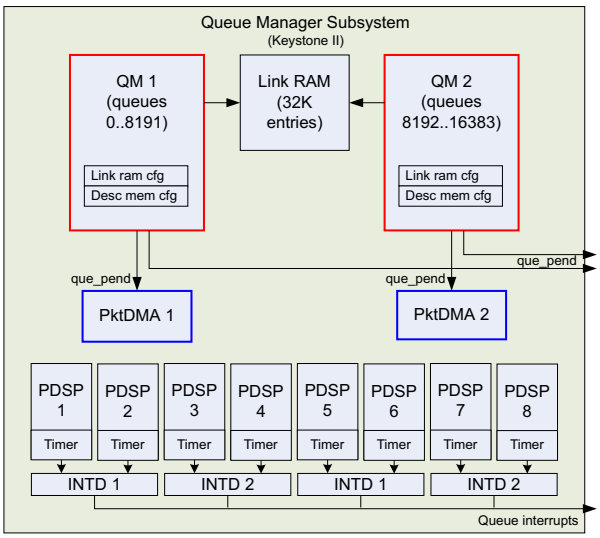

Figure 6. Queue Manager Subsystem for KeyStone II

2.12.3 Migration Overview

When migrating from KeyStone I to KeyStone II, the first thing to consider is the increase in the *number* of Queue Manager Subsystem (QMSS) components over KeyStone I. There are no new components. This increase simply means that there are now multiple instances of the same components, each with its own register set located at a regular offset within the QMSS configuration space. But these components must be used cooperatively in order to be successful.

The most noticeable changes in the QMSS are the addition of a second 8192 queue QM, yielding a total of 16384 queues, a second Infrastructure Packet DMA (PKTDMA), and six more PDSPs.

The one QMSS component that must be used as a shared resource is the internal Linking RAM, because it was doubled in size only. This means that each KeyStone II QM must use the Linking RAM with respect to how the other QM is using it. This creates "usage modes" that are new to KeyStone II.

2.12.4 QMSS Shared Mode

In this usage mode, QM1 and QM2 are programmed to use all QMSS resources as if there is only a single 16K QM. This means that all QM2 register configurations must be identical to QM1 register configurations. Figure 7 shows the internal Link RAM usage and programming for shared mode:

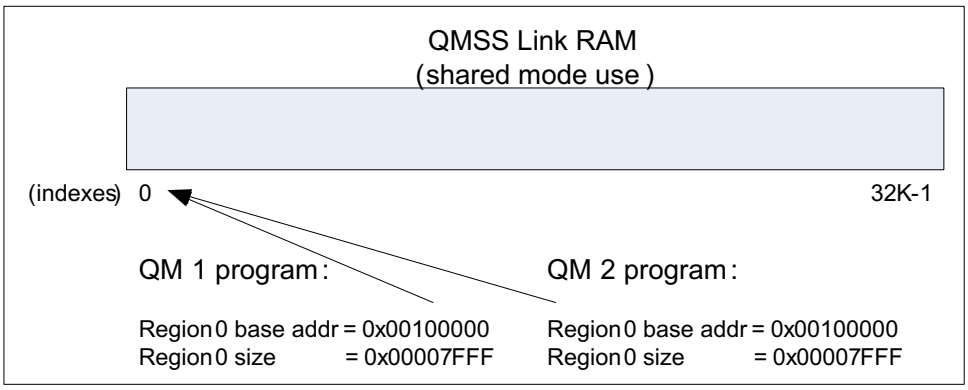

Figure 7. Queue Manager Linking RAM — Shared Mode for KeyStone II

Because each QM in KeyStone II has 64 memory regions for descriptors, this mode allows for a total of 64 distinct memory regions to be configured, because both QMs are sharing the entire Link RAM, and therefore must be configured with the same descriptor memory regions.

The advantage of this mode is its simplicity. Remember that even though the QMs are programmed identically, the other QMSS components probably are not. For example, the second Infrastructure PKTDMA is driven from queue pending signals coming from QM2, and may be configured to use different PDSP firmware resources than other PKTDMAs, which in turn might mean a different INTD configuration as well.

2.12.5 QMSS Split Mode

In this mode, QM1 and QM2 are programmed to use their own resources independently, and each QM uses only a portion of the internal Linking RAM. This means that all QM2 Link RAM and memory region configurations must use separate resources from QM1 or data corruption or Link RAM corruption may result.

Figure 8 shows the internal Link RAM usage and programming for Split Mode.

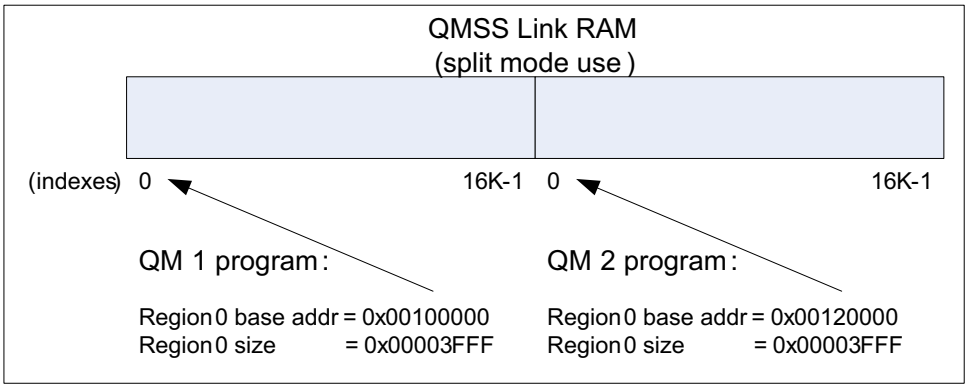

Figure 8. Queue Manager Linking RAM — Split Mode for KeyStone II

Note that the *split point*—the amount of the Link RAM used by each QM—is not strictly a 50/50 split as shown in Figure 8. If QM1 has more descriptors in its memory regions than QM2, its partition can be larger. It is always best to fully utilize the internal Link RAM before using an external Link RAM due to the latency benefit of the internal Link RAM (regardless of mode).

Because each QM in KeyStone II has 64 memory regions for descriptors, this mode allows for a total of 128 distinct memory regions to be configured. Because memory region sizing can be restrictive (due to the power of 2 sizing), 128 memory regions provides much finer granularity on region size and ultimately, memory requirements.

Also, this mode naturally supports having multiple Navigator Clouds (see Section 2.12.10) because one or more “clouds” can be isolated on each queue manager (set of queues) and memory regions. Multiple clouds are easily definable in shared mode as well, and the same cautions apply to both modes. Split mode is a little more flexible in this regard, due to the independence of programming each QM.

2.12.6 Choosing the Mode

So to determine which mode to use? One method would be to start with Shared Mode because its configuration is simpler, and identify reasons why Split Mode would be more beneficial. A few reasons might be:

- More than 64 memory regions are needed
- You want to isolate Navigator Clouds to QMs
- Special load balancing requirements (such as, bus/memory accesses)

Other application-specific requirements for queue/descriptor usage.

2.12.7 Register Use

Programming QMSS registers in KeyStone II is the same as KeyStone I, other than accounting for the aforementioned use modes (and Navigator Clouds discussed below). One other point remains to be clarified however. Because there are now multiple instances of many of the components and it is desirable to index the registers in a similar fashion regardless of which instance is being accessed, all instances are placed at a regular offset from the previous instance. So all you need is the address of the first instance and the offset to each of the following instances. Also, some register regions need to be accessed as if they are a single contiguous region. The Queue Management (push/pop) region is one example, because you would like to access queue 100 and 10,000 with the same logic. In these cases, the instance offsets are placed in contiguous memory so that a single offset calculation can be used to access queues in either QM (starting with the base address of QM1). Normal configuration register offsets are not guaranteed to be contiguous, since they do not need to be.

For more details, see the *KeyStone Architecture Multicore Navigator User's Guide* (SPRUGR9).

2.12.8 Queue Mapping

KeyStone I supports a total of 8192 queues, whereas KeyStone II supports a total of 16384 queues. In both KeyStone I and KeyStone II devices, most of the queues are available for general-purpose use, but some are dedicated for special use, and in some cases, have special hardware functionality associated with them. More details about queue mapping changes from KeyStone I to KeyStone II devices can be found in the *KeyStone Architecture Multicore Navigator User's Guide* (SPRUGR9).

2.12.9 Logical QM Mapping

Logical QM mapping is a PKTDMA feature that affects PKTDMA Rx Flow registers and all descriptors as well. It affects both TX and RX descriptor routing. It was added to allow a PKTDMA to address a QM in another device using HyperLink, though it can be used for other purposes. Note that nothing else in the QMSS (other than the PKTDMAs) has any notion of logical QMs. Everything in the QMSS (including the PDSPs) references physical queue numbers only. If the logical mapping of QMs in a PKTDMA is not straightforward, this can cause confusion when programming the PDSPs and loading FDQs with descriptors to be used by the PKTDMA. Try to keep the logical mapping as simple as possible.

One limitation in defining a logical QM mapping is that the PKTDMA gets its address for the TX queues from the QMn Base Address registers that define the logical QM mappings for the PKTDMA. For KeyStone I, the TX base address always comes from the first of these registers (QM0). For KeyStone II, the PKTDMAs assume a linear mapping of base addresses:

Table 13. Recommended Logical QM Mapping

Logical QMx	Value for Base Address	Description
0	Physical QM1, queue 0 (0x23a80000)	PKTDMAs with TX queues on QM1 use this register
1	Physical QM1, queue 4k (0x23a90000)	
2	Physical QM2, queue 0 (0x23aa0000)	PKTDMAs with TX queues on QM2 use this register
3	Physical QM2, queue 4k (0x23ab0000)	

It is important to note that descriptors that are passed from one PKTDMA to another are handled by each PKTDMA separately. So if the first PKTDMA has a different logical QM mapping than the second, the *queue_manager:queue_number* (qmgr:qnum) fields in the descriptor and RX Flow will mean different things to each PKTDMA, resulting in descriptors being pushed to incorrect queues. PKTDMAs with the same logical mapping are said to be part of the same Navigator Cloud.

2.12.10 Navigator Clouds

A Navigator Cloud is a set of PKTDMAs and descriptors. Neither PKTDMAs nor descriptors address the physical Queue Manager(s) directly, but instead use a *queue_manager:queue_number* (qmgr:qnum) notation and registers to create a logical mapping into the physical Queue Manager(s). All PKTDMAs with the same logical mapping are said to be part of the same Navigator Cloud. A descriptor can be sent to any PKTDMA in the same cloud, but may or may not transfer correctly through PKTDMAs in different clouds. A non-compatible logical qmgr:qnum mapping will cause descriptors to arrive in unexpected queues, potentially causing a memory leak.

It is possible to send a descriptor from one cloud to another, but each qmgr:qnum reference must point to the same physical queues for the PKTDMAs in both clouds. Another way to say this is by example: Let PKTDMA 1 and 2 have the same base addresses programmed for logical QM0 and QM1 in their respective QMn Base Address registers, but their QM2 and QM3 base addresses are different (so by definition they represent different clouds). Any descriptor traveling between them must reference only QM0 and/or QM1 in every descriptor and Rx Flow qmgr:qnum fields. This is especially true if the RX (output) queue for the first PKTDMA is the same physical queue as the TX (input) queue for the second PKTDMA.

2.12.11 PDSPs and INTDs

KeyStone I contains a pair of PDSPs that are serviced by a single INTD. The firmware written for them is such that they run on either the first (odd) or second (even) PDSP, and use INTD resources based on running in the even or odd position. KeyStone II expands this concept by adding three more pairs of PDSPs and a second INTD. The INTDs are configured to service two pair of PDSPs each, as shown in Table 14. Because interrupt resources are limited, conflicts will arise if the same firmware is running on PDSPs that use the same resources of the same INTD. This can be done, of course, if great care is taken to avoid conflicts, but this should only be done as a last resort.

Table 14. Possible PDSP Firmware Loading

PDSP 1	PDSP 2	PDSP 3	PDSP 4	PDSP 5	PDSP 6	PDSP 7	PDSP 8
INTD 1		**INTD 2**		**INTD 1**		**INTD 2**	
Acc 48		Acc 48		Acc 48		Acc 48	
QoS		QoS		QoS		QoS	
Acc 32		Acc 32		Acc 32		Acc 32	
Acc 16		Acc 16		Acc 16		Acc 16	
NRT1	NRT2	NRT1	NRT2	NRT1	NRT2	NRT1	NRT2

2.12.12 Load Balancing

This section discusses load balancing the QMSS subsystem, not load balancing jobs, which is the task of the Navigator Runtime PDSP firmware.

First, the hardware makes accommodations for the second queue manager by adding a second slave VBUSP for it. So push/pops entering QMSS in the configuration region (starting at 0x02a80000) will be diverted to one of the two slave ports. Push/pops to the data (VBUSM) region (starting at 0x23a80000) will be queued, because the VBUSM is capable of handling multiple requests.

Another issue is TX queue locations for the PKTDMAs in KeyStone II. Currently, only the second Infrastructure PKTDMA has its TX queues located in QM2; all others are in QM1. However, most of the other queue-pending signals are located in QM2 (EDMA3, XGE, HyperLink). Depending on the application's usage, one QM may handle considerably more traffic than the other. One way to determine this is to attach a simple logging function to the push/pop routines that counts the push/pops to a pre-defined set of queues per a given measure of time.

If the QMs become grossly imbalanced, there are several ways to adjust the load. Just a few of them are:

- Move RX and RX FDQs to the other QM (for example, if QM1 is loaded with driving TX PKTDMA queues).
- Define (or modify) a Navigator Cloud to use queues from the under-utilized QM.
- Determine (using a logging function) which queue(s) are largely responsible for the imbalance, and move them to the other QM, if possible.
- If moving queues is not feasible, another approach is to send larger packets, which reduces the bus overhead.

Another area of load balancing is in the PDSP and INTD area. With eight PDSPs to choose from, a lot of flexibility is available. The main point is to spread the load across the PDSPs to reduce latency and roughly balance the interrupt generation done by the INTDs.

For example, if accumulation is important and you can use multiple PDSPs for accumulation, then use the 32- or 16-channel accumulator firmware in one PDSP to gain the smallest latency. Both 32-channel (high priority) and 16-channel (low priority) firmware will scan their channels as fast as possible. Only in the 48-channel version will the low priority channels run at 1/16 the rate of the high priority channels. So the number of channels to be monitored, their latency, their interrupt type (broadcast or CGEM specific), and possibly even what QM or Navigator cloud are being used, are all things to be considered.

2.13 SerDes

All KeyStone II IPs like SRIO, SGMII, PCIE, HyperLink, and AIF2, use a 28-nm SerDes, compared to the 40-nm SerDes used in KeyStone I devices. In KeyStone II devices, the SerDes configuration registers are moved out of the BOOTCFG module and they are no longer protected by the kick registers. For more details about SerDes configuration and features, see the device-specific SerDes User's Guides.

2.14 IQNet2

The IQNet 2 (IQN2) peripheral is a new addition to some KeyStone II devices, but is not available on TCI6636K2H and TCI6638K2K devices. The IQN2 subsystem interfaces external I/O into TI DMA systems. It consists of an IQ sample data interface for Digital Front-End (DFE) (AID) module, Antenna Interface CPRI/OBSAI Link (AIL) module, Antenna interface timer (AT) module, one PKTDMA interface, Direct IO (DIO) engines and IQ streaming switch (IQS). The following are the main features of the IQN2 currently supported.

- Transport of baseband antenna streams over AIL physical links. IQN2 use each AIL module like each link in AIF2.
- Transport of baseband antenna streams to an integrated Digital Front-End via AID block. AID and AIL shares some common modules including IQS, DIO, AT and PKTDMA.
- Support the following radio standards transport: WCDMA, LTE, TD-SCDMA on OBSAI, CPRI or direct IQ interface with DFE through AID.
- Support maximum eight radio standards and multiple radio standards works on one AIL lane. The bandwidth of each radio standard can be perfectly separated within one AIL lane or AID.

- Support maximum 16 Ingress + 16 Egress WCDMA AxC channels by DIO.
- Support perfect dual mode operation (DIO + PKTDMA at the same time) for WCDMA and LTE/TD-SCDMA/GSM
- Support up to two AIL lanes
  - AIL supports OBSAI RP3 or CPRI5.0 at a 9.83-Gbps line rate max
  - AIL supports following OBSAI link rates - 2x, 4x, and 8x
  - AIL supports following CPRI link rates - 2x, 4x, 5x, 8x, 10x, and 16x
  - Support AIL PHY reset isolation (same to AIF2)
- Owns micro AT for each AIL, AID and DIO module and each µAT needs to be fully synchronized with macro AT. Macro AT will deliver a master sync signal to each µAT and this signal can be captured via capture register for each timer.
- Integrated Antenna interface Timer (macro AT)
  - 24 System Events, 1 BCN counter, 8 complex RADT (radio timers) to support a maximum of 8 radio standards
  - Supports various timing sync sources - RP1, generic input pins, CPTS or software sync

For more details about IQN2 peripheral and its features, see the *KeyStone II Architecture IQNet2 User's Guide* (SPRUH06).

3 Related Documentation From Texas Instruments

64-Bit Timer (Timer 64) for KeyStone Devices User Guide	SPRUGV5
ARM Bootloader User Guide for KeyStone II Devices	SPRUHJ3
Chip Interrupt Controller (CIC) for KeyStone Devices User Guide	SPRUGW4
Debug and Trace for KeyStone II Devices User Guide	SPRUGZ2
DDR3 Design Requirements for KeyStone Devices	SPRABI1
DDR3 Memory Controller for KeyStone Devices User Guide	SPRUGV8
External Memory Interface (EMIF16) for KeyStone Devices User Guide	SPRUGZ3
Emulation and Trace Headers Technical Reference	SPRU655
Enhanced Direct Memory Access 3 (EDMA3) for KeyStone Devices User Guide	SPRUGS5
General Purpose Input/Output (GPIO) for KeyStone Devices User Guide	SPRUGV1
Gigabit Ethernet (GbE) Switch Subsystem (1 GB) for KeyStone Devices User Guide	SPRUGV9
Hardware Design Guide for KeyStone II Devices	SPRABV0
Inter Integrated Circuit (I^2C) for KeyStone Devices User Guide	SPRUGV3
Interrupt Controller (INTC) for KeyStone Devices User Guide	SPRUGW4
Memory Protection Unit (MPU) for KeyStone Devices User Guide	SPRUGW5
Multicore Navigator for KeyStone Devices User Guide	SPRUGR9
Multicore Shared Memory Controller (MSMC) for KeyStone II Devices User Guide	SPRUHJ6
Network Coprocessor (NETCP) for KeyStone Devices User Guide	SPRUGZ6
Optimizing Application Software on KeyStone Devices	SPRABG8
Packet Accelerator (PA) for KeyStone Devices User Guide	SPRUGS4
Peripheral Component Interconnect Express (PCIe) for KeyStone Devices User Guide	SPRUGS6
Phase Locked Loop (PLL) Controller for KeyStone Devices User Guide	SPRUGV2
Power Sleep Controller (PSC) for KeyStone Devices User Guide	SPRUGV4
Security Accelerator (SA) for KeyStone Devices User Guide	SPRUGY6
Semaphore2 Hardware Module for KeyStone Devices User Guide	SPRUGS3
Serializer/Deserializer (SerDes) for KeyStone II Devices User Guide	SPRUHO3
Serial Peripheral Interface (SPI) for KeyStone Devices User Guide	SPRUGP2
Universal Asynchronous Receiver/Transmitter (UART) for KeyStone Devices User Guide	SPRUGP1
IQN2 for KeyStone II Devices User Guide	SPRUHO6

4 References

- *Enhanced Direct Memory Access (EDMA3) Controller User's Guide* (SPRUGS5)
- *KeyStone Architecture Multicore Navigator User's Guide* (SPRUGR9)
- KeyStone II Architecture IQNet2 User's Guide (SPRUH06)

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (October 2014) to A Revision	Page
• Note 18 was updated for Table 1	6

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265