

PR418  
TMS320VC550x Design 1

**FEATURES:**

- Provides sequenced core and I/O voltages from input voltages from 2.4 V to 5.0 V.
- /RESET delay fixed at 65 ms minimum, 130 ms typical.
- Wide input voltage range covering input voltages above and below the I/O voltage.
- The current draw on the input power supply is minimized by sequencing first the core rail and then the I/O rail.

**IMPORTANT WEB LINKS:**

- Link to the TI power management home page at <http://power.ti.com> then select the TI DSP Solutions link for more information and other reference designs.
- Link to datasheets at:
  - o <http://focus.ti.com/lit/ds/symlink/tps61130.pdf>
  - o <http://focus.ti.com/lit/ds/symlink/tps3103k33.pdf>
- Link to application note SLVA118 <http://focus.ti.com/lit/an/slva118/slva118.pdf> to explore the thermal considerations in using linear regulators.

**THEORY OF OPERATION:**

PR418 is designed around Texas Instrument's TPS61130 combination SEPIC converter and linear regulator (LDO). The circuit uses the SEPIC converter to generate 3.3 V from the input voltage source. The 3.3 V is used for the I/O voltage and to supply the LDO input voltage for the core. The LDO regulates the 3.3 V down to the core voltage of 1.2 or 1.6 V. The reset signal for the DSP is provided by a TPS3103 that monitors both the I/O and core voltages. The TPS3103 will hold /RESET low for about 130 ms once the I/O and core voltages exceed about 90% of their nominal values.

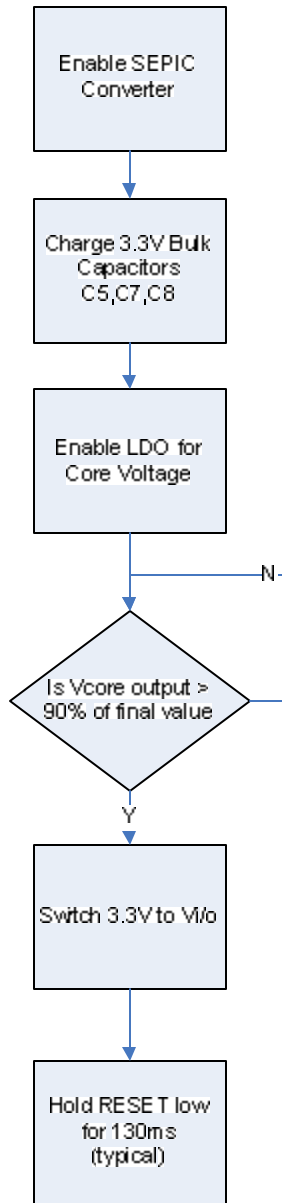
**CIRCUIT LIMITATIONS AND CAPABILITIES:**

The SEPIC converter of the TPS61130 is capable of supplying about 350 mA of current with an input voltage of 2.4 V. The SEPIC converter also supplies current to the LDO for the core voltage, so the sum of the core and I/O currents can not exceed 350 mA. This limit should be checked against the end application. Additionally, the LDO of the TPS61130 has a 200 mA output current limit. This may not be enough current for some 1.6 V, 200Mhz Core configurations and should be checked against the application.

For the current capability at other input voltages, see Figure 1 of the TPS61130 datasheet. From Figure 1, it is possible to operate this circuit with an input voltage as low as 1.8 V;

however, the SEPIC converter will only supply about 250 mA, which may not be enough total current for all DSP configurations.

### POWER UP SEQUENCING:



The circuit will apply the I/O voltage about 7 ms after the Core voltage exceeds 90% of its nominal voltage level. The 7 ms is set by a RC time constant that is created by R6 and C9. This additional delay is used to allow a reduction in peak turn on currents in the core voltage before turning on the I/O voltage. This time can be increased by increasing C9. It is not recommended to decrease this time constant.

The sequencing circuits can be removed if sequencing is not required. Components R6, R7, R8, R9, C9, Q1, and Q2 can all be removed and the I/O voltage supplied directly from the top of C8. The LDO enable can then be tied to the SEPIC's enable pin or simply tied to the input voltage so that it is always enabled. This will not affect the RESET timing. However, the SEPIC converter is only capable of supplying a total of 350 mA of current which includes both the I/O and core currents. If both the I/O and Core voltages are enabled together, there is a risk that the start-up currents may exceed 350 mA and the converter will have difficulties turning on. This condition should be checked in the application if the sequencing is removed.

### IMPLEMENTATION NOTES :

- **Component selection:**

- o If different capacitors are used for C4 and C7 than recommended per the BOM, they must meet the ESR requirements per the datasheet.

### WAVEFORMS:

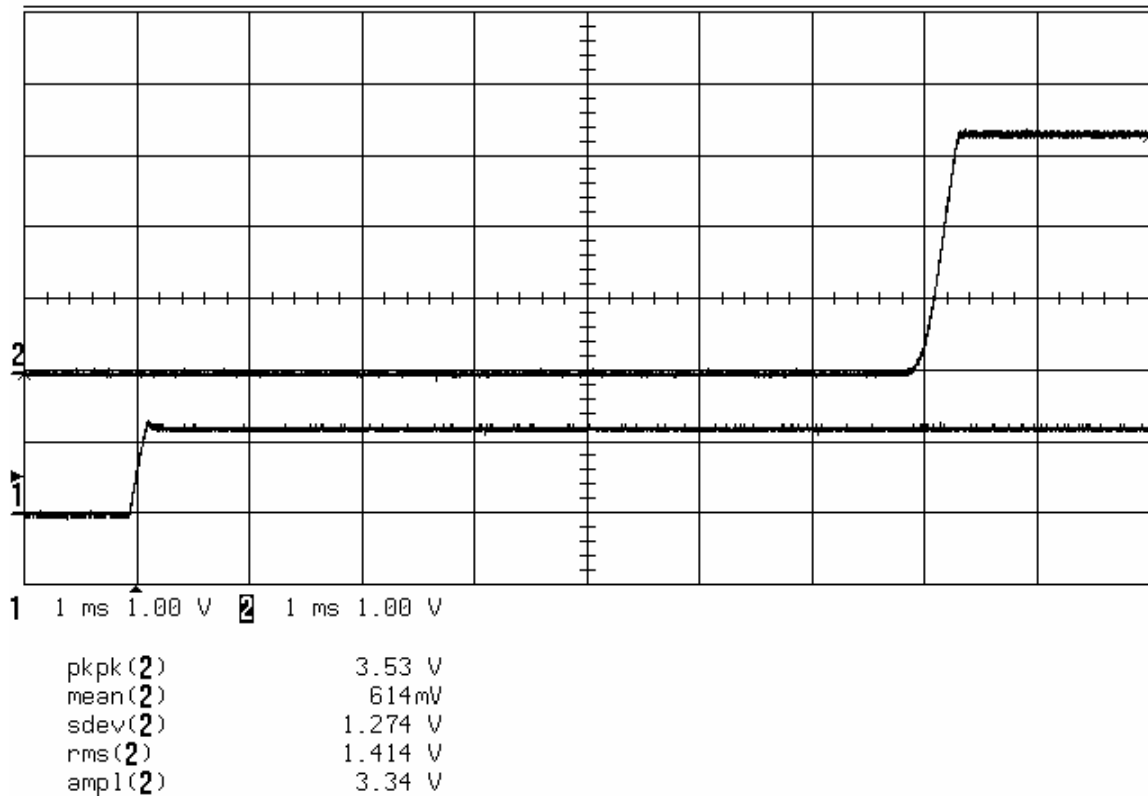
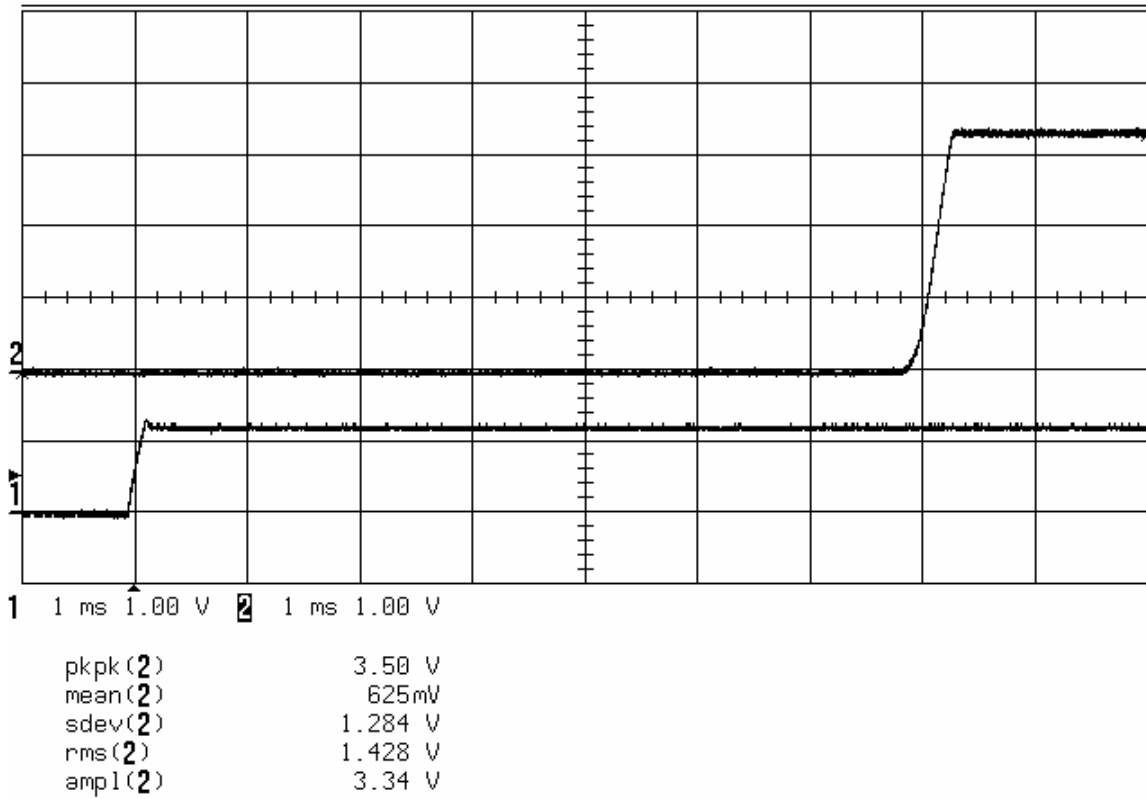


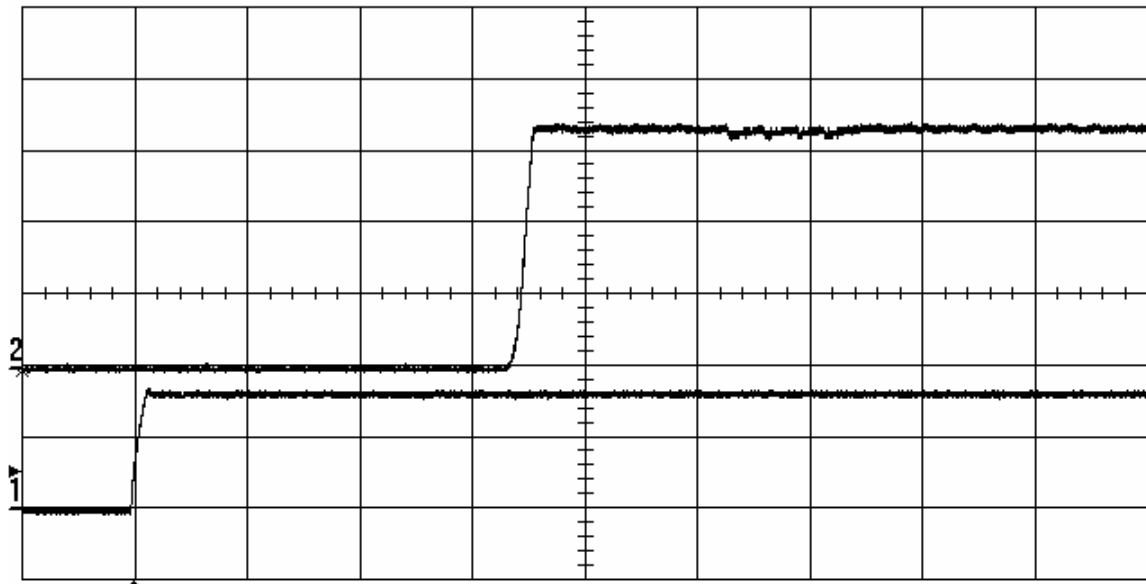
Figure 1 - Power up with  $V_{IN} = 2.4$  V,  $V_{core} = 1.2$  V @ 110 mA,  $V_{i/o} = 3.3$  V @ 50 mA



□ NORMAL

Figure 2 - Power up from Enable when  $V_{IN} = 2.4$  V,  $V_{core} = 1.2$  V @ 110 mA,  $V_{i/o} = 3.3$  V @ 50 mA

Reading Floppy Disk Drive

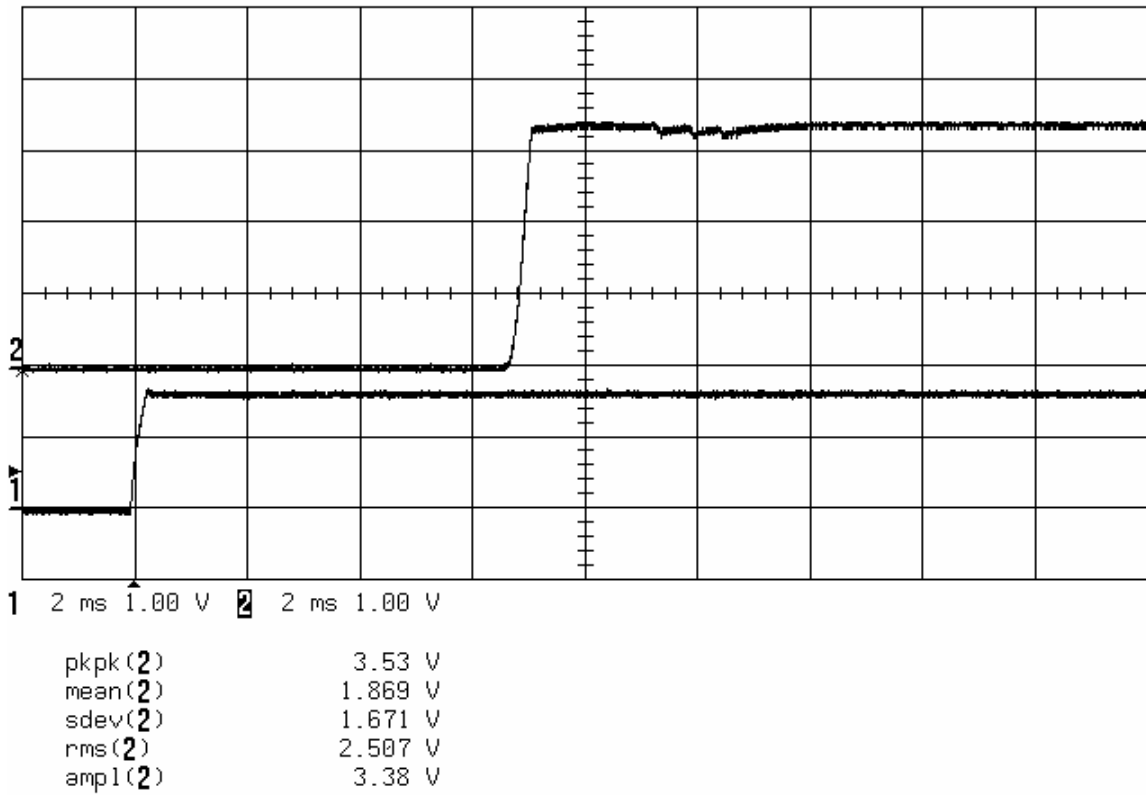


1 2 ms 1.00 V 2 2 ms 1.00 V

pkpk(2)	3.53 V
mean(2)	1.841 V
sdev(2)	1.651 V
rms(2)	2.473 V
ampl(2)	3.34 V

□ NORMAL

Figure 3 - Power up with  $V_{IN} = 2.4$  V,  $V_{core} = 1.6$  @ 228ma,  $V_{i/o} = 3.3$ V @ 70ma



□ NORMAL

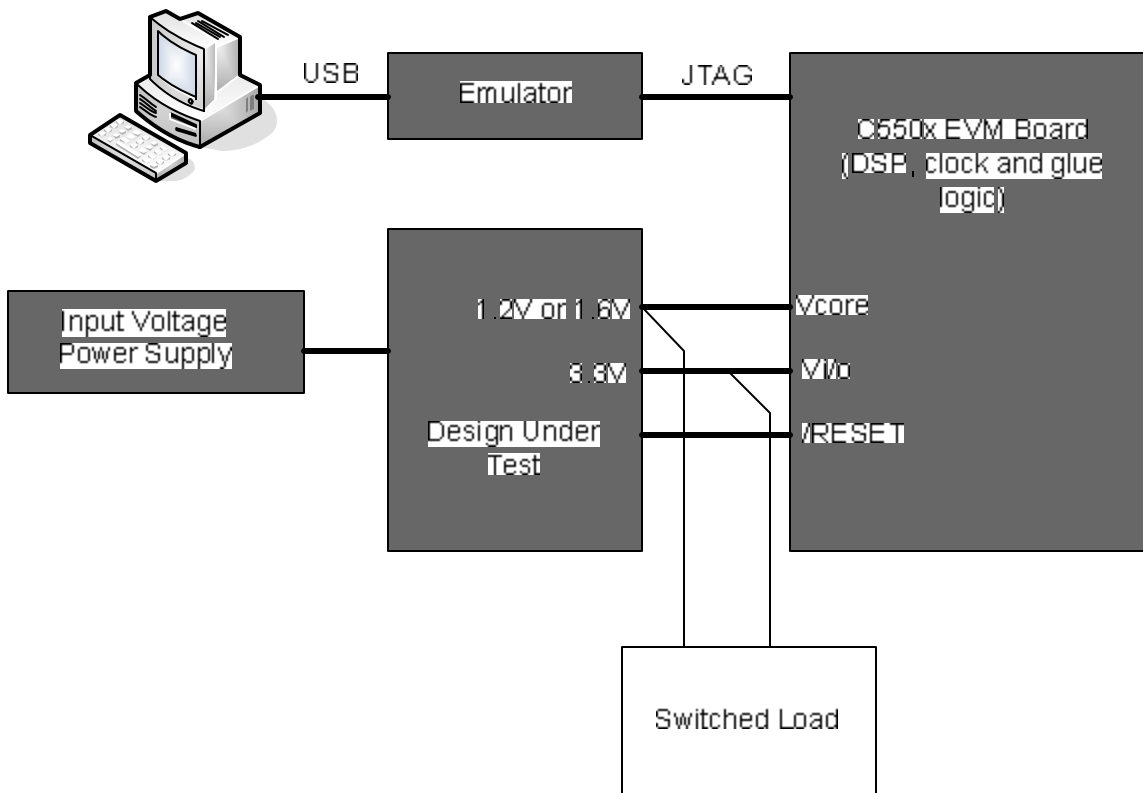
Figure 4 - Power up from Enable when  $V_{IN} = 2.4$  V,  $V_{core} = 1.6$  V @ 228 mA,  $V_{i/o} = 3.3$  V @ 70 mA

**TESTING METHOD:**

The solution was tested on the bench and in an actual DSP circuit. Bench testing included start up into full DSP load, switched load from no load to full DSP load, and power up sequencing. The full DSP load is defined as the current draw a C550x DSP would present to the power supply under worst operating conditions. This full DSP load current is heavily dependent on board layout, firmware configurations, DSP clock speed and core voltage. For testing purposes, the following values were assumed to be the full DSP load current.

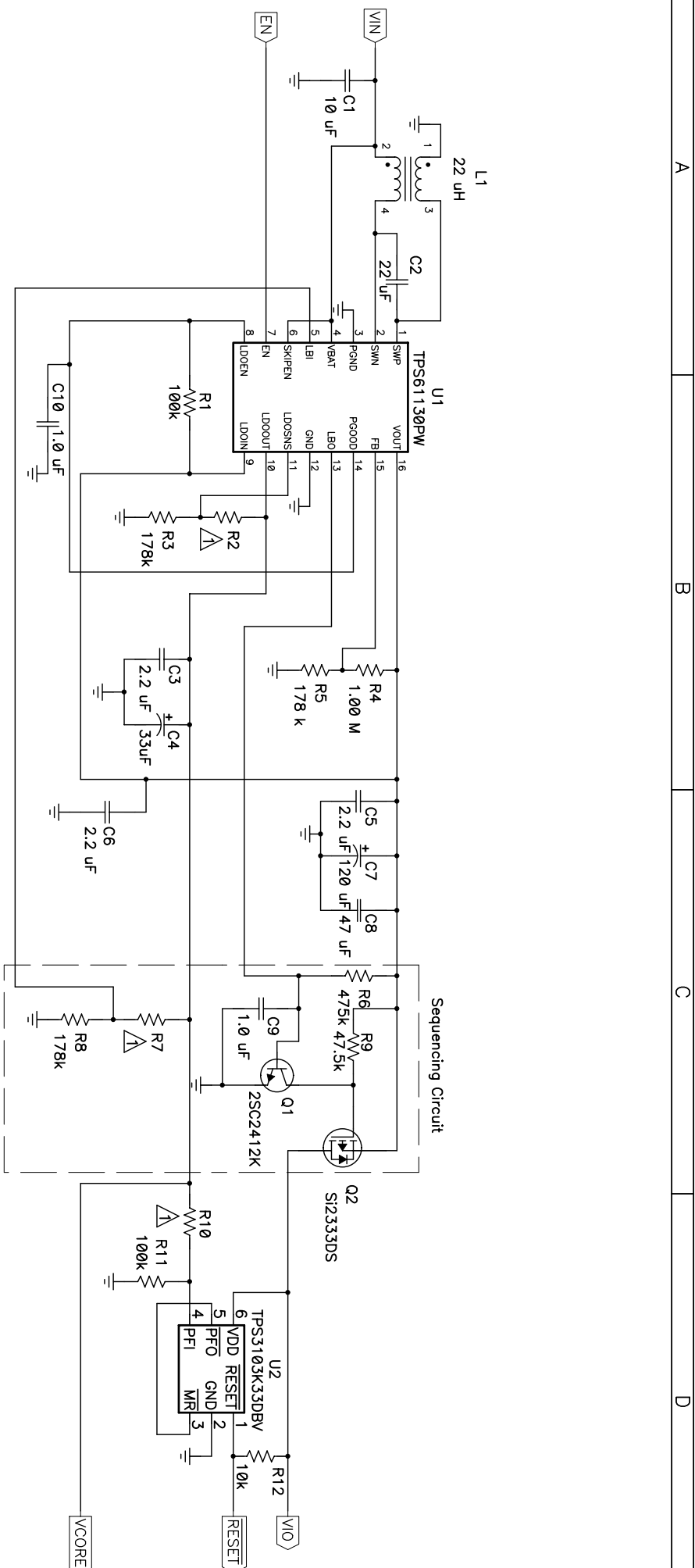
Voltage (V)	Function	Full load current (mA)
1.2	Core	110
1.6	Core	256
3.3	I/O	70

The solution was also tested in an active DSP board. The following test set up was used for this testing:



Filename: PR418_bom.xls						
Date: 02/14/2005						
<b>PR418 BOM</b>						
<b>COUNT</b>						
<b>-001</b>	<b>-002</b>	<b>RefDes</b>	<b>Description</b>	<b>Size</b>	<b>Part Number</b>	<b>MFR</b>
1	1	C1	Capacitor, Ceramic, 10-uF, 6.3-V, X5R, 10%	0805	GRM21BR60J106KE01	muRata
1	1	C2	Capacitor, Ceramic, 22-uF, 10-V, X5R, 10%	1210	GRM32ER61A226KA65	muRata
3	3	C3, C5, C6	Capacitor, Ceramic, 2.2-uF, 6.3-V, X5R, 10%	0805	GRM21BR60J225KC01B	muRata
1	1	C4	Capacitor, POSCAP, 33-uF, 8-V, 70-milliohm, 20%	6032 (C)	8TPC33M	Sanyo
1	1	C7	Capacitor, Tantalum, 120-uF, 10-V, 140-milliohm, 20%	7343 (D)	595D127X0010D2T	Vishay
1	1	C8	Capacitor, Ceramic, 47-uF, 6.3-V, X5R, 10%	1210	GRM32ER60J476ME20	muRata
2	2	C9, C10	Capacitor, Ceramic, 1.0-uF, 10-V, X5R, 10%	0603	GRM188R61A105KA61	muRata
1	1	L1	Inductor, SMT, 22-uH, 811-mA, 429-milliohm	0.300 x 0.300	DRQ74-220	Cooper
1	1	Q1	Transistor, NPN General Purpose, VCE 50V, VCB 60V, VEB 7V, IC 0.15A	SOT-23	2SC2412K	ROHM
1	1	Q2	MOSFET,P-ch, -12 V, 4 A, 51 milliohm	SOT23	Si2333DS	Vishay
2	2	R1, R11	Resistor, Chip, 100k-Ohms, 1/16-W, 1%	0603	Std	Std
1	0	R10	Resistor, Chip, 97.6k-Ohms, 1/16-W, 1%	0603	Std	Std
0	1		Resistor, Chip, 162k-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	R12	Resistor, Chip, 10k-Ohms, 1/16-W, 1%	0603	Std	Std
1	0	R2	Resistor, Chip, 249k-Ohms, 1/16-W, 1%	0603	Std	Std
0	1		Resistor, Chip, 392k-Ohms, 1/16-W, 1%	0603	Std	Std
3	3	R3, R5, R8	Resistor, Chip, 178k-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	R4	Resistor, Chip, 1.00M-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	R6	Resistor, Chip, 475k-Ohms, 1/16-W, 1%	0603	Std	Std
1	0	R7	Resistor, Chip, 205k-Ohms, 1/16-W, 1%	0603	Std	Std
0	1		Resistor, Chip, 332k-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	R9	Resistor, Chip, 47.5k-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	U1	IC, Single Cell or Dual Cell Li-Ion Boost/Secpic Converter	TSSOP-16	TPS61130PW	TI
1	1	U2	IC, Ultra Low Current/Supply, Voltage Supervisor	SOT23-6	TPS3103K33DBV	TI





Voltage	R2	R7	R10
1.2V	249k	205k	97.6k
1.6V	392k	332k	162k

Title		C5000 DSP Attach Design 1	
Size		for 2.4 < Vin < 5.0V	
Number	PR418	Rev	
Date	02/14/05	Drawn by	
Filename	pr418.sch	Sheet	of

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